Analog Moves Up To Full Data Systems

AMPLIFIERS AND MIXED-SIGNAL DATA CONverters have come a long way since their humble beginnings in the first rudimentary monolithic operational amplifier designed by Robert Widlar in 1965. Little did the engineering genius realize at the time that this marvel would soon become a workhorse of the analog world, and that it would spawn a multitude of other single-chip functions as well. Nor could he foresee that it would spark a revolution whose impact would soon be felt in every nook and corner of this world.

In essence, Widlar's first op-amp IC containing a few transistors on a silicon chip broke the ground for an industry that has mushroomed into a more than $35 billion business worldwide and continues to grow. Meanwhile, the dramatic progress in process technology over 36 years has allowed designers to build analog and mixed-signal chips with millions of transistors on a single die.

While the older bipolar process has evolved into the complementary-bipolar (CB) form to maintain its performance lead, the majority of analog and data-converter designers have migrated to popular CMOS and biCMOS processes, whose benefits include low power, high density, and low cost. The major thrust now is to narrow the decades-old technology gap between analog and digital CMOS ICs. Obviously, the designers are racing to build analog ICs on the same mainstream CMOS processes used for digital ICs.

Meanwhile, exotic materials like gallium arsenide (GaAs) have also surfaced to deliver amplifiers and data converters for niche applications. Although substantial gains have been made in the last decade, many challenges remain on the road to a true system-on-a-chip (SoC)—that is, an IC on which high-performance analog functions and high-density digital circuits reside side by side and use the same power supply.

Nevertheless, analog and mixed-signal ICs continue to make strides on all fronts. Continual improvements in process technology and circuit techniques are motivating designers to adopt 0.25-μm and finer CMOS design rules, with a migration path to even smaller geometries. At their current pace, I'm sure they will take full advantage of nanometer gate lengths, sub-2.0-V supply voltages, higher speeds, and lower power consumption in the next few years. The result will be SoC solutions that combine high-performance wideband amplifiers, signal conditioning circuitry, and faster high-resolution analog-to-digital and digital-to-analog converters (ADCs and DACs) with microprocessors, DSPs, and dense logic for a plethora of applications.

Even as CMOS continues to permeate the analog/mixed-signal domain, many applications will still demand the performance of CB transistors, especially those built with silicon-on-insulator (SOI) processes. Silicon germanium (SiGe) will also boost the performance of CB transistors. This will permit designers to develop amplifiers and other linear ICs with much lower noise and higher speed, while reducing power consumption, die size, and supply voltage. Concurrently, designers will focus on miniaturizing packages. In fact, packaging will play a key role in meeting the demands of future applications.

As digital circuits drop below 1-V operation, pressure is mounting to make analog ICs perform well at less than 2 V. Consequently, developers will combine advances in process technologies with circuit techniques to achieve amplifiers with wide bandwidths and faster slew rates at a 1.5-V supply, with pressure to go even below 1 V.

While the density of op-amp arrays on a single CMOS die will continue to rise to serve the needs of multichannel data-acquisition systems, current-feedback amplifiers will set new standards in high-speed amplifier design. And, digitally controlled variable-gain amplifiers will offer a new level of flexibility to designers of analog and mixed-signal circuits.

As for data-converter architectures, the delta-sigma (Δ-Σ) topology pervaded the scene, making precision data converters possible on a 5-V CMOS process without thin-film resistors or

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laser trimming. Today, Δ-Σ exploits the latest advances in CMOS to realize faster, monolithic high-resolution ADCs and DACs with high dynamic range and lower noise. This opens the door to commercially feasible software-defined radios for wireless communications, including digital audio broadcasting. Innovative techniques are also propelling pipelined and successive-approximation-register ADCs to break speed barriers and set new standards,

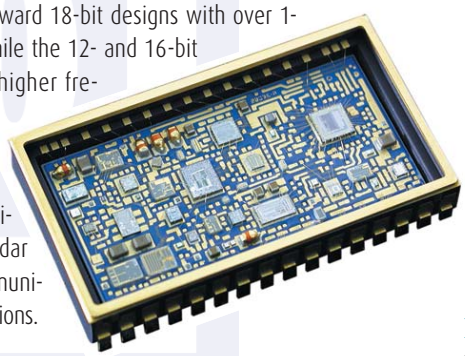
Meanwhile, wideband high-resolution DACs are enabling multicarrier, multimode transmission in cellular basestations. Additionally, advances in CMOS process technology will let designers integrate high-performance data converters with powerful digital signal processing cores to create integrated solutions for a variety of audio, industrial control, and communications applications. Finally, highly integrated analog front ends optimized for a specific task will gain momentum, as developers seek fewer analog and mixed-signal ICs to solve their respective problems.

Innovative designs have helped developers break the speed barrier in the successive-approximation-register (SAR) ADC domain without compromising power. As a result, last year Analog Devices *(www.analog.com)* released a 16-bit SAR ADC with a conversion speed of 1 Msample/s—double the previous record. That record will be broken again this year, and efforts are under way to double it again. Also, many more suppliers will join the fray, introducing faster 16-bit ADCs.

Concurrently, there is a trend to pack multiple SAR ADCs on a chip. In fact, a six-channel version with at least 500-ksample/s conversion capability is in the works, with a drive toward even more channels and faster speeds from a monolithic solution.

As usual, hybrid and board-level designs will take advantage of leading-edge converters to push their performance a step further. To justify the cost, the hybrids and boards will include all the functions needed to deliver complete solutions, with the ability to maintain ac and dc performance over an extended temperature range. This will let time- and frequency-domain applications migrate to higher-resolution ADCs with ease.

Hence, the trend is toward 18-bit designs with over 1-Msample/s sampling, while the 12- and 16-bit parts will be driven to higher frequencies. Also, dual and quad versions in a single package will be driven by applications like radar and communications.



Although the major thrust in will be toward deep- and very deep-submicron CMOS for their cost, low power, and integration advantages, many high-end applications will prefer to pay more for the superior performance of biCMOS. In fact, silicon-germanium (SiGe) bipolars will begin to play an important role in next-generation biCMOS processes. As it evolves in the next few years, it will aid in the integration of high-performance ADCs with RF front ends for many wireless and wireline communications applications. Meanwhile, methodologies and transistor technologies are under development to narrow the technology gap and fabricate these devices in the mainstream digital CMOS process. At this rate, it will not be long before the two merge on the same platform.

Some applications will continue to tap the attributes of the pipelined topology, namely high speed and high resolution at a low supply voltage. As resolution and speed are pushed to new heights, differential techniques and high-performance sample-and-hold circuits will be incorporated to drive power consumption to a new low.

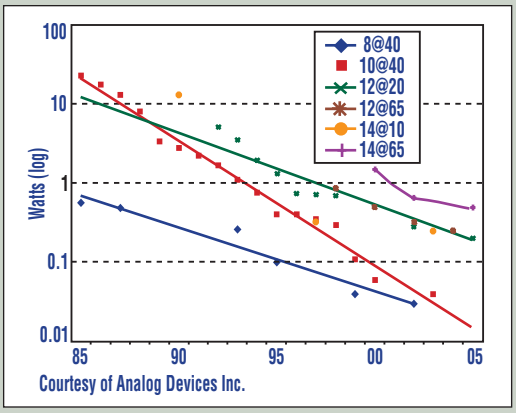
As ADCs strive to adequately serve the appetite of the powerful digital signal processors they encounter in today's DSP-centric solutions, the pressure to push sampling frequencies higher is even greater. Thus, be prepared to see 14-bit ADCs boasting conversion rates of 100 Msamples/s, while 10- and 12-bit versions will come with data rates as high as 200 Msamples/s. Obviously, power consumption will be a real challenge for these faster units. To address this problem, developers will exploit the benefits of low-voltage designs using fine-line CMOS and biCMOS technologies. Development work on 0.18-μm CMOS processes conducted last year will bear fruit this year and in the future.

For motor-control and measurement applications, 8-bit microcontrollers have recently been integrated with low-end analog functions like 8- and 10-bit ADCs, general purpose operational amplifiers, and sensors. Now, developers want to incorporate medium-performance analog/mixed-signal functions on-board with the microcontrollers. So users will start to see faster 12-bit and higher-resolution ADCs, along with wideband op amps, combined with speedier 8-bit and 16-bit microcontrollers.

Analog-To-Digital Converters

INTRODUCED IN THE LATE EIGHTIES, the delta-sigma (Δ-Σ) architecture has become the norm among ADC designers. It has facilitated the integration of dense mixed-signal ICs using advanced CMOS processes. Today, it boasts 24-bit resolution at output data rates as high as 192 kHz, with developers working to deliver even higher performance at lower prices. In fact, the insatiable quest for better audio is motivating developers to adopt multibit topologies with clever dynamic element matching to further boost the ac performance and the dynamic range, while cutting power and cost.

As they begin to tap 0.25-μm and finer CMOS processes, designers will bring more functionality on-chip without compromising on power or die size.



Courtesy of Analog Devices Inc.

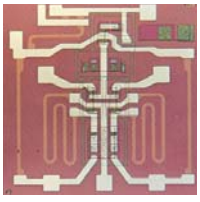
Over time, the low-speed 24-bit chip has become a complete data-acquisition solution to effectively serve markets such as weight and temperature measurement, control, and sensing. As suppliers work to wring more performance from a miniature package, they are also adding more bells and whistles to this line of ADCs. Developers have begun to include filters to reject 50- and 60-Hz signals, even as they are pushing for conversion rates of over 40 ksamples/s. In fact, the trend is toward 100 ksamples/s. For programming, nonvolatile flash memory will be added. The addition of microcontrollers to these ADCs is also on the drawing board.

Speaking of speed, this year's International Solid-State Circuits Conference (ISSCC) will provide a quantum leap in conversion rates for 8-bit ADCs. Agilent Technologies *(www.agilent.com)* will demonstrate a 4-Gsample/s, 8-bit ADC in 0.35-μm CMOS with an accuracy of 6.1 effective bits at 1 GHz. Philips *(www.philips.com)* will unveil a 1.6-Gsample/s, 6-bit flash ADC in 0.18-μm CMOS. Agilent's 8 bitter will consume 4.6 W, and Philips' 6-bit ADC will dissipate 340 mW. Analog Devices will describe a high-performance ADC with on-chip mixer for dual-conversion superheterodyne receivers. This multibit bandpass Δ-Σ ADC with continuous-time LC and active RC resonators, including SC resonators, consumes only 50 mW and offers an unprecedented 90-dB dynamic range. Other highlights include a presentation by Maxim Integrated Products *(www.maxim-ic.com)*, which will introduce a fifth-order, multibit Δ-Σ ADC with 14-bit resolution and a 4-MHz conversion bandwidth. Implemented in 0.18-μm CMOS, it achieves a dynamic range of 80 dB at a low oversampling ratio. In another paper, scientists at Infineon Technologies *(www.infineon.com)*, in cooperation with the Technical University of Munich, Germany, will disclose a Δ-Σ ADC at 0.7 V.

Multichannel chips are not limited to SAR ADCs. Other architectures, like Δ-Σ and pipelined, also permit multiple functions on the same die. Depending on the demands of the application, several high-performance ADCs will be integrated on the same chip to replace multiple parts traditionally used in a multichannel application. For instance, in high-quality audio, six- and eight-channel versions of 24-bit Δ-Σ ADCs will be offered. If flexibility is important, suppliers will provide high-performance multichannel chips with the ability to operate each channel independently of the other.

1954 The first-known SAR 11-bit ADC is built by Bernard Gordon at EPSCO. It was based on vacuum tubes.

1964 Fairchild Semiconductor introduces the industry's first linear IC.



1974 Paul Brokaw invents the Brokaw cell, a bandgap voltage reference.

1978 Analog Devices introduces the first complete 10-bit monolithic ADC.

1988 Crystal Semiconductor unveils the first delta-sigma ADC, a 16-bit resolution device. The seminal delta-sigma patent is granted to Crystal Semiconductor, now a division of Cirrus Logic.

1997 Cirrus Logic releases the first 120-dB audio ADC.

1999 Cirrus Logic introduces the first self-calibrating ADC.