Measuring And Evaluating Dynamic ADC Parameters

Dynamic ADC testing, Part 2

The second half of this article provides test systems and measurement software that can be used to test the dynamic parameters of ADCs.

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ANALOG-TO-DIGITAL converters (ADCs) represent the link between analog and digital worlds in receivers (Rxs), test equipment, and other electronic devices. As outlined last month in Part 1 of this article series, a number of key dynamic parameters provide a fairly accurate correlation of the performance to be expected from a particular ADC. In this concluding article installment, some of the test setups and measurement procedures for testing the dynamic parameters of high-speed ADCs will be presented. This installment will describe the required software tools, hardware configurations, and test instruments needed to evaluate a 10-b, +3-VDC converter-family example.

Table 1: Summarizing the key dynamic ADC parameters

Dynamic parameter	Description definition
Signal-to-noise ratio (SNR)	$SNR_{dB} = 6.02 \bullet N + 1.763$
Signal-to-noise plus distortion (SINAD)	$SINAD_{dB} = 20 \bullet \log_{10} (A_{SIGNAL}[rms]/A_{NOISE}[rms])$
Effective number of bits (ENOB)	$ENOB = (SINAD - 1.763)/6.02$
Total harmonic distortion (THD)	$THD_{dBc} = 20 \bullet \log_{10} (\sqrt{(V_{HD\_2}^2 + V_{HD\_3}^2 + ... + V_{HD\_N}^2)} / V[f_{IN}])$
Spurious-free dynamic range (SFDR)	SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.
Two-tone intermodulation distortion (TTIMD)	$TTIMD_{dB} = 20 \bullet \log_{10} \{\Sigma(A_{IMF\_SUM}[rms] + A_{IMF\_DIFF}[rms])/A_{FUNDAMENTAL}[rms]\}$ IMF_SUM and IMF_DIFF in a TTIMD setup containing 2 input tones only.
Multi-tone intermodulation distortion (MTIMD)	$MTIMD_{dB} = 20 \bullet \log_{10} \{\Sigma(A_{IMF\_SUM}[rms] + A_{IMF\_DIFF}[rms])/A_{FUNDAMENTAL}[rms]\}$ IMF_SUM and IMF_DIFF in and MTIMD setup containing more than 2 (usually up to 4) input tones.
Voltage standing-wave ratio (VSWR)	$VSWR = (1+\lvert\rho\rvert)/(1-\lvert\rho\rvert)$, where: ρ = the reflection coefficient.

A variety of approaches are available for capturing output data from general-purpose and high-speed ADCs, and for analyzing their dynamic performance. The methods in this article represent one proven approach; readers are encouraged to modify these methods as necessary for the application at hand.

In Part 1, numerous definitions and mathematical descriptions of important dynamic parameters for high-speed ADCs were presented (Table 1), including signal-to-noise ratio (SNR), signal-to-noise-plus-distortion (SINAD), effective number of bits (ENOB), total harmonic distortion (THD), and spurious-free dynamic range (SFDR).

To perform adequate dynamic tests on high-speed data converters, it is recommended to use a test or evaluation board supplied (assembled) by the manufacturer, or to follow the circuit-board layout recommendations provided on the ADC's data sheet. This article considers the layout requirements for dynamic testing before delving into the details of hardware and software. An evalu-

ation or characterization board for fast data converters must incorporate high-speed layout techniques. The dynamic performance specified in an ADC's data sheet can usually be replicated by following the basic rules below:

• Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount components to achieve minimum trace length, inductance, and capacitance.

• Bypass analog and digital supplies, references, and common-mode inputs with two 0.1-μF ceramic capacitors in parallel and a 2.2-μF bipolar capacitor to ground.

• Multilayer boards with separate ground and power planes produce the highest level of signal integrity.

• Consider the use of a split ground plane arranged to match the physical location of analog and digital grounds on the ADC's package. The impedance of the two ground planes must be kept as low as possible, and to avoid possible damage or latchup, their AC- and DC-voltage differences (or both) must be less than +0.3 VDC. The two grounds should be joined at a single point, so that noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally, as the point along the gap between the two ground planes that produces optimum results. This connection can be achieved with a low-value surface-mount resistor of 1 to 5 Ω, a ferrite bead, or a direct short.

• As an alternative [if the ground plane is sufficiently isolated from noisy digital systems such as the downstream output buffer and digital signal processor (DSP)], all ground pins can share the same ground plane.

• Route high-speed digital signal traces away from sensitive analog traces.

• Keep all signal lines short and free of 90-deg. turns.

• Always consider the clock input as an analog input. Route it away from actual analog inputs and other digital signal lines.

A proper test setup and the right test equipment is necessary to realize the performance specified for a given converter (Figs. 1a and 1b). The following hardware has proven to be efficient, and is therefore recommended for the test setup (although readers are invited to substitute equivalent equipment):

For the DC power supply, a model E3620A dual-supply unit from Agilent Technologies (Santa Clara, CA) [formerly Hewlett-Packard Co.] can provide voltages and currents of 0 to +25 VDC and 0 to 1 A, respectively. Separate supplies should be used for the analog and digital nodes. Each supply should provide at least 100 mA of output drive current.

For the clock-signal function generator, a model HP8662A signal generator from Agilent Technologies provides stable signals. The clock input for the device under test (DUT) accepts complementary-metal-oxide-semiconductor (CMOS)-compatible clock signals. This signal should have low phase noise and fast rise and fall times, because the high-speed ADC has a 10-stage pipeline, and its interstage conversion depends on the repeatability of the rising and falling edges of the external clock. Sampling occurs on the falling edge of the clock signal, so that edge should have the lowest possible jitter/phase noise. Significant aperture jitter limits the ADC's SNR performance as follows:

$SNR_{dB} = 20\log_{10}(0.5\pi f_{IN} \times t_{AJ})$,

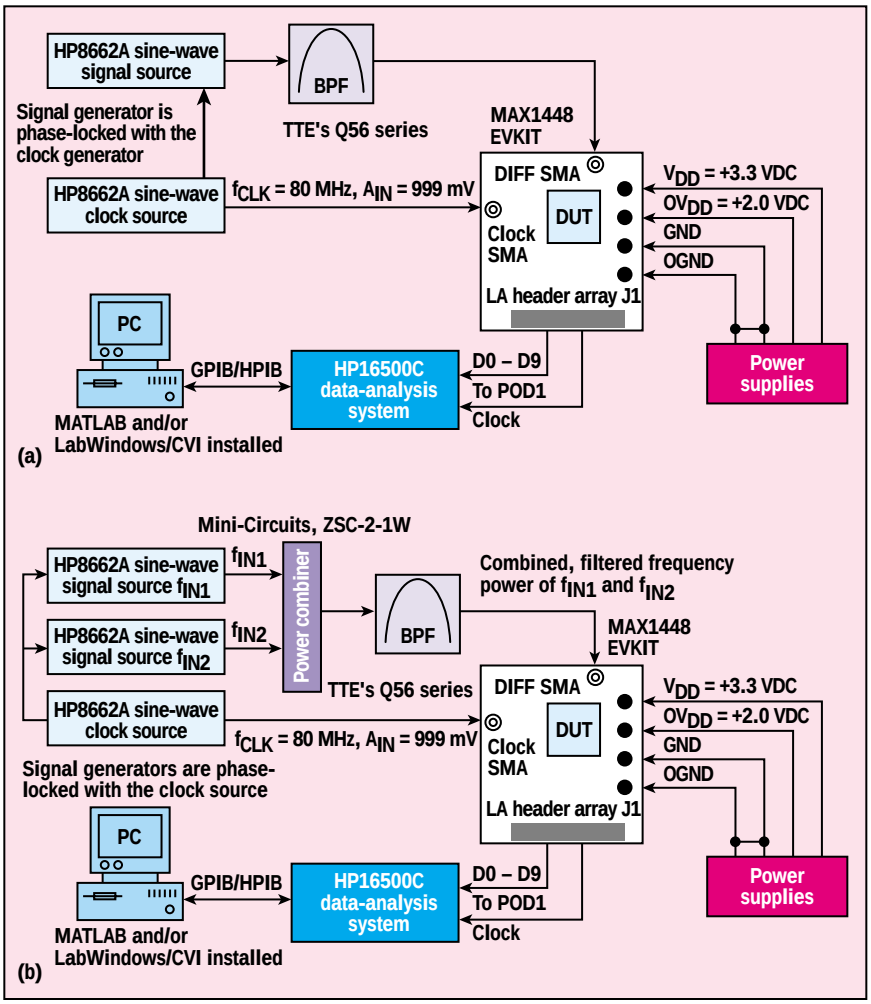
where:

f_{IN} = the analog input frequency, and

t_{AJ} = the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications.

For the input-signal function generator, another model HP 8662A sig-



1. This test setup is suitable for evaluating SNR, SINAD, THD, and SFDR (a) while it can be modified for testing two-tone IMD performance (b).

nal generator from Agilent Technologies is recommended. For proper operation, this function generator should be phase-locked to the clock-signal generator.

For the logic analyzer, a model HP16500C from Agilent Technologies offers flexible and accurate measurement power. Depending on the number of points in the proposed Fast Fourier transform (FFT), it may be possible to capture the data using a logic analyzer with less memory depth than the HP16500C, such as the 4-kB data record available in the firm's model HP1663C/EP logic analyzer.

For the analog bandpass filter, the Q56 series elliptical function bandpass filters from TTE (Los Angeles, CA) provide high rejection with low insertion loss. The series is available with cutoff frequencies of 7.5, 20, 40, and 50 MHz.

Digital multimeters (DMMs) for the measurement system are available from a variety of sources, including Fluke Manufacturing Co. (Everett, WA), Keithley Instruments (Cleveland, OH), and Hewlett-Packard Co. (Palo Alto, CA), including the handheld model HP2373A and the AC-powered model HP34401A. The DMMs are used to check for proper reference voltages, supplies, and common-mode voltages.

EVALUATING THE DUT

To simplify evaluation of the DUT, it was measured with a performance-optimized, fully assembled and tested surface-mount EVKit evaluation board. Follow the steps below to configure the setup and operate this board. One should complete all the connections before turning on the power supplies or enabling the function generators.

- Apply a +3.0-VDC analog power supply to pins VAIN1 and VAIN2, and connect its ground terminal to pin AGND.
- Apply a +3.0-VDC digital power supply to pins VDIN1 and VDIN2, and connect its ground terminal to DGND.
- Verify that no shunts are installed for jumpers JU1 (shutdown disabled) and JU2 (digital outputs enabled).
- Connect the clock-function generator to the CLOCK-SMA connector.
- Connect the output of the analog-signal function generator to the input of one of the bandpass filters.
- To evaluate differential analog signals, verify that shunts are installed on pins 1 and 2 of jumpers JU3 and JU4. Connect the output of the bandpass filter to the DIFF-IN-SMA connector.
- To evaluate single-ended analog signals, verify that shunts are installed on pins 2 and 3 of jumpers JU3 and JU4, and connect the output of the bandpass filter to the SINGLE-IN-SMA connector.

• Connect one of the logic-analyzer interface cables (pods) to the square pin header J1.

• Turn on both power supplies, and verify with a voltmeter that a voltage of +1.20 VDC is present across test points TP4 and TP5. If necessary, adjust potentiometer R34 to obtain the required +1.20 VDC.

• Enable the function generators. Set the clock-function generator to its maximum output amplitude (999 mV for the suggested HP8662A signal generator) and a clock frequency of f_{CLK} = 80 MHz. Set the analog signal-function generator to the desired input tone, with any amplitude between 10 μV and 999 mV. Note that the input amplitude and frequency must be selected according to the bandpass filter's corner frequency. Bandpass filters used in evaluating high-speed data converters usually tolerate a narrow passband. To achieve optimum performance (depending on filter type and manufacturer), set the input tone to within 5 percent of the corner frequency. Since the filter attenuates the generator's output signal, set the generator's amplitude slightly higher to achieve the desired full-scale input specification.

• For proper operation, phase-lock the two function generators [or three function generators, if testing for two-tone intermodulation distortion (IMD)].

• Synchronize the logic analyzer with the external clock signal from the board, and set the logic analyzer to latch data on the clock's rising edge.

• Enable the logic analyzer and begin collecting data. Data can be stored on a floppy disk, on the logic analyzer's hard disk, or on a data-acquisition (DAQ) board communicating through the logic analyzer's general-purpose-interface-bus (GPIB) port.

Now that the necessary steps for test setup and hardware configuration have been completed and the system is ready to capture data from the DUT, it is time to select the software tools for data capture and analysis.

• LabWindows/CVI from National Instruments (Austin, TX) serves as the required data capture and communications link between the logic analyzer and the DAQ-controller board. (The C-language-based program routine used for this purpose will not be discussed in this article.)

• MATLAB from The MathWorks (Natick, MA) is a powerful tool that performs the FFT and dynamic analysis of the captured data.

To help understand how a MATLAB program routine analyzes and graphs the dynamic performance of a high-speed data converter, the next section reviews some of the FFT and power-spectrum basics.

The FFT and the power spectrum are adequate tools for measuring and analyzing signals from captured data records. They can capture time-domain signals, measure their frequency content, convert the results to convenient units, and display them. To perform FFT-based measurements, however, one must understand the issues and calculations involved. Basic functions of an FFT-based signal analysis are the FFT itself and the power spectrum. Both are extremely useful for measuring the

frequency content of stationary or transient signals. FFTs usually produce the average of a signal's frequency content over the time interval that the signal was acquired. Thus, FFTs are always recommended for stationary-signal analysis.

Among the most basic and important computations in signal analysis are the use of the FFT in converting from a two-sided to a single-sided power spectrum, adjusting the frequency resolution, and displaying the spectrum. A power spectrum usually returns a matrix containing the two-sided representation of the time-domain signal power in the frequency domain. The values in this matrix are proportional to the amplitude squared of each frequency component making up the time-domain signal.

A plot of the two-sided power spectrum usually contains negative and positive frequency components. Actual frequency-analysis tools, however, focus on the positive half of the frequency spectrum only, noting that the spectrum of a real signal is symmetrical around DC. Negative frequency information is therefore irrelevant. In a two-sided spectrum, half the energy resides in the positive frequencies and half in the negative frequencies. To convert from a two-sided spectrum to a single-sided spectrum, therefore, one must discard the second half of the matrix and multiply every point (except DC) by two.

The frequency range and resolution on the x-axis of a spectrum plot depend on the sampling rate and the size of the data record (the number of acquisition points). The number of frequency points or lines in the power spectrum is N/2, where N is the number of signal points captured in the time domain. The first frequency line in the power spectrum always represents DC. The last frequency line can be found at $f_{SAMPLE}/2 - f_{SAMPLE}/N$. Frequency lines are spaced at even intervals of f_{SAMPLE}/N, commonly referred to as a frequency bin or FFT bin (Fig. 2). Bins can also be computed with reference to the ADC's sampling period:

$$Bin = f_{SAMPLE}/N = 1/N\Delta t_{SAMPLE}$$

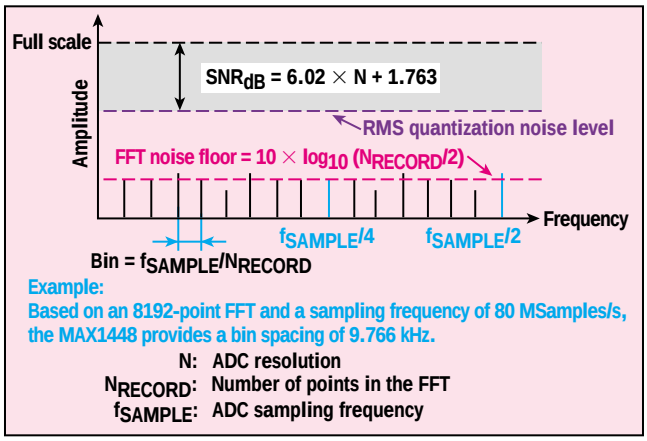
where:

f_{SAMPLE} = the sampling frequency, and

Δt_{SAMPLE} = the sample time differential.

For example, with a sampling frequency of f_{SAMPLE} = 82.345 MHz and a record length of 8,192 data points, the distance between each frequency line in the FFT plot is exactly 10.052 kHz. (See Fig. 1 of Part 1 of this article series, *Microwaves & RF*, November 2000, p. 75).

The calculations for the frequency axis (x-axis) are proof that the sampling frequency determines the range or bandwidth of the frequency spectrum. For a given sampling frequency, the number of points acquired in the time domain determines the resolution frequency. To increase the resolution for a given frequency range, the depth of the data record can be increased at the same frequency (see the sidebar for program-code extraction No. 1).



2. An FFT graph is composed of a number of separate frequency/FFT data bins.

Window functions are common in FFT analysis, and their proper use is critical in FFT-based measurements. The following discussion of spectral leakage stresses the need to select an appropriate window function and scale it properly for a given application. To accurately determine spectral leakage, however, it may not be enough to use adequate signal-acquisition techniques, convert a two-sided power spectrum into a single-sided one, and rescale the result. To gain a better understanding of this term, one should perform an N-point FFT on a spectrally pure sinusoidal input.

Spectral leakage is the result of an assumption in the FFT algorithm that the time record is precisely repeated throughout all time, and that all signals contained in this time record are periodic at intervals corresponding to the length of the time record. However, a nonintegral number of cycles in the time record ($f_{IN}/f_{SAMPLE} \sim N_{WINDOW}/N_{RECORD}$) violates this condition and causes spectral leakage (Fig. 3) [See also the second sidebar in Part 1]. Only two cases can guarantee the acquisition of an integral number of cycles:

- Synchronous sampling with respect to the input tone.
- The capture of a transient signal that fits entirely into the time record.

Table 2: Characteristics of frequently used window functions (see also MATLAB program code)

Window type	−3-dB mainlobe width	−6-dB mainlobe width	Maximum sidelobe level	Sidelobe rolloff rate
No window (uniform)	0.89 bins	1.21 bins	−13 dB	20 dB/decade 6 dB/octave
Hanning	1.44 bins	2.00 bins	−32 dB	60 dB/decade 18 dB/octave
Hamming	1.30 bins	1.81 bins	−43 dB	20 dB/decade 6 dB/octave
Flat top	2.94 bins	3.56 bins	−44 dB	20 dB/decade 6 dB/octave

In most cases, however, the application deals with an unknown stationary input. (A stationary signal is one that is present before, during, and after the data capture.) This means that there is no guarantee of sampling an integral number of cycles. Spectral leakage distorts the measurement by spreading the energy of a particular frequency component over the adjacent frequency lines or bins. Selecting an appropriate window function can minimize the effects of this spectral leakage.

To fully understand how a particular window function affects the frequency spectrum, one must take a closer look at the frequency characteristics of windows. Windowing of the input data is equivalent to convolving the spectrum of the original signal with the spectrum of the window. Even for coherent sampling, the signal is convolved with a rectangular-shaped window of uniform height. (Performing an FFT with no apparent window function selected is frequently referred to as performing the FFT with a "uniform" or "rectangular" window.) Such convolution shows a typical sine-function characteristic spectrum.

The real-frequency characteristic of a window is a continuous spectrum consisting of a main lobe and several side lobes. The main lobe is centered at each frequency component of the signal in the time domain. Side lobes approach zero at intervals on each side of the main lobe. An FFT, on the other hand, produces a discrete frequency spectrum. The continuous, periodic spectrum of a window is sampled by the FFT, just as an ADC would sample an input signal in the time domain. What appears in each frequency line of the FFT is the value of the continuous convolved spectrum at each FFT frequency line.

If the frequency components of the original signal match a frequency line exactly, as is the case when one acquires an integral number of cycles, one sees only the main lobe of the spectrum. Side lobes do not appear because the window spectrum approaches zero at bin-frequency intervals on either side of the main lobe. If a time record does not contain an integral number of cycles, the continuous spectrum of the window is shifted from the main lobe center at a fraction of the frequency bin that corresponds to the difference between the frequency component and the FFT frequency lines. This shift causes the sidelobes to appear in the spectrum. So, the window's sidelobe characteristics directly affect the extent to which adjacent frequency components "leak into" the neighboring frequency bins.

WINDOW CHARACTERISTICS

Before choosing an appropriate window, it is necessary to define the parameters and characteristics that enable users to compare windows. Such characteristics include the –3-

dB main lobe width, the –6-dB main lobe width, the maximum sidelobe level, and the sidelobe rolloff rate (Table 1).

Sidelobes of the window are characterized by the maximum sidelobe level, defined as the maximum sidelobe level in decibels with respect to the main lobe's peak gain, and the sidelobe rolloff, which is defined as the asymptotic decay rate (in decibels/decade or decibels/octave of frequency) of the sidelobe peaks (Table 2).

Different windows suit different applications, and to choose the right spectral window, one has to guess the signal-frequency content. If the signal contains strong interfering frequency components distant from the frequency of interest, one should choose a window whose side lobes have a high rolloff rate. If strong interfering signals are close to the frequency of interest, a window with low maximum levels of side lobe is more suitable.

If the frequency band of interest contains two or more signals close to each other, spectral resolution becomes important. In that case, a window with a narrow main lobe is better. For a single-frequency component in which the focus is on amplitude accuracy rather than its precise location in the frequency bin, a window with a broad main lobe is recommended. Finally, coherent sampling (instead of a window) is recommended for a flat or broadband frequency spectrum (see the sidebar for program-code extraction No. 2).

The Hanning window function, which provides good frequency resolution and reduced spectral leakage, offers satisfactory results in most applications. The flat-top window has good amplitude accuracy, but its wide main lobe provides poor frequency resolution and more spectral leakage. The flat-top window has a lower maximum sidelobe level than the Hanning window, but the Hanning window has a faster rolloff rate.

An application of only transient signals should have no spectral windows at all, because they tend to attenuate important information at the beginning of the sample block. With a transient signal, a nonspectral window such as a force or exponential window should be chosen.

Selecting an appropriate window is not easy, but if the signal content is unknown, one can start with the Hanning characteristic. It is also an excellent idea to compare the performance of multiple window functions to find the one most suitable for a particular application (Table 3).

With the knowledge gained in preceding sections of this article, the following program-code extraction should be easy to understand. Based on the FFT, power spectrum, and attention to spectral leakage and window functions, the specifications SNR, SINAD, THD, and SFDR are calculated as follows, using MAT-

LAB:

$SNR = 10\log_{10}(P_s/P_n)$

$SINAD = 10\log_{10}[P_s/(P_n + P_d)]$

$THD = 10\log_{10}(P_d/Ph_{(1)})$

$SFDR = 10\log_{10}[P_{h(1)}/\max(P_{h(2:10)})]$

where:

P_s = the signal power,

P_n = the signal noise,

P_d = the distortion power caused by second-through-fifth-order harmonics,

$P_{h(1)}$ = the fundamental harmonic power, and

$P_{h(2:10)}$ = the harmonic power of the second through ninth harmonics (see the sidebar for program-extraction code No. 3 for computing the power-spectrum level).

Based on MATLAB source code, a high-speed ADC from Maxim Integrated Products (Sunnyvale, CA), the MAX1448, was tested not only for its data-sheet specifications, but also for many other over- and under-sampling input frequencies as well. It achieved excellent dynamic performance for all conditions.

Two-tone IMD can be a tricky measurement, since the additional equipment required—a power combiner that combines two input frequencies—can contribute unwanted IM products that falsify the ADC's IMD. The following conditions must be carefully observed to optimize IMD performance, although they make the selection of proper input frequencies a tedious task.

First, the input tones must fall into the passband of the input filter. If these tones are close together (several tens or hundreds of kilohertz for a megahertz bandwidth), an appropriate window function must be chosen as well. Placing them too close together, however, may allow the power combiner to falsify the overall IMD readings by contributing unwanted second- and third-order IMD products (depending on the location of the input tones within the passband). Spacing the input tones too far apart may call for a different window type that has less frequency resolution.

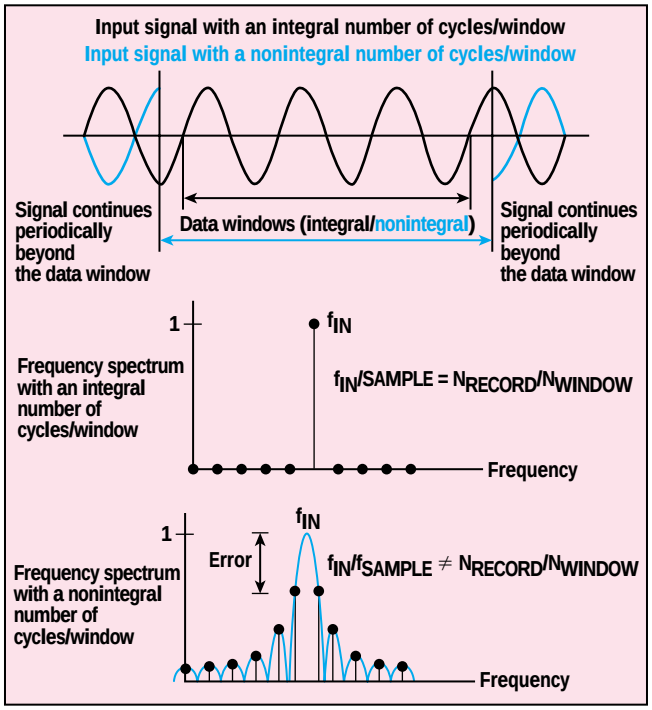
The setup also requires a minimum of three phase-locked signal generators. This requirement seldom poses a problem for test labs, but generators have differing capabilities for matching frequency and amplitude. Compensating such mismatches to achieve (for example) a –0.5-dB full-scale (FS) two-tone envelope and signal amplitudes of –6.5 dB full scale will increase the effort and test time required (see the sidebar for program-code extraction No. 4).

In short, besides the points covered above, many other issues confront an engineer trying to determine the dynamic range of a high-speed ADC by capturing its signals and analyzing them. Unfortunately, mistakes are easily made in spectral-measurement procedures. However, this task of DAQ and analysis is eased by an understanding of FFT-based measurement and related computations, the effect of spectral leakage and how to prevent it, and the necessary layout techniques and equipment.

A free copy of the MATLAB source code used in the evaluation of the MAX1448 high-speed ADC is available free upon request from the author at tanja_hofner@maximhq.com, or by sending an e-mail to jbrowne@penton.com and requesting a copy of the MATLAB code. ••

Table 3: Signal content versus window selection and advantages

Window type	Signal content	Window characteristics
No window (uniform)	Broadband random Closely spaced sine-wave signals	Narrow mainlobe Slow rolloff rate Poor frequency resolution
Hanning	Narrowband random signals Nature of content is unknown Sine wave or combination of sine-wave signals	High maximum sidelobe level Good frequency resolution Reduced leakage Faster rolloff rate
Hamming	Closely spaced sine-wave signals	Good spectral resolution Narrow mainlobe
Flat top	Sine wave with need for amplitude accuracy	Good amplitude accuracy Wide mainlobe Poor frequency resolution More spectral leakage



3. This plot shows the effects of data windows on spectral leakage.

For further reading

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