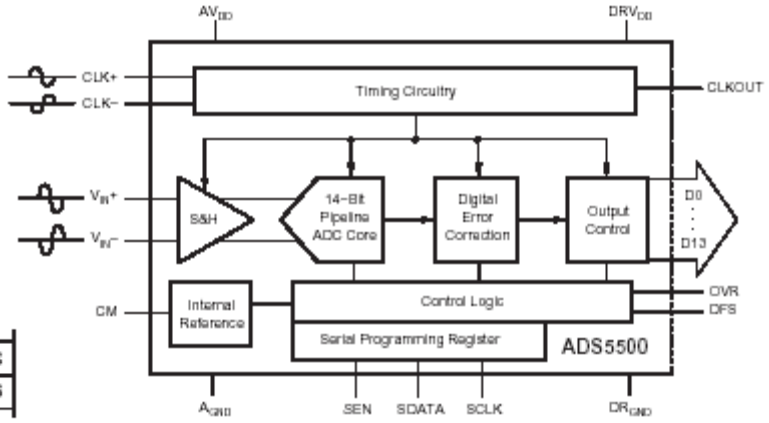
ADS5500

14-Bit, 125MSPS
Analog-to-Digital Converter

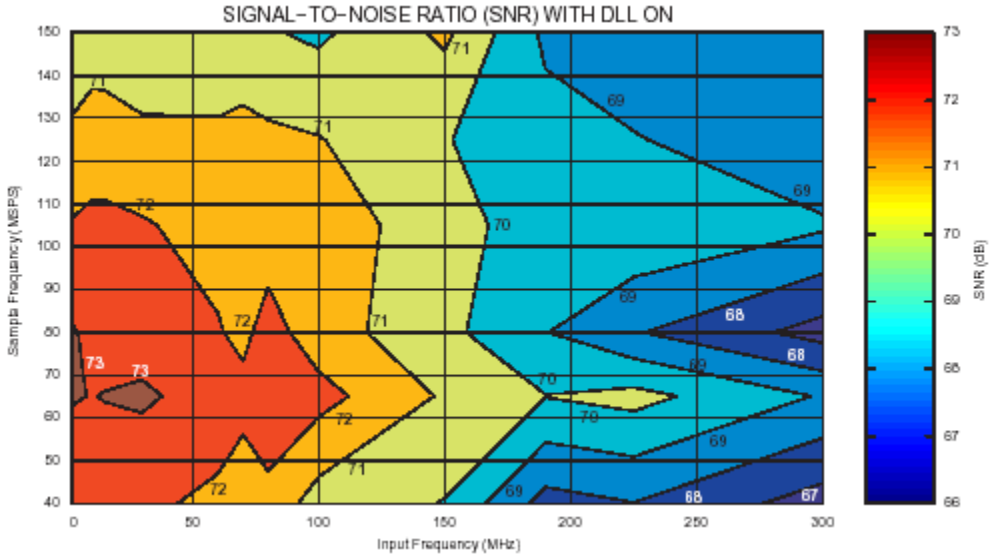


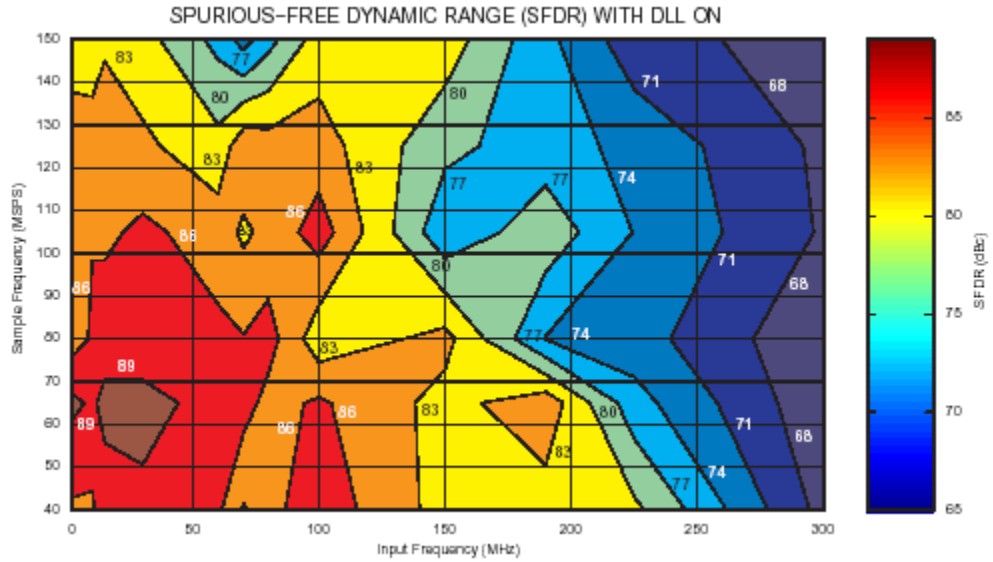
RECOMMENDED OPERATING CONDITIONS

ADCLK input sample rate (sine wave) $1/t_C$	DLL ON	60	125	MSPS
	DLL OFF	10	80	MSPS

digital phase lock loop (DLL).

Complex relationship between converter performance and signaling conditions





ADS5500 home: http://www.ti.com/corp/docs/landing/ads5500/

TABLE 2–REPRESENTATIVE PIPELINED ADCs

Manufacturer	Model	Resolution (bits)	NMC* (bits)	Speed (M samples/sec)	NMC* speed product (Mbps)	Maximum power dissipation (mW)	Power efficiency (Mbps/mW)	Typical −3-dB bandwidth (MHz)	Package	Price (1000)
Analog Devices	AD9433	12	12	125	1500	1250	1.2	750	PQ4-52**	$80
Texas Instruments	ADS809	12	11	80	880	945	0.9	1000	TQFP-48	$29.95
Maxim	MAX1448	10	10	80	800	160 EST	5.0	400	TQFP-32	$8.35
Analog Devices	AD6644	14	13	65	845	1500	0.6	250	LQFP-52	$39
Analog Devices	AD9226	12	12	65	780	500	1.6	750	SSOP-28	$18.55
Maxim	MAX1446	10	10	60	600	135 EST	4.4	400	TQFP-32	$7.35
STMicroelectronics	TSA1201	12	12	50	600	158	3.8	1000	TQFP-48	$17
STMicroelectronics	TSA1002	10	10	50	500	158	3.2	100	TQFP-48	$5.95
Maxim	MAX1444	10	10	40	400	90 EST	4.4	400	TQFP-32	$5.85

*NMC = no missing codes; **PQ4 = "power quad 4," according to Analog Devices.

EDN | May 10, 2001

Blindingly fast ADCs

TABLE 3–HIGH-SPEED PIPELINE ADCs

Manufacturer	Model	Channels	Resolution (bits)	NMC* resolution (bits)	Minimum ENOB (bits)	At input frequency (MHz)	Maximum sampling rate (M samples/sec)	ENOB-sample rate product (Mbps)	Maximum power dissipation (mW)	Minimum power efficiency (Mbps/mW)	Bandwidth (full power) (MHz)	Bandwidth (−3 dB) (MHz)	Pipe latency (cycles)	Package	Price (1000)
Texas Instruments	ADS5270	Eight	12	12	11.3**	5	40	453**	904**	TBD		300**	6.5	TQFP-80	$45
Texas Instruments	ADS5271	Eight	12	12	11.3**	5	50	567**	936**	TBD		300**	6.5	TQFP-80	$50
Texas Instruments	ADS5272	Eight	12	12	11.3**	5	65	737**	984**	TBD		300**	6.5	TQFP-80	$65
Maxim	MAX1126	Four	12	12**	10.8	19.3	40	431	616	2.8	100		6.5	QFN-68	$31.85
Maxim	MAX1127	Four	12	12**	10.8	19.3	65	699	648	4.31	100		6.5	QFN-68	$35.85
Analog Devices	AD9229	Four	12	12	11.4**	10.3	65	740**	1250**	2.37	500		Nine	LFCSP-48	$34
Analog Devices	AD9289	Four	8	8	7.5**	10.3	65	488**	330**	5.91	400		Six	BGA-64	$10.52
National Semi	ADC12DL066	Two	12	12	10.2	10	66	675	895	1.51	450		Six	TQFP-64	$25
Texas Instruments	ADS5500	One	14	14	11.1	70	125	1386	875	1.58	750		16.5	TQFP-64	$95
TelASIC	TC1410	One	14	14	11.3***	225	240	2721***	15455	0.18	1000		N/A	BGA-256	$120
Maxim	MAX1122	One	10	10	8.9	100	170	1518	630	2.41	600		Eight	QFN-68	Start
Maxim	MAX1123	One	10	10	8.8	100	210	1857	639	2.91	600		Eight	QFN-68	at
Maxim	MAX1124	One	10	10	8.6	100	250	2149	657	3.27	600		Eight	QFN-68	$36.85
Maxim	MAX1418	One	15	15	11.5	70	65	748	2340	0.32	260		Three	QFN-56	start
Maxim	MAX1419	One	15	15	11.8	15	65	769	2305	0.33	260		Three	QFN-56	at
Maxim	MAX1427	One	15	15	11.8	15	80	947	2305	0.41	260		Three	QFN-56	$29.75
Linear Technology	LTC1749	One	12	12	11.4***	30	80	913***	1690	0.54	500		Five	TSSOP-48	$19.55
Linear Technology	LTC1750	One	14	14	11.8***	30	80	945***	1690	0.56	500		Five	TSSOP-48	$32.30

*NMC=no missing codes.
**Typical.
***Estimated.

EDN | May 13, 2004

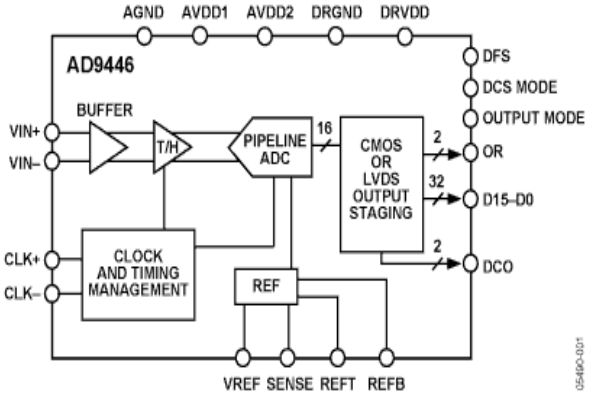
High-speed ADCs: preventing front-end collisions

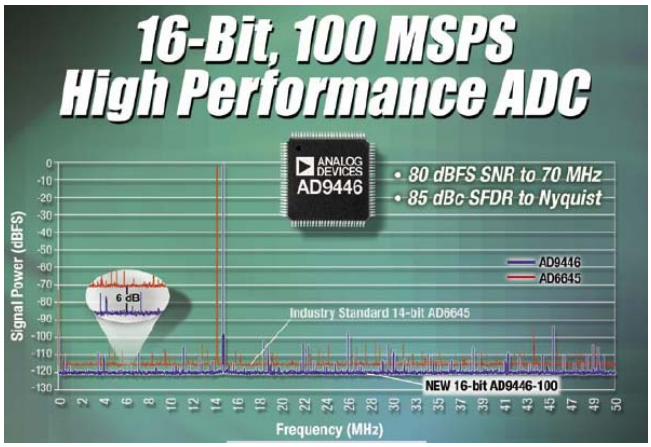
COMPARISON OF **HIGH-SPEED ADC** OUTPUT OPTIONS				
Parameter	**Output Type**			
	CMOS	**Demultiplexed CMOS**	**Parallel LVDS**	**Serial LVDS**
Where used (**conversion rates**)	Up to 100 MSPS, depending on converter resolution	At 200 MSPS and higher	Critical at 100 MSPS to maintain ADC's dynamic performance for converters with 12 bits or more	May be used at speeds as low as 10 MSPS, particularly with multichannel devices

****

Norwood, MA (5/9/2005) - Analog Devices, Inc. (NYSE:ADI) the world leader in data converter technology, today introduced the industry's first **16-bit** analog-to-digital converter (ADC) to deliver **100-MSPS** (mega-samples-per-second) data rates while offering both best-in-class signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

AD9446 - 16-Bit, 80 MSPS / 100 MSPS A/D Converter





Features

- 100 MSPS guaranteed sampling rate
- 100 dB two-tone SFDR with 30 MHz and 31 MHz
- **81.6 dB SNR with 30 MHz input** (3.2 Vp-p input, 80 MSPS)
- **90 dBc SFDR with 30 MHz input** (3.2 Vp-p input, 80 MSPS)
- Excellent linearity DNL = ±0.5 LSB typical INL = ±3.0 LSB typical
- 2.3 W power dissipation
- 3.3 V and 5 V supply operation
- 2.0 V p-p to 3.2 V p-p differential full-scale input
- **LVDS outputs (ANSI-644 compatible) or CMOS outputs**
- Data format select (Offset Binary or 2's compliment)
- Output clock available

http://www.analog.com/en/prod/0%2C2877%2CAD9446%2C00.html

ADCs deliver faster sampling rates with new levels of dynamic range

Combining a 0.35-micron biCMOS process with improved circuit design and optimal layout and simulation techniques, Analog Devices Inc. has launched two high-performance, high-resolution analog-to-digital converters (ADCs) with unprecedented signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) performance at faster sampling rates. While the 16-bit part delivers 100 megasamples per second (Msps) data rates, the 14-bit part boasts 125 Msps sampling rate.

Together, the reduced noise and 16-bit resolution of the AD9446 enables developers of instrumentation and automated test and measurement equipment, data acquisition systems, medical imaging devices and advanced military/aerospace communication subsystems to build more performance overhead into their designs by capturing a better representation of the input signal using fewer samples. Likewise, the 14-bit AD9445 is optimized for multicarrier, multimode receivers such as those found in next-generation cellular infrastructure equipment. The device's high resolution and outstanding performance also make it suitable for antenna array positioning, power amplifier linearization, broadband wireless, radar and infrared imaging, medical imaging, communications instrumentation, and software-defined and cognitive radios.

As part of a family of high-speed converters optimized to deliver higher sample rates and improved dynamic performance at competitive prices, the 16-bit AD9446 achieves a 10x increase in sample rates over other ADCs in its class while offering 90 dBc SFDR and 80 dBfs SNR at baseband—a full 6 dB better than the SNR achieved by the closest competing ADC, claims ADI. The AD9446 is available in an 80 Msps speed-grade option that also achieves industry-leading 85 dBc SFDR, while improving the SNR by another 2 dB to 82 dBfs SNR.

For high-performance test and measurement applications that use digital time sampling for frequency and time-domain analysis, the AD9446 significantly lowers aperture jitter to just 60 fs (femto seconds), compared to the 250 fs to 300 fs range of competing ADCs.

"Today's industrial equipment manufacturers are under constant pressure to scale the performance of their products without introducing new sources of signal noise," said John Hussey, vice president of the high-speed converter group at Analog Devices. "In the case of advanced test equipment, for example, designers are on the lookout for ways to improve noise while maintaining a wide enough performance margin to ensure the reliable, repeatable testing of high-performance components, boards and systems. To build equipment capable of accurate testing and rapid debugs, these manufacturers need the resolution, speed and low noise characteristics that are enabled by the AD9446."

In addition to delivering the industry's best 16-bit SFDR and SNR at baseband, the AD9446 is accurate and features a typical 16-bit differential non-linearity (DNL) of ±0.5 LSB and a typical16-bit integral

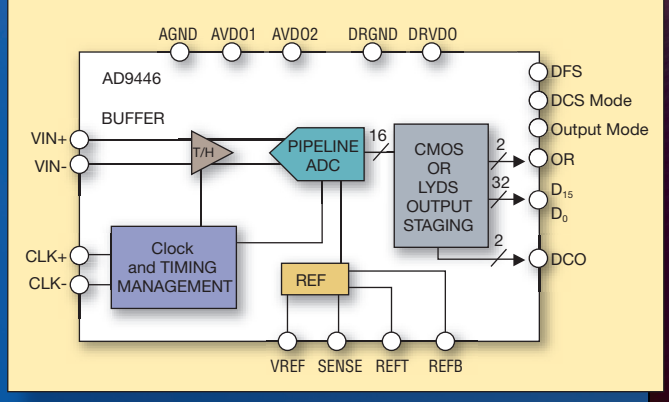


Figure 1. AD9446 features parallel low-voltage differential signaling (LVDS) outputs, including an output clock, which simplifies the interface to digital processing components and reduces the potential for digital noise coupling back into the ADC core.

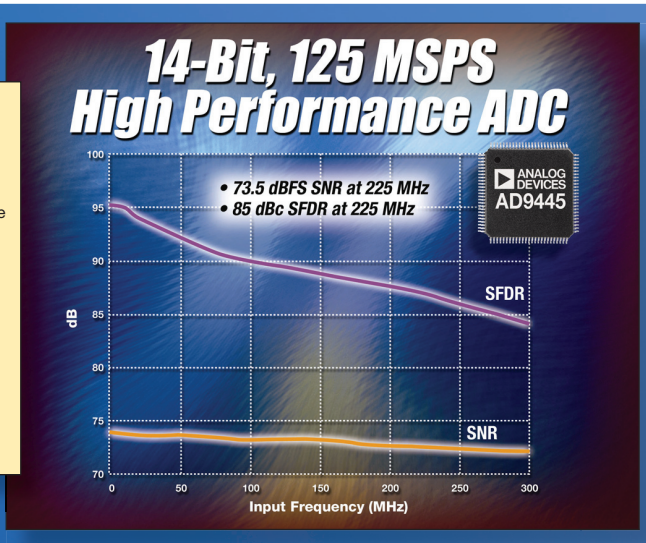


Figure 2. The AD9445 is the first 14-bit, 125 Msps ADC to achieve a SFDR above 80 dBc and an SNR of 72.5 dBfs at input frequencies up to 300 MHz.

non-linearity (INL) of ±3 LSB. Like other members of this family of high-speed ADCs, the new AD9446 features parallel low-voltage differential signaling (LVDS) outputs, including an output clock, which simplifies the interface to digital processing components and reduces the potential for digital noise coupling back into the ADC core (Figure 1). It requires 3.3 V and 5 V for operation. Typical power dissipation is 2.5 W at 100 Msps conversion speed.

Unparalleled performance

According to ADI, the AD9445 is the first 14-bit, 125 Msps ADC to achieve an SFDR above 80 dBc and an SNR of 72.5 dBfs at input frequencies up to 300 MHz, better than competing solutions by a full 10 dB and 4 dB, respectively (Figure 2). A converter with high SFDR can capture weak signals in the frequency band of interest, despite the presence of strong, interfering signals. The industry-leading SNR characteristics of the AD9445 enable wireless infrastructure equipment designers to improve cellular base station receivers by offering lower overall system noise at higher intermediate frequencies, which translates to expanded cellular coverage and fewer dropped calls. Furthermore, the combination of high input frequency and high sampling rate eliminates a frequency downconversion step before the ADC, thereby easing the analog filtering burden. Both of these elements offer significant cost savings to the wireless system designer, said the supplier.

"The 14-bit AD9445 offers unparalleled SFDR and aperture jitter to expand the dynamic range of wireless base station receivers, while improving quality of service and lowering component count and cost," said Ahmed M A. Ali, senior design engineer with ADI's high-speed converter group. The AD9445 also achieves an aperture jitter of 60 fs compared to the 250 fs to 300 fs aperture jitter of competing ADCs, which is critical to maintaining SNR at high input frequencies. Aperture jitter is the sample-to-sample variation in aperture delay and a major contributor to overall system signal degradation.

In addition to delivering greater than 80 dBc SFDR at a 300 MHz input frequency and 85 dBc SFDR at 225 MHz, the AD9445 provides high DC accuracy, with typical differential non-linearity (DNL) of ±0.2LSB and integral non-linearity (INL) of ±1.0 LSB. The ADC also features a flexible input range up to 3.2 Vp-p, allowing the user to achieve SNR performance as high as 78 dBfs, a full 6 dB better than any ADC of this class, while maintaining the state-of-the-art SFDR and IF sampling performance. The AD9445 also has an on-chip reference and track-and-hold, and parallel LVDS outputs to ease the interface to digital downconverters. The high-speed 14-bit ADC uses 3.3 V and 5 V supplies for operation. It offers 2.2 W (typical) power dissipation at maximum sampling speed.

The 14-bit AD9445 and 16-bit AD9446 are sampling with production slated for the end of the third quarter. Both the new high-performance ADCs come in Pb-free 100-lead TQFP/EP (thin quad flat pack/exposed paddle) packages. Pricing for the AD9445-125 and AD9445-105 is $59.50 and $49.30, respectively, in 1000-unit quantities. In similar quantities, the AD9446-100 and AD9446-80 are priced at $79.90 and $72.25 each. The devices are supported by two evaluation boards and a behavioral model that can be used with Analog Devices' ADIsimADC modeling software.

Analog Devices Inc.
804 Woburn St.
Wilmington, MA 01887
(800) 262-5643
www.analog.com

Replace four A/D converters with one tiny A/D converter

By Bettyann Liotta, eeProductCenter
Jun 15 2005 (12:07 PM)
URL: http://www.eeproductcenter.com/showArticle.jhtml?articleID=164303377

Milpitas, Calif. — Linear Technology Corp. is expanding its low-power, high-speed analog-to-digital converter offering with six new devices.

The showstopper of the group, which is aimed at cellular basestations, is a 125 Msamples/s, 14-bit converter (LTC2255) that boasts strong AC performance and extremely low power.

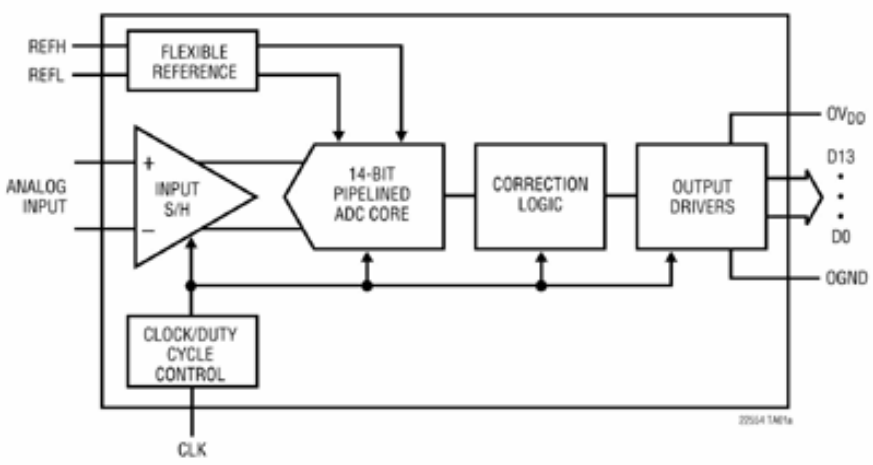
Outperforming its nearest 14-bit competitor, the A/D converter consumes 49 percent less power at just 395 mW, significantly lowering the power budget and thermal considerations required for multiple channel devices, said Todd Nelson, product marketing manager of Linear Technology's mixed-signal products. "This provides a significant advantage in applications where efficiency and cooling is critical, such as satellite receivers, wireless basestations and portable electronics," he said.

The A/D converter comes in a 5mm x 5mm QFN package with integrated bypass capacitors — requiring only a small number of tiny external components. The device eliminates the need for large and costly decoupling capacitors, affording the smallest solution size available, which eases printed-circuit board space constraints and allows for more compact, cost effective designs. "With its small dimensions, low power and reduced external component requirement, designers can easily fit four of these A/D converters where just one competing solution would fit," Nelson said.

The LTC2255 is aimed at 3G and emerging 4G technologies, Worldwide Interoperability for Microwave Access, Inc. (WiMAX) and other wideband wireless applications. In addition, the combination of high sampling rate, low-current and 14-bit resolution make it suited to battery powered, high performance test and instrumentation equipment.

The A/D converter offers exceptional low-level input signal performance due to its high linearity, and it is designed with good margin relative to the sample rate for reliable performance over a wide temperature range. At 125 Msamples/s sampling rate, it achieves excellent AC performance with 72.1dB signal-to-noise ratio (SNR) and 85dB spurious-free dynamic range (SFDR) at 70 MHz.

The LTC2255 is one of six new A/D converters that fall within Linear Technology's pin- compatible family of low-power, high-speed A/D converters — with higher sampling rates of 105 Msamples/s and 125 Msamples/s in resolutions of 10-, 12- and 14-bits. Each device is available in both commercial and industrial temperature grades.

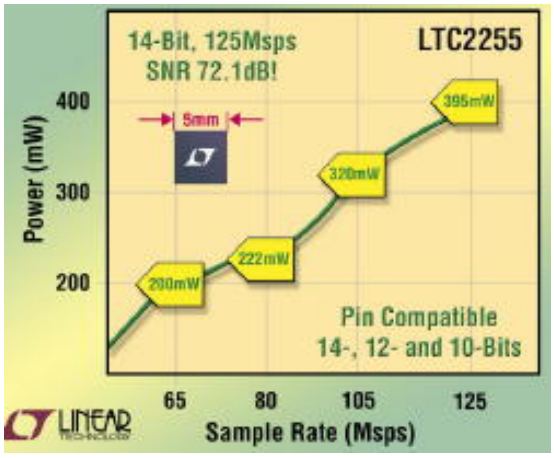


Pricing is $49.00 for the LTC2255 (14-bit, 125 Msamples/s), $41.00 for the LTC2254 (14-bit, 105 Msamples/s), $27.50 for the LTC2253 (12-bit, 125 Msamples/s), $23.00 for the LTC2252 (12-bit, 105 Msamples/s), $12.00 for the LTC2251 (10-bit, 125 Msamples/s), and $7.50 for the LTC2250 (10-bit, 105 Msamples). Click here for the LTC2255/LTC2254 data sheets. Click here for the LTC2253/LTC2252 data sheets. Click here for the LTC2250/LTC2251 data sheets.

Linear Technology, 1-800-454-6327, www.Linear.com.

Linear Technology's new A/D converter family is similar to its older dual 14-bit A/D converter family (see *Related Stories* link below), which came out in January. "These parts offer solid performance, smaller size and lower power. The customer isn't giving up anything. We're just extending these features to A/D converters that operate at faster rates," Nelson said.

Of the six new A/D converters, the company is most proud of its LTC2255 device. This one offers the highest resolution (14-bit) and fastest speed (125 Msamples/s) of the lot.



Most designers look at AC performance and power consumption when considering an A/D converter, Nelson said. Generally, one spec is more important than the other, depending on the application. While there may be competing devices with stronger AC performance, Nelson believes the LTC2255 offers the lowest power (about half of competing devices). "You may find similar A/D converters with very good dynamic range, but at just under 400 mW, our part will be the preferred choice," he said.

Basestations are the biggest market for converters at this speed and resolution. "The power level and size (5mm x 5mm) of the LTC2255 offers a win/win solution for basestation designers," Nelson said.

Cellular basestation units are getting smaller so designers need to pack more channels into a tighter space. Doing this generates additional heat and there is no room for airflow and heat sinks around the parts, which is why smaller parts that produce less heat are very enticing to basestation makers right now, Nelson said. Also, power supplies in the same unit have to be sized smaller so the power consumption of each product must be lower, he said.

In response to size constraints, Linear Technology integrated a lot of the capacitance necessary for supply and reference bypassing. "In addition, the internal reference is designed so it needs less capacitance as well," Nelson said.

Adding capacitance takes up a lot of unnecessary space, which Linear Tech has minimized. "We're probably being conservative when we say that you can replace four A/D converters with one of ours," Nelson added.

Last month, Analog Devices Inc. (Norwood, Mass.) unveiled a similar device. Linear Tech's new A/D converters are available now in volume. ADI's A/D converters won't be available in production quantities until September.

ADI's AD9445 is optimized to capture weak signals in noisy environments while simplifying basestation receiver designs. It provides SFDR above 80 dBc and a SNR of 72.5 dBfs at input frequencies up to 300 MHz.

Click here to read more about ADI's AD9445 A/D converter.

Texas Instruments Inc. (Dallas) appears have been the first company on the scene with a 14-bit, 125 Msamples/s A/D converter in 2003! TI's ADS5500, with total power dissipation of 750 mW, featured 70-dB SNR and 82-dB SFDR at 100-MHz input frequency.

Click here to read more about TI's ADS5500 A/D converter.

Smoking 16-bit A/D converter delivers high SFDR

By Bettyann Liotta, eeProductCenter
Sep 6 2005 (9:00 AM)
URL: http://www.eeproductcenter.com/showArticle.jhtml?articleID=170101853

Milpitas, Calif. — Linear Technology Corp. announced what it claims is the fastest 16-bit (130 Msamples/second) analog-to-digital converter on the market for the most demanding wideband, low noise, signal acquisition applications.

The LTC2208 A/D converter addresses the key requirements for maximizing performance of high sensitivity receivers and data acquisition systems. The device's exceptional spurious free dynamic range (SFDR) performance of 100 dBc, combined with 78 dB signal-to-noise ratio (SNR), enable it to resolve low level signals in the presence of large interferers and blockers, said Todd Nelson, product marketing manager of LTC's mixed-signal products.

The LTC2208 incorporates two unique features that simplify receiver design and improve system performance. The first is an internal transparent dither circuit that improves the A/D converter's SFDR response well beyond 100 dBc for low level input signals. The second feature is a digital output randomizer that dramatically reduces unwanted tones caused by digital feedback. The flexible digital outputs can be run as CMOS or low-voltage differential signaling (LVDS).

The LT2208 also features a programmable gain amplifier (PGA) front end that eases the A/D converter driver output power requirements when driving the lower input range of 1.5-V peak to peak. This improves the distortion performance and power consumption of the driver with minimal impact on A/D converter noise performance, Nelson said.

The LTC2208 packages an extensive feature set in a 9mm x 9mm QFN package delivering low power consumption at 1250 mW without the need for heat sinking. Most importantly, both the power consumption and total solution size with integrated bypass capacitance are less than half that of the nearest competitor, according to Nelson.

Designed for ease of use, it requires only a single 3.3-V supply for operation and comes with a clock duty cycle stabilizer for maintaining the A/D converter performance over varying duty cycles. The LTC2208 can accept high frequency, wide dynamic range signals, offering a wide analog input bandwidth of 700 MHz.

The LTC2208 family includes speed grades of 130-, 105-, 80-, 65-, 40-, 25- and 10- Msamples/s. In addition to the 16-bit parts, 14-bit versions will also be available before the end of the year. All devices are supported with demo boards.

 See related art

The LTC2208 is available today in production quantities in both commercial and industrial temperature grades and is priced at $65 each in 1,000-piece quantities. Click here for the LTC2208 data sheet.

Linear Technology, 1-800-454-6327, www.Linear.com.

A few months ago, LTC introduced the LTC2255 family, which included a low power (395 mW), 14-bit, 120 Msamples/s device. LTC focused on low power when it developed this family. Even though the company concentrated on performance this time around, it was still able to deliver very low power products. Typically, lower power translates to less performance, but that isn't the case with this family.

To date, the new pin-compatible family consists of 11 devices with different speed grade options. The LTC2208 has both LVDS and CMOS outputs. The others have CMOS outputs.

The LTC2255 family currently tops out at 130 Msamples/s (LTC2208), and goes all the way down to 10 Msamples/s. Naturally, lower speeds tout reduced power consumption. Power consumption on the LTC2208 is 1.25 W, compared to 150 mW for the slowest 10 Msamples/s device.

However, there are similar competing devices, with the same sampling rate, with significantly higher power consumption, Nelson said. "Another competing 16-bit A/D converter, for instance, operates at 80 Msamples/s with 2.5-W power consumption, compared to our 80 Msamples/s part, with 650 mW power consumption."

Nelson attributes some of the low power to the CMOS process — but most of it is due to the device's design, he said.

LTC has included special features in the family that can either reduce or eliminate noise and distortion, which is especially crucial at the 16-bit level. "We believe adding dither and output randomizer functions to a monolithic A/D converter has never been done before. While these features aren't new, they have been implemented by our customers previously — external to the AD converter," Nelson said.

Dither introduces pseudo random noise into the conversion process and spreads the point where it's converted to different locations around the transfer function. "Therefore you spend less time where the non-linearity occurs. This has been a real challenge for our customers to do themselves in the past," Nelson said.

No one else provides output randomizing, according to Nelson. "The randomizer takes the least significant bit (LSB) and encodes it with other outputs so there is less opportunity for all the bits to switch at once, thereby generating less noise," he said.

LTC has also seen its customers focus on noise due to digital outputs. When you are clocking output at 130 MHz, there are several techniques that can be used to minimize feedback of the digital switching noise back to the converter, Nelson said. "We already have a very low digital output swing — down to as low as half a volt and we offer LVDS outputs, because this is a parallel output bus, not a single, serial port," he said.

 See related functional block diagram