Micro Linear

ML2037

500kHz, Serial Input, Programmable Sine Wave Generator with Digital Gain Control

GENERAL DESCRIPTION

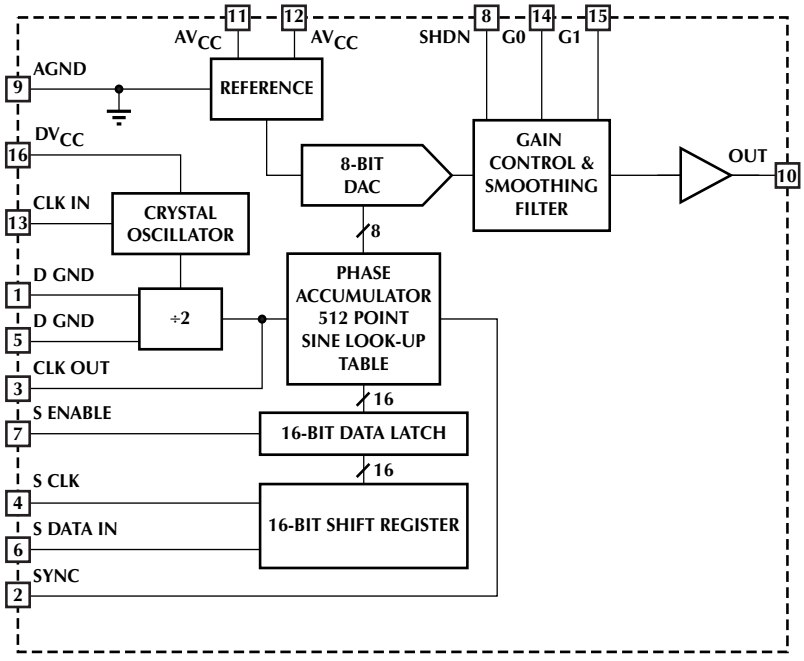
The ML2037 is a precision programmable sine wave generator with a frequency range of DC to 500kHz. The device is capable of generating a wide frequency range of low distortion sine waves with no external passive components. The frequency of the sine wave output is programmed by a 16-bit word that is loaded through a serial input. The sine wave output frequency is determined by the programmed value and the clock frequency. The clock frequency is derived from either an external crystal connected to the device or an external clock input to provide a stable and accurate frequency reference.

The sine wave output of the ML2037 is filtered and has a programmable amplitude that is digitally programmed in 0.5V steps. The maximum amplitude is $2.0V_{P-P}$ centered at a 2.5V level. The device functions from a single 5V power supply and has a shutdown pin to put the device into a low power mode that disables the output. A sync input is provided to allow the synchronization of more than one device in a system.

FEATURES

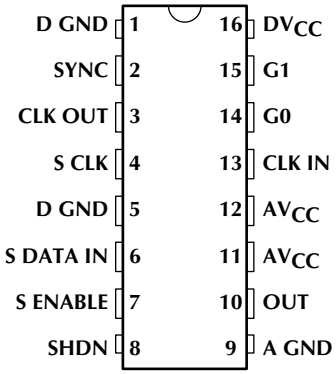
- Programmable output frequency:
  DC to 400kHz—using a crystal
  DC to 500kHz—using an external digital clock
- 3-wire SPI compatible serial interface with double buffered latch for programming the frequency
- Digital gain control for programming output amplitude
- SYNC input for synchronization of multiple sine waves
- Shutdown pin for sleep mode
- Single 5V power supply operation

BLOCK DIAGRAM



PIN CONFIGURATION

ML2037
16-Pin PDIP (P16)
16-Pin Wide SOIC (S16W)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 5	D GND	Ground connection for the digital sections of the IC.
2	SYNC	Synchronization input. Holding this pin low stops the sine wave output, and resets the phase to zero.
3	CLK OUT	Output of the internal high frequency clock generator. $f_{CLK\ OUT} = ½f_{CLK\ IN}$.
4	S CLK	Serial data clock input. Serial data is clocked into the shift register on falling edges of S CLK.
6	S DATA IN	Serial data input for programming the output frequency.
7	S ENABLE	Serial interface enable control. A logic high on this pin allows data to be entered into the latch.
8	SHDN	A logic high on this pin causes the output of the generator to shut off and places the IC in a low power standby mode.
9	A GND	Ground reference for analog sections of the IC and reference for OUT.
10	OUT	Sine wave output. The amplitude of the sine wave will vary around a 2.5V DC level.
11,12	AV_{CC}	Power supply for the analog sections of the IC.
13	CLK IN	Input of the internal high frequency clock generator. This pin is either driven from an external clock input or connected to a crystal for use with the internal oscillator.
14	G0	Output gain control. Works with G1 to set the output amplitude to one of four different full scale ranges.
15	G1	Output gain control. Works with G0 to set the output amplitude to one of four different full scale ranges.
16	DV_{CC}	Power supply for the digital sections of the IC.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

AV_{CC}, DV_{CC} 7V
Voltage on any other pin .... AGND - 0.3V to AV_{CC} + 0.3V
Input Current ..... ±25mA
Junction Temperature 150ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA})
Plastic DIP 80ºC/W
SOIC 105ºC/W

OPERATING CONDITIONS

Temperature Range
ML2037CX ..... 0ºC to 70ºC
ML2037IX ..... -40ºC to 85ºC
AV_{CC}, DV_{CC} Range ..... 4.75V to 5.25V

ELECTRICAL CHARACTERISTICS

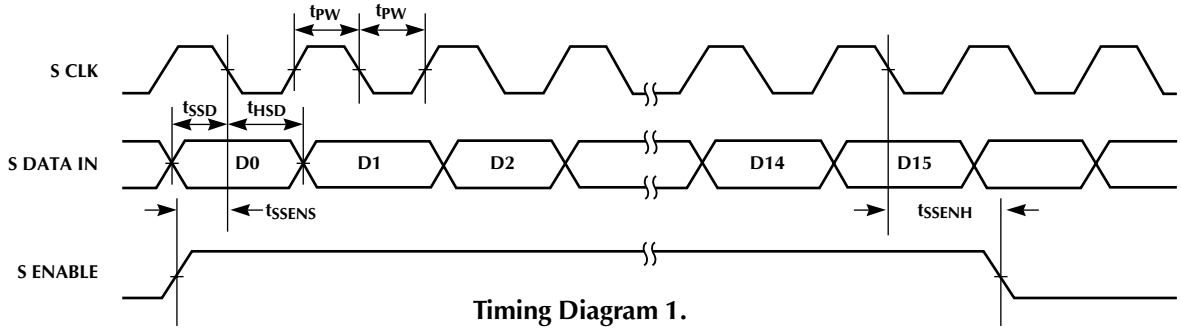
Unless otherwise specified, AV_{CC} = DV_{CC} = 4.75V to 5.25V, SHDN = 0V, CLK IN = 25.6MHz (crystal) or 32MHz (external clock), C_L = 50pF, R_L = 1kΩ, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT							
HD	Harmonic Distortion	20Hz to 31.25kHz				-45	dB
	(2nd and 3rd Harmonic)	31.25kHz to 500kHz				-40	dB
SND	Signal to Noise + Distortion	1kHz to 31.25kHz, f_{OUT} BW < 31.25kHz				-45	dB
		31.35kHz to 500kHz, f_{OUT} BW < 500kHz				-40	dB
	Gain Error	f_{OUT}<125kHz, AV_{CC} = 5V, G1=1, G0=1	C Suffix			±0.15	dB
		f_{OUT}<125kHz, AV_{CC} = 5V, G1=1, G0=1	I Suffix			±0.25	dB
		125kHz<f_{OUT}<500kHz, AV_{CC} = 5V, G1=1, G0=1	Both			±0.5	dB
	Idle Noise	SHDN = 5V			500		μV_{rms}
PSRR	Power Supply Rejection Ratio	200mV_{P-P}, f_{OUT} = 0 - 100kHz			-40		dB
	DC Output Voltage			2.4		2.6	V
	Peak-to-Peak Output Voltage	G1 = 0, G0 = 0			0.5		V_{P-P}
		G1 = 0, G0 = 1			1.0		V_{P-P}
		G1 = 1, G0 = 0			1.5		V_{P-P}
		G1 = 1, G0 = 1		1.88	2.0	2.12	V_{P-P}
OSCILLATOR							
	CLK IN Input Low Voltage					1.5	V
	CLK IN Input High Voltage			3.5			V
	CLK IN Input Low Current	External Clock		-250			µA
	CLK IN Input High Current	External Clock				250	µA
	CLK IN Input Capacitance				12		pF
	CLK IN Maximum Frequency	External Clock		32			MHz
	CLK OUT to CLK IN Frequency Ratio			0.49	0.5	0.51	

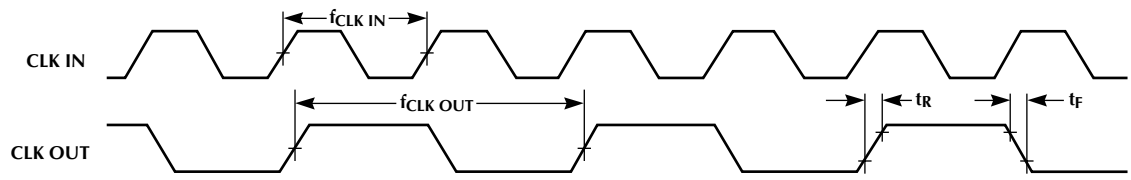
ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (Continued)						
t_R	CLK OUT Rise Time	C_L = 25pF, See Timing Diagram 2			8	ns
t_F	CLK OUT Fall Time	C_L = 25pF, See Timing Diagram 2			8	ns
LOGIC						
V_{IL}	Input Low Voltage				1.0	V
V_{IH}	Input High Voltage		DV_{CC} - 1			V
I_{IL}	Input Low Current		-1			µA
I_{IH}	Input High Current				1	µA
V_{OL}	Output Low Voltage	I_{OL} = -2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	4.0			V
$f_{S\ CLK}$	Serial Clock Frequency		0.01		10	MHz
t_{PW}	Serial CLock Pulse Width		40			ns
t_{SSD}	S DATA IN Setup Time		10			ns
t_{HSD}	S DATA IN Hold Time		10			ns
t_{SSENS}	S ENABLE Setup Time		30			ns
t_{SSENH}	S ENABLE Hold Time		50			ns
t_{DSEN}	Delay from S ENABLE to Stable Output	$f_{CLK\ IN}$ = 32MHz		500		ns
t_{DSYNC}	Delay from SYNC to Output Start	$f_{CLK\ IN}$ = 32MHz		500		ns
SUPPLY						
AI_{CC}	AV_{CC} Current	$f_{CLK\ IN}$ = 16MHz		35	45	mA
		$f_{CLK\ IN}$ = 32MHz		40	50	mA
		SHDN = 5V			10	µA
DI_{CC}	DV_{CC} Current	$f_{CLK\ IN}$ = 16MHz		10	14	mA
		$f_{CLK\ IN}$ = 32MHz		16	20	mA
		SHDN = 5V			30	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.



Timing Diagram 1.



Timing Diagram 2.

FUNCTIONAL DESCRIPTION

The ML2037 is composed of a programmable frequency generator, a sine wave generator, a crystal oscillator, and a digital interface. The functional block diagram is shown in Figure 1.

PROGRAMMABLE FREQUENCY GENERATOR

The programmable frequency generator produces a digital output whose frequency is determined by a 16-bit digital word.

The frequency generator is composed of a phase accumulator which is clocked at $\frac{1}{2}f_{CLK\ IN}$. The value stored in the data latch is added to the phase accumulator every two cycles of CLK IN. The frequency of the analog output is equal to the rate at which the accumulator overflows and is given by the following equation:

$$f_{OUT} = \frac{f_{CLKIN} \times (D15 \rightarrow D0)_{DEC}}{2^{22}} \quad (1)$$

Where (D15–D0) is the decimal value of the programming word.

The frequency resolution and the minimum frequency are the same and can be calculated using:

$$\Delta f_{MIN} = \frac{f_{CLKIN}}{2^{22}} \quad (2)$$

When $f_{CLK\ IN}$ = 25MHz, Δf_{MIN} = 5.96Hz (±2.98Hz). Lower output frequencies are obtained by using a lower clock frequency.

The maximum frequency output can be easily calculated with the following equation:

$$f_{OUT(MAX)} = \frac{f_{CLKIN}}{2^{6}} \quad (3)$$

When $f_{CLK\ IN}$ = 25MHz, $f_{OUT(MAX)}$ = 391kHz. Higher frequencies, up to 500kHz, are obtained by using an external clock, where 25MHz < $f_{CLK\ IN}$ < 32MHz.

Due to the phase quantization nature of the frequency generator, spurious tones can be present in the output in the range of –50dB relative to fundamental. The energy from these tones is included in the signal to noise + distortion specification (SND) given in the electrical table. The frequency of these tones can be very close to the fundamental, and it is not practical to filter them out.

SINEWAVE GENERATOR

The sinewave generator is composed of a sine lookup table, an 8-bit DAC, an output smoothing filter, and an amplifier. The sine lookup table is addressed by the phase accumulator. The DAC is driven by the output of the table and generates a staircase representation of a sine wave.

The output filter smooths the analog output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with the second and third harmonic distortion components at least 40dB below the fundamental.

The ML2037 has a 2-bit (G1, G0) digital gain control. With the gain input equal to logic 00, the sine wave amplitude is equal to $0.5V_{P-P}$. Incrementing the gain control input increases the output amplitude in 0.5V steps to a maximum of $2.0V_{P-P}$. The output amplitude is accurate to within ±0.5dB over the frequency range.

G1	G0	P–P OUTPUT AMPLITUDE
0	0	.5V
0	1	1.0V
1	0	1.5V
1	1	2.0V

The analog section is designed to operate over a frequency range of DC to 500kHz and is capable of driving 1kΩ, 50pF loads at the maximum amplitude of $2.0V_{P-P}$. The sine wave output is typically centered about a 2.5V DC level, so for a $2V_{P-P}$ sine wave, the output will swing from 1.5V to 3.5V.

CRYSTAL OSCILLATOR

The crystal oscillator generates an accurate reference clock for the programmable frequency generator. The internal clock can be generated with a crystal or external clock.

If a crystal is used, it must be placed between CLK IN and DGND. An on-chip oscillator will then generate the internal clock. No other external components are required. The crystal should be a parallel resonant type with a frequency between 5MHz to 25.6MHz. It should be placed physically as close as possible to CLK IN and DGND, to minimize trace lengths.

The crystal must have the following characteristics:

- Parallel resonant type
- Frequency: 5MHz to 25.6MHz
- Maximum ESR: 120Ω @ 5 to 10MHz, 80Ω @10 to 15MHz, and 50Ω @ 15 to 25.6MHz
- Drive level: 500µW
- Typical load capacitance: 18 - 20pF
- Maximum case capacitance: 7pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. In general,

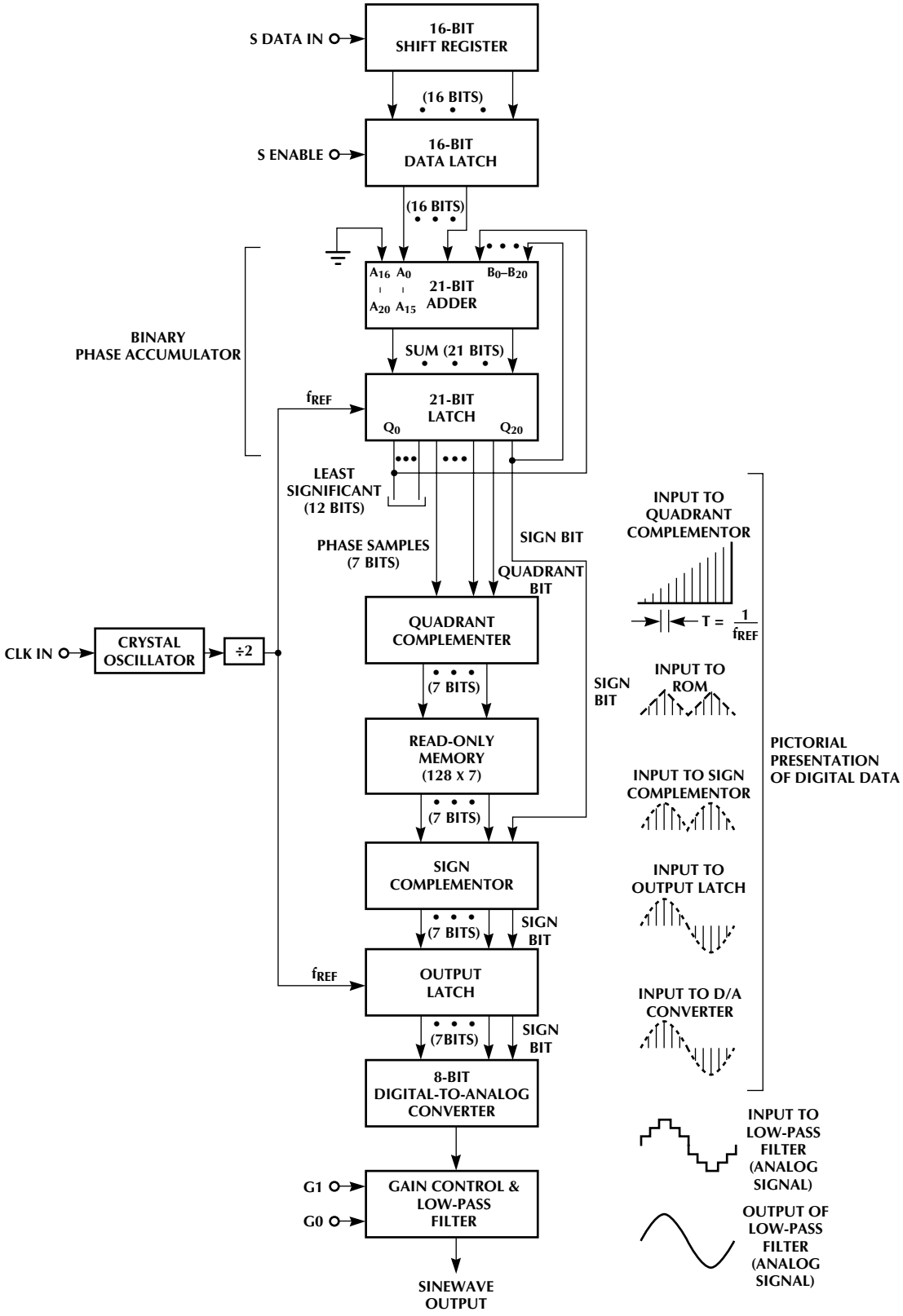


Figure 1. Detailed Block Diagram of the ML2037.

FUNCTIONAL DESCRIPTION (Continued)

microprocessor crystals meet the above requirements, but it is recommended to test the selected crystal in circuit to insure proper operation. Suitable crystals can be purchased from the following suppliers:

ECS, Inc.
FOX Electronics
M-TRON Industries

An external clock can drive CLK IN directly if desired. The frequency of this clock can be anything from 0 to 32MHz. However, at clock frequencies below 5MHz, the sine wave output begins to exhibit "staircasing".

The ML2037 has a clock output that can be used to drive other external devices. The CLK OUT output is a buffered output from the oscillator which runs at one half the frequency of CLK IN.

SERIAL DIGITAL INTERFACE

The digital interface consists of a shift register and data latch. The serial 16-bit data word on S DATA IN is clocked into a 16-bit shift register on falling edges of the serial shift clock, S CLK. The LSB should be shifted in first and the MSB last as shown in Timing Diagram 1. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the falling edge of S ENABLE. To insure that true data is loaded into the data latch from the shift register, the S ENABLE falling edge should occur before the S CLK transitions high to low. S ENABLE should be high while shifting data into the shift register. Note that all data is entered and latched on edges, not levels, of S CLK and S ENABLE.

Upon power up, the data in the latch is indeterminate. It is therefore recommended to initialize the frequency data as part of a power up routine.

SYNCHRONIZATION

When the SYNC pin is held high, the sine wave generator operates normally. Pulling this pin low causes the sine wave output to be interrupted and resets the phase back to zero. The sine wave output goes to the 2.5V DC level approximately 1µs after the SYNC input goes low. Switching the SYNC pin back to a high level starts the sine wave going again from zero phase. The delay from when the SYNC goes high to the start of the sine wave is about 500ns, as shown in Figure 2. If several generator chips are driven from the same clock, the SYNC input allows them to be phase synchronized to any value. Figure 3 gives an example of how a microcontroller can be used with two ML2037s to generate two sine waves that are 90º out of phase.

SHUTDOWN

The SHDN input provides a means to power down the analog section and the internal clock of the sine wave generator. When in the power down mode the part will draw only 10µA of input current and the output will go to zero approximately 500ns after the SHDN pin goes high. Switching the SHDN back to a low level allows the sine wave to resume at the last programmed frequency. The delay from when the SHDN goes low to when the sine wave resumes is about 200µs. The use of the power down mode allows power management for portable applications or for gating the internal oscillator for low noise applications.

POWER SUPPLIES

The analog circuitry in the device is powered from 5V (AV_{CC}) and is referenced to AGND. The digital circuits in the device can also powered from the same 5V supply (DV_{CC} to DGND). It is recommended that AGND and DGND be connected together close to the device and have a good connection back to the power source.

It is recommended that the power supplies to the device should be bypassed by placing decoupling capacitors from AV_{CC} to AGND and DV_{CC} to DGND as physically close to the device as possible.

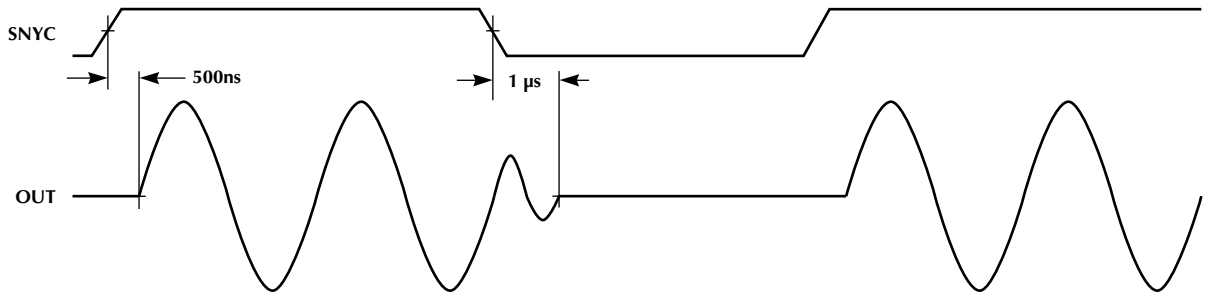


Figure 2. SYNC Pin Timing.

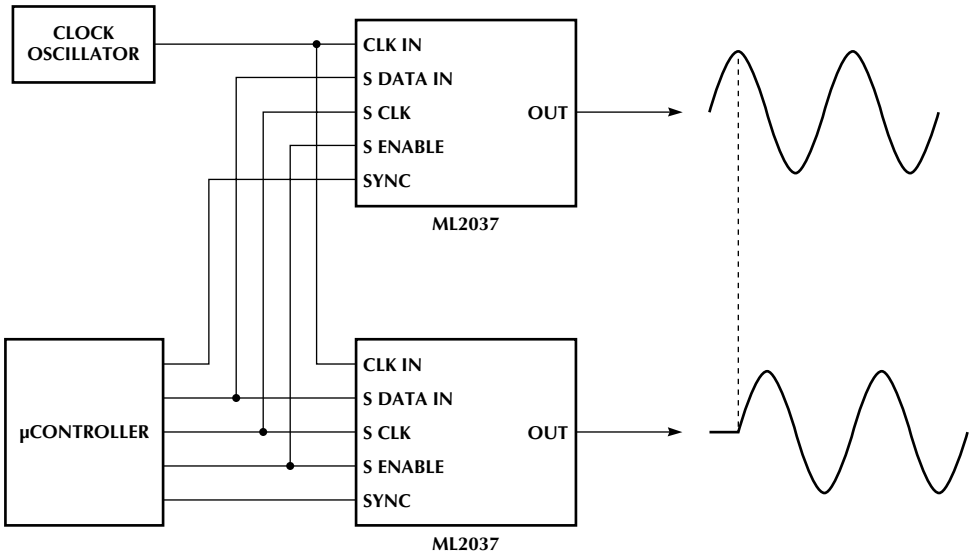
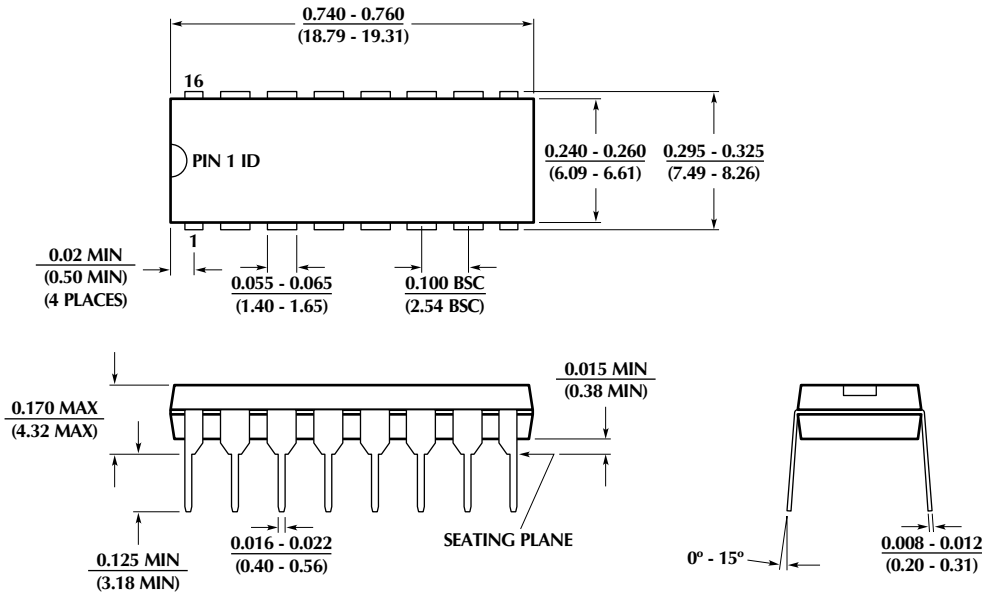


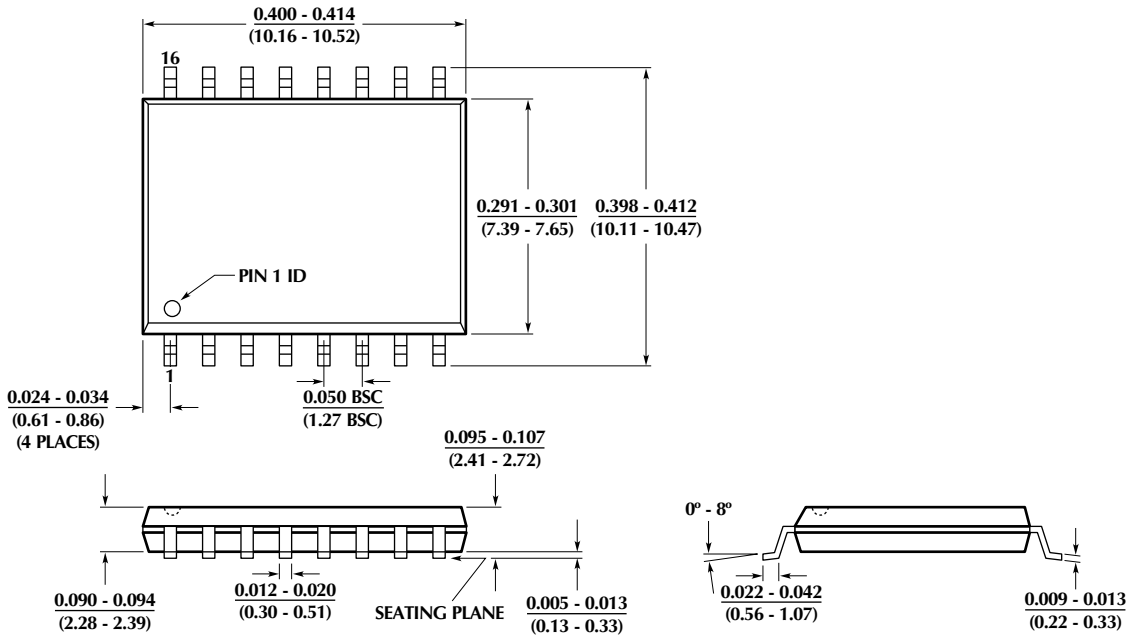
Figure 3. Synchronizing Two ML2037 Sine Wave Generators.

PHYSICAL DIMENSIONS inches (millimeters)

Package: P16
16-Pin PDIP



Package: S16W
16-Pin Wide SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2037CP	0°C to 70°C	16-Pin PDIP (P16)
ML2037CS	0°C to 70°C	16-Pin Wide SOIC (S16W)
ML2037IP	-40°C to 85°C	16-Pin PDIP (P16)
ML2037IS	-40°C to 85°C	16-Pin Wide SOIC (S16W)

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Micro Linear

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