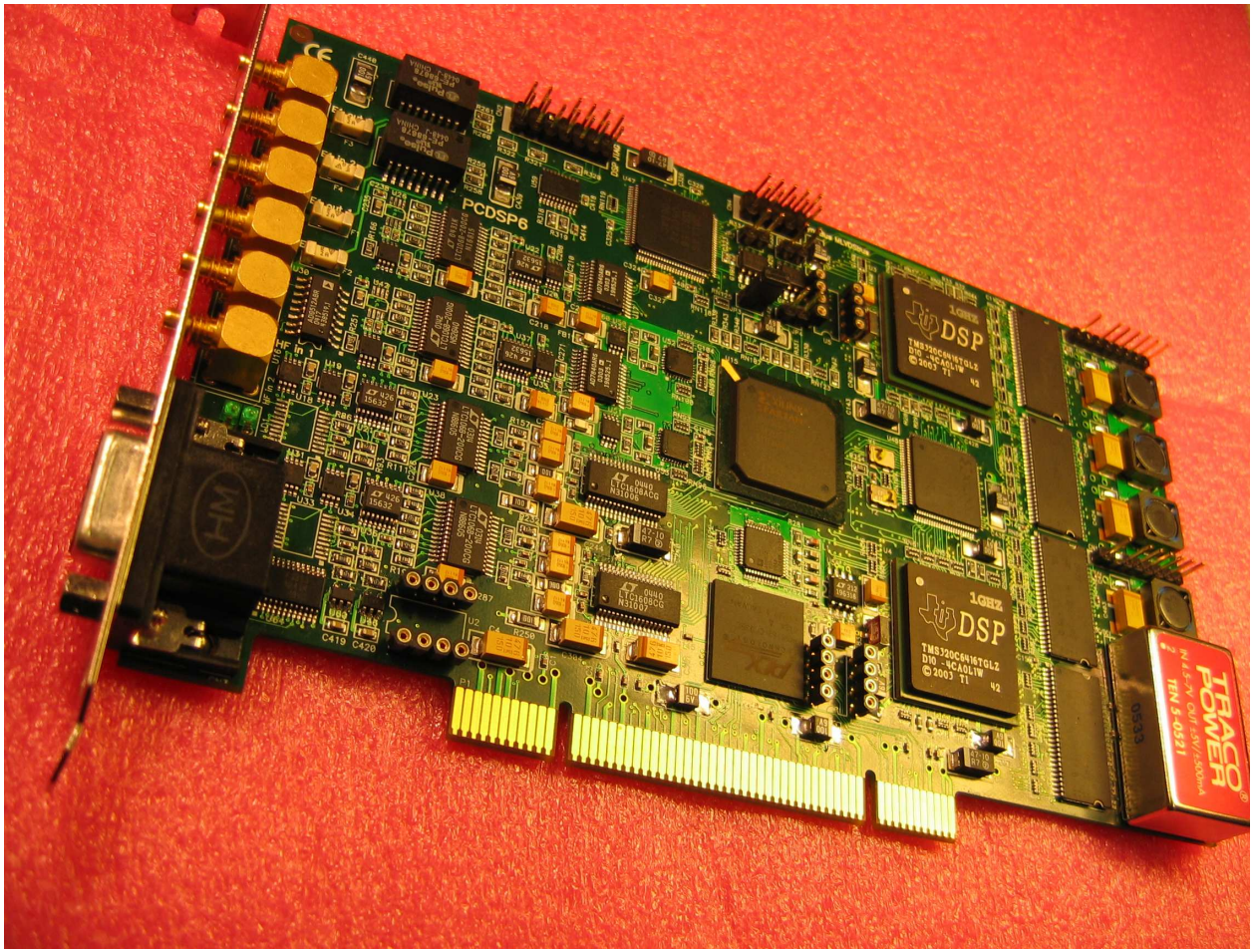
PCDSP6 DSP kártya - 2005

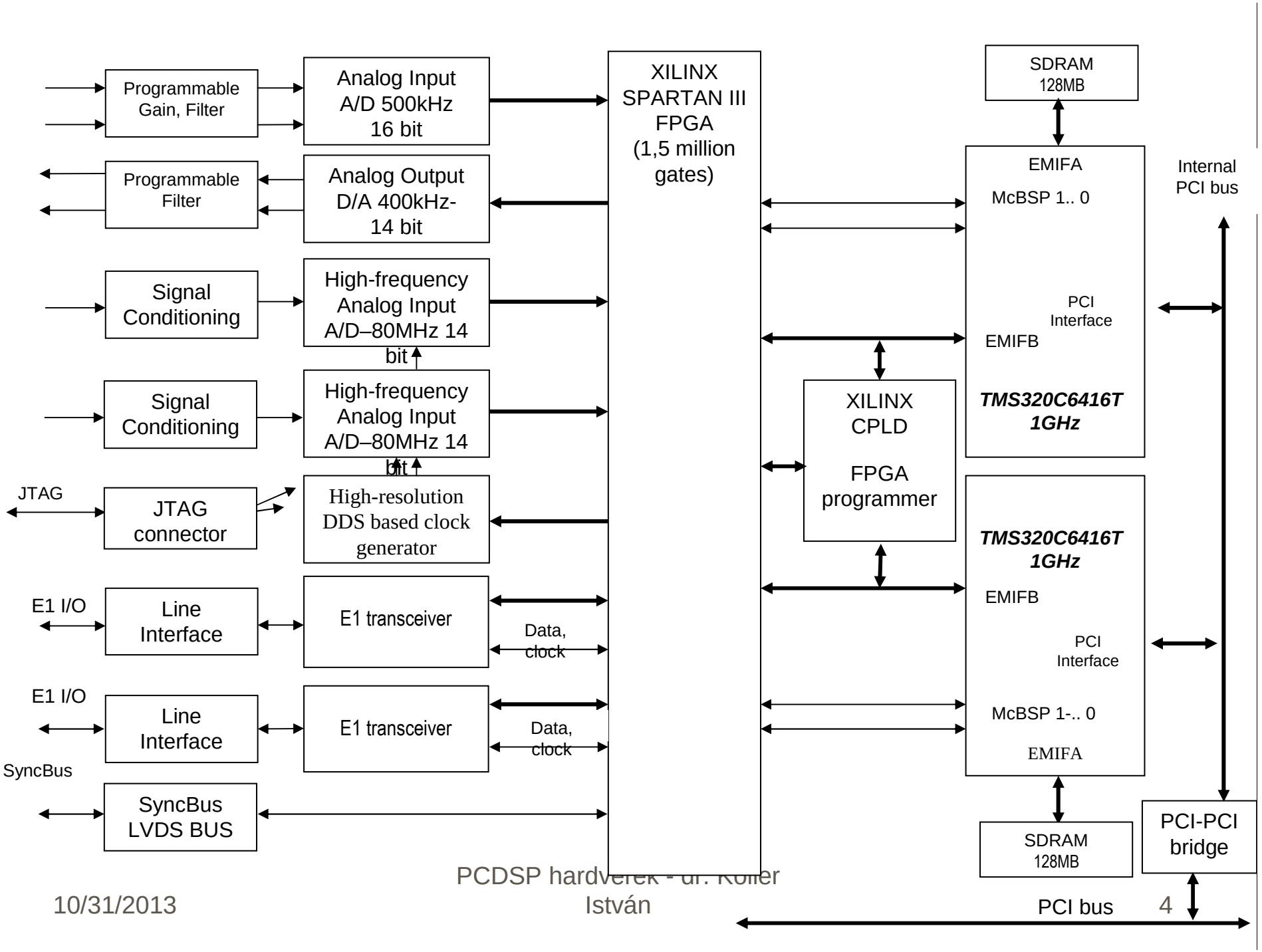
- PCI buszos PC interfész, 3/5V 32bit 132MB/s
- 2 TMS320C6416T 90nm **1GHz** DSP
- PCI/PCI bridge
- 1.5 millió kapus XILINX Spartan 3 FPGA
- 2 500kHz - 16bit A/D csatorna szűrőkkel
- 2 400kHz - 14 bit D/A csatorna szűrőkkel
- 2 E1/T1/J1 transceiver
- 2 80MHz - 14 bit A/D

PCDSP6TEL (V7) DSP kártya - 2006

- PCI buszos PC interfész, 3/5V 32bit 132MB/s
- 2 TMS320C6416T 90nm **1GHz** DSP
- PCI/PCI bridge
- 1.5 millió kapus XILINX Spartan 3 FPGA
- 16 E1/T1/J1 transceiver
- 1 E3/DS3 transceiver

PCDSP6 kártya




Programmable Gain, Filter
Analog Input A/D 500kHz 16 bit
Programmable Filter
Analog Output D/A 400kHz- 14 bit
Signal Conditioning
High-frequency Analog Input A/D–80MHz 14 bit
Signal Conditioning
High-frequency Analog Input A/D–80MHz 14 bit
JTAG
JTAG connector
High-resolution DDS based clock generator
E1 I/O
Line Interface
E1 transceiver
Data, clock
E1 I/O
Line Interface
E1 transceiver
Data, clock
SyncBus
SyncBus LVDS BUS
XILINX SPARTAN III FPGA (1,5 million gates)
SDRAM 128MB
EMIFA
McBSP 1.. 0
PCI Interface
EMIFB
TMS320C6416T 1GHz
XILINX CPLD
FPGA programmer
TMS320C6416T 1GHz
EMIFB
PCI Interface
McBSP 1-.. 0
EMIFA
SDRAM 128MB
Internal PCI bus
PCI-PCI bridge
PCI bus

Bekapcsolás után

- Nincs DSP program
- Nincs FPGA tartalom
- DSP-k *PCI boot* állapotban várják a programot
- FPGA lebegteti lábait - várja a konfigurációs adatokat

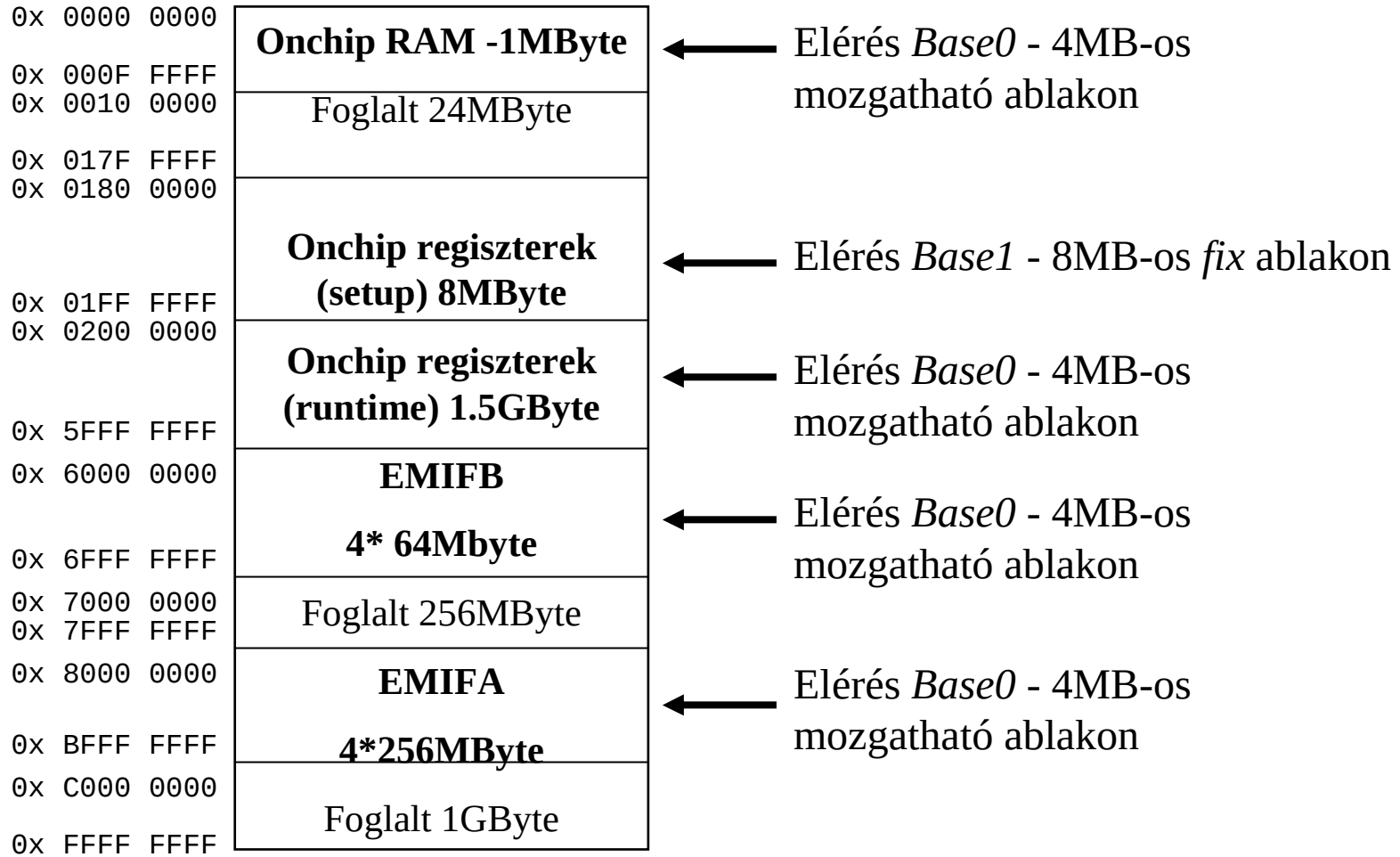
A PCDSP6 címtartományai

- PCI busz felől
  - Base0 - 4MB gyorsan elérhető, memória elérésre
  - Base1 - 8MB egyszeres PCI ciklusokban elérhető, Onchip regiszterek elérésére
  - Base2 - I/O terület, nem használt

A PCDSP6 címtartományai

- DSP felől
  - Onchip memória
  - Onchip regiszterek
  - External memóriaterületek
    - EMIFA
      - CE0, CE1, CE2, CE3
    - EMIFB
      - CE0, CE1, CE2, CE3

DSP-k memóriatérképe



DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Size (Bytes)	Description of Memory
0000 0000–000F FFFF	DSPP=0, 00 0000–0F FFFF	-	1M	L2 Internal RAM
0010 0000–017F FFFF	-	-	23M	Reserved
0180 0000–0183 FFFF	DSPP=006 00 0000–03 FFFF	00 0000–03 FFFF	256K	External Memory Interface A- EMIFA registers
0184 0000–0187 FFFF	DSPP=006 04 0000–07 FFFF	04 0000–07 FFFF	256K	L2 control registers
0188 0000–018B FFFF	DSPP=006 08 0000–0B FFFF	08 0000–0B FFFF	256K	HPI registers
018C 0000–018F FFFF	DSPP=006 0C 0000–0F FFFF	0C 0000–0F FFFF	256K	McBSP 0 registers
0190 0000–0193 FFFF	DSPP=006 10 0000–13 FFFF	10 0000–13 FFFF	256K	McBSP 1 registers
0194 0000–0197 FFFF	DSPP=006 14 0000–17 FFFF	14 0000–17 FFFF	256K	Timer 0 registers
0198 0000–019B FFFF	DSPP=006 18 0000–1B FFFF	18 0000–1B FFFF	256K	Timer 1 registers
019C 0000–019F FFFF	DSPP=006 1C 0000–1F FFFF	1C 0000–1F FFFF	256K	Interrupt selector registers
01A0 0000–01A3 FFFF	DSPP=006 20 0000–23 FFFF	20 0000–23 FFFF	256K	EDMA RAM and registers

01A4 0000–01A7 FFFF	DSPP=006 24 0000–27 FFFF	24 0000–27 FFFF	256K	McBSP2 registers
01A8 0000–01AB FFFF	DSPP=006 28 0000–2B FFFF	28 0000–2B FFFF	256K	External Memory Interface B EMIFB registers
01AC 0000–01AF FFFF	DSPP=006 2C 0000–2F FFFF	2C 0000–2F FFFF	256K	Timer2 registers
01B0 0000–013F FFFF	DSPP=006 30 0000–33 FFFF	30 0000–33 FFFF	256K	GPIO registers
01B4 0000–01B7 FFFF	DSPP=006 34 0000–37 FFFF	34 0000–37 FFFF	256K	UTOPIA registers
01B8 0000–01BB FFFF	DSPP=006 38 0000–3B FFFF	38 0000–3B FFFF	256K	TCP/VCP registers
01BC 0000–01BF FFFF	DSPP=006 3C 0000–3F FFFF	3C 0000–3F FFFF	256K	Reserved
01C0 0000–01C3 FFFF	DSPP=007 00 0000–03 FFFF	40 0000–43 FFFF	256K	PCI registers
01C4 0000–01FF FFFF	-	-	4M-256K	Reserved
0200 0000–0200 0033	DSPP=008 00 0000–3F FFFF	-	52	QDMA registers
0200 0034–2FFF FFFF	-	-	736M-52	Reserved

3000 0000–33FF FFFF	DSPP=0C0 00 0000–3F FFFF..	-	64M	McBSP0 Data
3400 0000–37FF FFFF	DSPP=0D0 00 0000–3F FFFF ..	-	64M	McBSP1 Data
3800 0000–3BFF FFFF	DSPP=0E0 00 0000–3F FFFF ..	-	64M	McBSP2 Data Not used
3C00 0000–3FFF FFFF	DSPP=0F0 00 0000–3F FFFF ..	-	64M	Utopia queues Not used
4000 0000–4FFF FFFF	-	-	256M	Reserved
5000 0000–5FFF FFFF	DSPP=140 00 0000–3F FFFF ..	-	256M	TCP/VCP

6000 0000–63FF FFFF	DSPP=180 00 0000–00 8FFF	-	64M 32KB is used	External memory interface EMIFB CE0 as 8bit wide asynchronous *CPLD and FPGA implemented control registers* *FPGA programming area*
6400 0000–67FF FFFF	DSPP=190 00 0000–00 1FF	-	64M 512B is used	External memory interface EMIFB CE1 as 8bit wide asynchronous *E1 interfaces*
6800 0000–6BFF FFFF	DSPP=1A0 00 0000–00 FFFF	-	64M 64KB is used	External memory interface - EMIFB CE2 as 16bit wide asynchronous *A/D-D/A*
6C00 0000–6FFF FFFF	DSPP=1B0 00 0000–00 FFFF	-	64M 64KB is used	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D FIFOs* *Two-port memory*
7000 0000–7FFF FFFF	-	-	256M	Reserved
8000 0000–87FF FFFF	DSPP=200.. 21F 00 0000–3F FFFF	-	128M	External memory interface EMIFA CE0 *128MB SDRAM*
8800 0000–8FFF FFFF	-	-	128M	*Not used*
9000 0000–9FFF FFFF	DSPP=240 00 0000–3F FFFF	-	256M	External memory interface EMIFA CE1 *Not used*
A000 0000–AFFF FFFF	DSPP=280 00 0000–3F FFFF	-	256M	External memory interface EMIFA CE2 *Not used*
B000 0000–BFFF FFFF	DSPP=2C0 00 0000–FF FFFF	-	256M	External memory interface EMIFA CE3 *Not used*
C000 0000–FFFF FFFF	-	-	1G	Reserved

EMIFA, EMIFB regiszterek

0180 0000–0183 FFFF	256K	External Memory Interface EMIFA registers for CE0 - SDRAM settings
01A8 0000–01AB FFFF	256K	External Memory Interface EMIFB registers for CE0.. CE3 settings

Memóriába ágyazott eszközök - CPLD regiszterek, EMIFB CE0

Absolute DSP Address (hex)	EMIFB CE0, DSPP= 180 Base0 offset Address Hexa	Decoded function in DSP1/ DSP2 By CPLD/ FPGA	Function
6000 0000	00	DSP1 DSP2 CPLD	DSP identification - read only The 8 LSB bits read value of this register is 0x01 from DSP1, while 0x02 form DSP2.
6000 0001	01	DSP1 CPLD	I2C Data read/write I2C data is a 1bit wide data bus. It can be written/read via LSB bit of data bus. The power-up state of this bit is zero. ☜
6000 0002	02	DSP1 CPLD	I2C Data Bus Drive Enable - read/write Data Bus Drive Enable The I2C data bus driver 0 disabled - I2C device drives the bus ☜ 1 enabled - I2C device is driven by the CPLD
6000 0003	03	DSP1 CPLD	I2C SERCLK - read/write SERCLK is an LSB valuable register. SERCLK is the clock signal of the I2C bus. It can be written/read via LSB bit of this register. The power-up state of this bit is zero. ☜
6000 0004	04	DSP1 DSP2 CPLD	LED switch - read/write The DSP1 can switch the LED1, while DSP2 can switch the LED2. LED switch is an LSB valuable register. LED state LED 0 on ☜ 1 off

Memóriába ágyazott eszközök - CPLD regiszterek, EMIFB CE0

6000 0005	05	DSP1 DSP2 CPLD	Doorbell - read/write Doorbell is an 8-bit wide register (LSB byte), which can be read and written from both DSPs. This register is implemented in the nonvolatile CPLD and is ready to use after power up before FPGA programming. A write cycle of the doorbell register may generate a low to high transition on EXTINT7, generating an interrupt in the other DSP. The written data can be read by the other DSP. See address 6000 0011. The power-up state of this byte is zero. ☜
6000 0006	06	DSP1 CPLD	FPGA PROG_B - read/write FPGA PROG_B is an LSB valuable register, which is used to control the FPGA PROG_B signal. The power-up state of this bit is high. ☜

Memóriába ágyazott eszközök - CPLD regiszterek, EMIFB CE0

6000 0007	07	DSP1 CPLD	FPGA INIT_B - read only FPGA INIT_B is an LSB valuable register, which is used to read the FPGA INIT_B signal.
6000 0008	08	DSP1 CPLD	FPGA CS_B - read/write FPGA CS_B is an LSB valuable, which is used to control the FPGA CS_B signal. The chip select CS_B signal is active low. The power-up state of this bit is one. ☜
6000 0009	09	DSP1 CPLD	FPGA RDWR_B - read/write FPGA RDWR_B is an LSB valuable register, which is used to control the FPGA RDWR_B signal. Low means write. The power-up state of this bit is zero. ☜
6000 000A	0A	DSP1 CPLD	FPGA data port - read/write FPGA data port is an 8-bit register for writing and reading the FPGA configuration memory. The power-up state of this byte is zero. ☜
6000 000B	0B	DSP1 CPLD	FPGA BUSY - read only FPGA BUSY is an LSB valuable register, used to monitor the status of FPGA BUSY signal.
6000 000C	0C	DSP1 CPLD	FPGA DONE - read only FPGA DONE is an LSB valuable register, used to monitor the status of FPGA DONE signal. FPGA DONE goes high, when the configuration is ready.

Memóriába ágyazott eszközök - CPLD regiszterek, EMIFB CE0

6000 000D	0D	DSP1 CPLD	SWAOUT1 - read/write SWAOUT1 is 2 LSB bit valuable register used to control the base-band analog output signal: SWAOUT1 SWAOUT1 00 is driven by BAOUT1☜ 01 is driven. FAOUT1 10 is not driven. 11 is not driven.
6000 000E	0E	-	Not used
6000 000F	0F	DSP1 CPLD	SWAOUT2 - read/write SWAOUT2 is 2 LSB bit valuable register used to control the base-band analog output signal: SWAOUT2 SWAOUT2 00 is driven by BAOUT2☜ 01 is driven. FAOUT2 10 is not driven. 11 is not driven.
6000 0010	10	DSP1 DSP2 CPLD	NMI command - write only Writing a dummy value to this address, an NMI interrupt is generated in the DSP.
6000 0011	11	DSP1 DSP2 CPLD	EXTINT7 Doorbell WRITE register - read/write EXTINT7 Doorbell WRITE register is an LSB bit valuable register used to control the source of EXTINT7 interrupt line driving source: EXTINT7 Doorbell WRITE EXTINT7 source 0 can be driven by CTx_GPINT7☜ 1 is driven by mailbox write See Chapter 16.

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4000	4000	DSP1 FPGA	DA1T1LT2H - read/write DA1T1LT2H is an LSB valuable register, used to assign base-band D/A1 to DSP1 or DSP2. If DA1T1LT2H = 0 the D/A1 is assigned to DSP1☜ If DA1T1LT2H = 1 the D/A1 is assigned to DSP2
6000 4001	4001	DSP1 FPGA	DA2T1LT2H - read/write DA2T1LT2H is an LSB valuable register, used to assign base-band D/A2 to DSP1 or DSP2. If DA2T1LT2H = 0 the D/A2 is assigned to DSP1☜ If DA2T1LT2H = 1 the D/A2 is assigned to DSP2
6000 4002	4002	DSP1 FPGA	F1T1LT2H - read/write F1T1LT2H is an LSB valuable register, used to assign F1 framer to DSP1 or DSP2. If F1T1LT2H = 0 the F1 framer is assigned to DSP1☜ If F1T1LT2H = 1 the F1 framer is assigned to DSP2
6000 4003	4003	DSP1 FPGA	F2T1HT2L - read/write F2T1HT2L read/write F2T1HT2L is an LSB valuable register, used to assign F1 framer to DSP1 or DSP2. If F2T1HT2L = 1 the F2 framer is assigned to DSP1 If F2T1HT2L = 0 the F2 framer is assigned to DSP2☜

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4004	4004	DSP1 FPGA	F1TCLKSEL - read/write F1TCLKSEL is a 4bit (D3, D0) register, used to define F1 framer TCLK source. F1TCLKSEL F1 TCLK 0000 F1RCLK. 0001 Local 2048KHz signal 0010 SYNCBUS0 0011 SYNCBUS1. 0100 SYNCBUS2. 0101 F2RCLK.
6000 4005	4005	DSP1 FPGA	F2TCLKSEL - read/write F2TCLKSEL is a 4bit (D3, D0) register, used to define F2 framer TCLK source. F2TCLKSEL F2 TCLK 0000 F2RCLK. 0001 Local 2048KHz signal 0010 SYNCBUS0 0011 SYNCBUS1. 0100 SYNCBUS2. 0101 F1RCLK.
6000 4006	4006	DSP1 FPGA	DDSSDIO - read/write DDSSDIO is an LSB valuable register, used as a one bit wide serial data bus to control the DDS chip. The power up reset state is zero.
6000 4007	4007	DSP1 FPGA	DDSSDIO_DRVENH - read/write DDSSDIO_DRVENH is an LSB valuable register, used to enable to drive the DDSDIO one bit wide bus by the FPGA. If DDSSDIO_DRVENH = 0 then the DDSDIO is driven by the DDS chip If DDSSDIO_DRVENH = 1 then the DDSDIO is driven by the FPGA with the content of DDSSDIO register

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4008	4008	DSP1 FPGA	DDSCSL - read/write DDSCSL is an LSB valuable register, used to generate the Chip select signal of the DDS chip. The power up reset state is high. ☜
6000 4009	4009	DSP1 FPGA	DDSSCLK - read/write DDSSCLK is an LSB valuable register, used to generate the serial clock signal of the DDS chip. The power up reset state is zero. ☜
6000 400A	400A	DSP1 FPGA	DDSIOUPDATE - read/write DDSIOUPDATE is an LSB valuable register, used to update of the DDS chip. After filling up the DDS registers via the serial port, using the clock and data registers, a low to high transition updates the new values. The power up reset state is zero. ☜
6000 400B	400B	DSP1 FPGA	AD1_FILTDEV - read/write The AD1_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band A/D1 input filter. The Cutoff Frequency = 125000 / (AD1_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ☜
6000 400C	400C	DSP1 FPGA	AD2_FILTDEV - read/write The AD2_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band A/D2 input filter. The Cutoff Frequency = 125000 / (AD2_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ☜

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 400D	400D	DSP1 FPGA	DA1_FILTDEV - read/write The DA1_FILTDEV is an 8-bit register, used to define the cutoff frequency of D/A1 filter. The Cutoff Frequency = 125000 / (DA1_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ☜
6000 400E	400E	DSP1 FPGA	DA2_FILTDEV - read/write The DA2_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band D/A2 filter. The Cutoff Frequency = 125000 / (DA2_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ☜
6000 400F	400F	DSP1 FPGA	MLVDSBUS0_DRIVE - read/write MLVDSBUS0_DRIVE is an LSB valuable register, used to enable the drive of MLVDSBUS0 signal. If MLVDSBUS0_DRIVE = 0 then MLVDSBUS0 is not driven☜ If MLVDSBUS0_DRIVE = 1 then MLVDSBUS0 is driven by the signal which is selected by MLVDSBUS0_DRIVE_SELECT
6000 4010	4010	DSP1 FPGA	MLVDSBUS1_DRIVE - read/write MLVDSBUS1_DRIVE is an LSB valuable register, used to enable the drive of MLVDSBUS1 signal. If MLVDSBUS1_DRIVE = 0 then MLVDSBUS1 is not driven☜ If MLVDSBUS1_DRIVE = 1 then MLVDSBUS1 is driven by the signal which is selected by MLVDSBUS1_DRIVE_SELECT

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4011	4011	DSP1 FPGA	MLVDSBUS0_DRIVE_SELECT - read/write The MLVDSBUS0_DRIVE_SELECT is a 4-bit register, used to define the MLVDSBUS0 drive source: MLVDSBUS0_DRIVE_SELECT MLVDSBUS0 0000 DDS output signal ☜ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal 0110 DSP2 TOUT0 signal 0111 DSP2 TOUT1 signal 1000 DSP2 TOUT2 signal
6000 4012	4012	DSP1 FPGA	MLVDSBUS1_DRIVE_SELECT - read/write The MLVDSBUS1_DRIVE_SELECT is a 4-bit register, used to define the MLVDSBUS1 drive source: MLVDSBUS1_DRIVE_SELECT MLVDSBUS1 0000 DDS output signal☜ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal 0110 DSP2 TOUT0 signal 0111 DSP2 TOUT1 signal 1000 DSP2 TOUT2 signal

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4013	4013	DSP1 FPGA	FPGAT1T2CLKIN_SELECT - read/write The FPGAT1T2CLKIN_SELECT is a 4-bit register, used to define the FPGAT1T2CLKIN signal: FPGAT1T2CLKIN_SELECT FPGAT1T2CLKIN 0000 RBMLVDSBUS0 signal☜ 0001 RBMLVDSBUS1 signal 0010 DDS out signal
6000 4014	4014	DSP1 FPGA	HAD12CLKSEL - read/write The HAD12CLKSEL is a 4-bit register, used to define the HAD12CLK signal: HAD12CLKSEL HAD12CLK 0000 DDS out signal ☜ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal

Memóriába ágyazott eszközök - FPGA erőforrások , EMIFB CE0

6000 4015	4015	DSP1 DSP2 FPGA	INT4_SEL - read/write Writing this register from DSP1 means the setting of DSP1_INT4_SEL, while from the DSP2 means the setting of DSP2_INT4_SEL register. The INT4_SEL is a 4-bit register, used to define the INT4 source: INT4_SEL INT4 0000 INT4_SEND of the other DSP ☜ 0001 RBMLVDSBUS0 signal 0010 RBMLVDSBUS1 signal 0011 SYNCBUS0 signal 0100 SYNCBUS1 signal 0101 SYNCBUS2 signal 0110 AD1BUSYL signal 0111 AD2BUSYL signal 1000 FRAMER1INT signal 1001 FRAMER2INT signal 1010 HAD1OVERLOAD signal 1011 HAD2OVERLOAD signal

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4018	4018	DSP1 DSP2 FPGA	INT4_SEND - write only Writing a dummy data to this address generates a TINT4SEND in the other DSP.
6000 4019	4019	DSP1 DSP2 FPGA	INT5_SEND - write only Writing a dummy data to this address generates a TINT5SEND in the other DSP.
6000 401A	401A	DSP1 DSP2 FPGA	INT6_SEND - write only Writing a dummy data to this address generates a TINT6SEND in the other DSP.
6000 401B	401B	DSP1 FPGA	HAD12_FIFO_STATUS - read only Reading this 4-bit register the high-speed A/D1 and A/D2 FIFO status can be read: D3 D2 D1 D0 HAD2 Empty HAD2 Full HAD1 Empty HAD1 Full *FIFO status bits are only valid after an active write enable and FIFO write signal.*

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 401C	401C	DSP1 FPGA	AD1CONVSTARTSEL - read/write The AD1CONVSTARTSEL is a 4-bit register, used to define the AD1CONVSTARTsource: AD1CONVSTARTSEL — AD1CONVSTARTsource 0000 — DSP1 SW1_START command ☜ 0001 — DSP1 SW2_START command 0010 — DSP2 SW1_START command 0011 — DSP2 SW2_START command 0100 — RBMLVDSBUS0 signal 0101 — RBMLVDSBUS1 signal 0110 — SYNCBUS0 signal 0111 — SYNCBUS1 signal 1000 — SYNCBUS2 signal 1001 — DSP1 TOUT0 signal 1010 — DSP1 TOUT1 signal 1011 — DSP1 TOUT2 signal 1100 — DSP2 TOUT0 signal 1101 — DSP2 TOUT1 signal 1110 — DSP2 TOUT2 signal 1111 — DDS out signal

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4020	4020	DSP1 FPGA	AD1MODESEL - read/write The AD1MODESEL is a 4-bit register, used to define the AD1MODE: AD1MODESEL AD1MODE 0000 A/D1 Gain = off Filter off ☜ 0001 A/D1 Gain = on Filter off 0010 A/D1 Gain = on Filter on
6000 4021	4021	DSP1 FPGA	AD2MODESEL - read/write The AD2MODESEL is a 4-bit register, used to define the AD2MODE: AD2MODESEL AD2MODE 0000 A/D2 Gain = off Filter off☜ 0001 A/D2 Gain = on Filter off 0010 A/D2 Gain = on Filter on

Memóriába ágyazott eszközök - FPGA erőforrások , EMIFB CE0

6000 4022	4022	DSP1 FPGA	SYNCBUS0SEL - read/write The SYNCBUS0SEL is an 8-bit register, used to define the SYNCBUS0SEL source: SYNCBUS0SEL SYNCBUS0 source 0-0000 0000 RDDSCOMPOUT ☜ 1-0000 0001 C2048K 2-0000 0010 F1_RCLK 3-0000 0011 F2_RCLK 4-0000 0100 T1_TIMER_OUT0 5-0000 0101 T1_TIMER_OUT1 6-0000 0110 T1_TIMER_OUT2 7-0000 0111 T2_TIMER_OUT0 8-0000 1000 T2_TIMER_OUT1 9-0000 1001 T2_TIMER_OUT2 A-0000 1010 AD1SCCLK B-0000 1011 AD2SCCLK C-0000 1100 DA1SCCLK D-0000 1101 DA2SCCLK E-0000 1110 AD1CONVSTARTL F-0000 1111 AD2CONVSTARTL 10-0001 0000 DA1LDACL 11-0001 0001 DA2LDACL 12-00010010 T1_GP_INT4 13-00010011 T1_GP_INT5 14-00010100 T1_GP_INT6 15-00010101 T2_GP_INT4 16-00010110 T2_GP_INT5 17-00010111 T2_GP_INT6 18-00011000 T1_GPIO8 19-00011001 T2_GPIO8 1A-00011010 F1_RCLK 1B-00011011 F2_RCLK 1C-00011100 F1_TCLK 1D-00011101 F2_TCLK

Memóriába ágyazott eszközök - FPGA erőforrások

6000 4023	4023	DSP1 FPGA	SYNCBUS1SEL - read/write The SYNCBUS1SEL is an 8-bit register, used to define the SYNCBUS1SEL source: SYNCBUS1SEL — SYNCBUS1 source 0- 0000 0000 — RDDSCOMPOUT ☜ 1- 0000 0001 — C2048K 2- 0000 0010 — F1_RCLK 3- 0000 0011 — F2_RCLK 4- 0000 0100 — T1_TIMER_OUT0 5- 0000 0101 — T1_TIMER_OUT1 6- 0000 0110 — T1_TIMER_OUT2 7- 0000 0111 — T2_TIMER_OUT0 8- 0000 1000 — T2_TIMER_OUT1 9- 0000 1001 — T2_TIMER_OUT2 A- 0000 1010 — AD1SCCLK B- 0000 1011 — AD2SCCLK C- 0000 1100 — DA1SCCLK D- 0000 1101 — DA2SCCLK E- 0000 1110 — AD1CONVSTARTL F- 0000 1111 — AD2CONVSTARTL 10-0001 0000 — DA1LDACL 11-0001 0001 — DA2LDACL 12-0001 0010 — T1_GP_INT4 13-0001 0011 — T1_GP_INT5 14-0001 0100 — T1_GP_INT6 15-0001 0101 — T2_GP_INT4 16-0001 0110 — T2_GP_INT5 17-0001 0111 — T2_GP_INT6 18-0001 1000 — T1_GPIO8 19-0001 1001 — T2_GPIO8 1A-00011010 — F1_RSER 1B-00011011 — F2_RSER 1C-00011100 — F1_TSER 1D-00011101 — F2_TSER

Memóriába ágyazott eszközök - FPGA erőforrások

6000 4024	4024	DSP1 FPGA	SYNCBUS2SEL - read/write The SYNCBUS2SEL is an 8-bit register, used to define the SYNCBUS2SEL source: SYNCBUS2SEL — SYNCBUS2 source 0- 0000 0000 — RDDSCOMPOUT ☜ 1- 0000 0001 — C2048K 2- 0000 0010 — F1_RCLK 3- 0000 0011 — F2_RCLK 4- 0000 0100 — T1_TIMER_OUT0 5- 0000 0101 — T1_TIMER_OUT1 6- 0000 0110 — T1_TIMER_OUT2 7- 0000 0111 — T2_TIMER_OUT0 8- 0000 1000 — T2_TIMER_OUT1 9- 0000 1001 — T2_TIMER_OUT2 A- 0000 1010 — AD1SCCLK B- 0000 1011 — AD2SCCLK C- 0000 1100 — DA1SCCLK D- 0000 1101 — DA2SCCLK E- 0000 1110 — AD1CONVSTARTL F- 0000 1111 — AD2CONVSTARTL 10-0001 0000 — DA1LDACL 11-0001 0001 — DA2LDACL 12-00010010 — T1_GP_INT4 13-00010011 — T1_GP_INT5 14-00010100 — T1_GP_INT6 15-00010101 — T2_GP_INT4 16-00010110 — T2_GP_INT5 17-00010111 — T2_GP_INT6 18-00011000 — T1_GPIO8 19-00011001 — T2_GPIO8 1A-00011010 — F1_RSYNC 1B-00011011 — F2_RSYNC 1C-00011100 — F1_TSYNC 1D-00011101 — F2_TSYNC

Memóriába ágyazott eszközök - FPGA erőforrások , EMIFB CE0

6000 4025	4025	DSP1 FPGA	SYNCBUS0DRVEN - read/write SYNCBUS0DRVEN is an LSB valuable register used to control the drive source of SYNCBUS0 signal. If SYNCBUS0DRVEN = 1 then the SYNCBUS0 is driven by the SYNCBUS0SEL selected signal. If SYNCBUS0DRVEN = 0 ☜ then the SYNCBUS0 is not driven on the board. SYNCBUS0 may be driven by only one source.
6000 4026	4026	DSP1 FPGA	SYNCBUS1DRVEN - read/write SYNCBUS1DRVEN is an LSB valuable register used to control the drive source of SYNCBUS10 signal. If SYNCBUS1DRVEN = 1 then the SYNCBUS1 is driven by the SYNCBUS1SEL selected signal. If SYNCBUS1DRVEN = 0 ☜ then the SYNCBUS1 is not driven on the board. SYNCBUS1 may be driven by only one source.
6000 4027	4027	DSP1 FPGA	SYNCBUS2DRVEN - read/write SYNCBUS2DRVEN is an LSB valuable register used to control the drive source of SYNCBUS2 signal. If SYNCBUS2DRVEN = 1 then the SYNCBUS2 is driven by the SYNCBUS2SEL selected signal. If SYNCBUS2DRVEN = 0 ☜ then the SYNCBUS2 is not driven on the board. SYNCBUS2 may be driven by only one source.

Memóriába ágyazott eszközök - FPGA erőforrások, EMIFB CE0

6000 4028	4028	DSP1 FPGA	DA1UPDATESEL - read/write The DA1UPDATESEL is a 4-bit register, used to define the DA1UPDATE source: DA1UPDATESEL — DA1UPDATE source 0000 — DSP1 SW_UPDATE1 command ☜ 0001 — DSP1 SW_UPDATE2 command 0010 — DSP2 SW_UPDATE1 command 0011 — DSP2 SW_UPDATE2 command 0100 — RBMLVDSBUS0 signal 0101 — RBMLVDSBUS1 signal 0110 — SYNCBUS0 signal 0111 — SYNCBUS1 signal 1000 — SYNCBUS2 signal 1001 — DSP1 TOUT0 signal 1010 — DSP1 TOUT1 signal 1011 — DSP1 TOUT2 signal 1100 — DSP2 TOUT0 signal 1101 — DSP2 TOUT1 signal 1110 — DSP2 TOUT2 signal 1111 — DDS out signal

E1 Interfészek – EMIFB CE1 8 bit

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Size (Bytes)	Description of Memory
6400 0000–6400 00FF	DSPP=190 00 0000–00 00FF	-	256	*Framer1 E1 interface* External memory interface EMIFB CE1 as 8bit wide asynchronous memory
6400 0100–6400 01FF	DSPP=190 00 0100–00 01FF	-	256	*Framer2 E1 interface* External memory interface EMIFB CE1 as 8bit wide asynchronous memory

A/D, D/A – EMIFB CE2 16 bit

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 Offset Address	Size (Bytes)	Read access to memory	Write access to memory
6800 0000–6C00 0001	DSPP=1A0 00 0000–00 0001	-	1W 2B	*A/D1 16bit read*	*SW1_START* Writing a dummy data to this address generates an SW1_START command.
6800 0002–6C00 0003	DSPP=1A0 00 0002–00 0003	-	1W 2B	*A/D2 16bit read*	*SW2_START* Writing a dummy data to this address generates an SW2_START command.
6800 0004–6C00 0005	DSPP=1A0 00 0004–00 0005	-	1W 2B	-	*SW1/SW2_START* Writing a dummy data to this address generates a simultaneous SW1_START and SW2_START command.

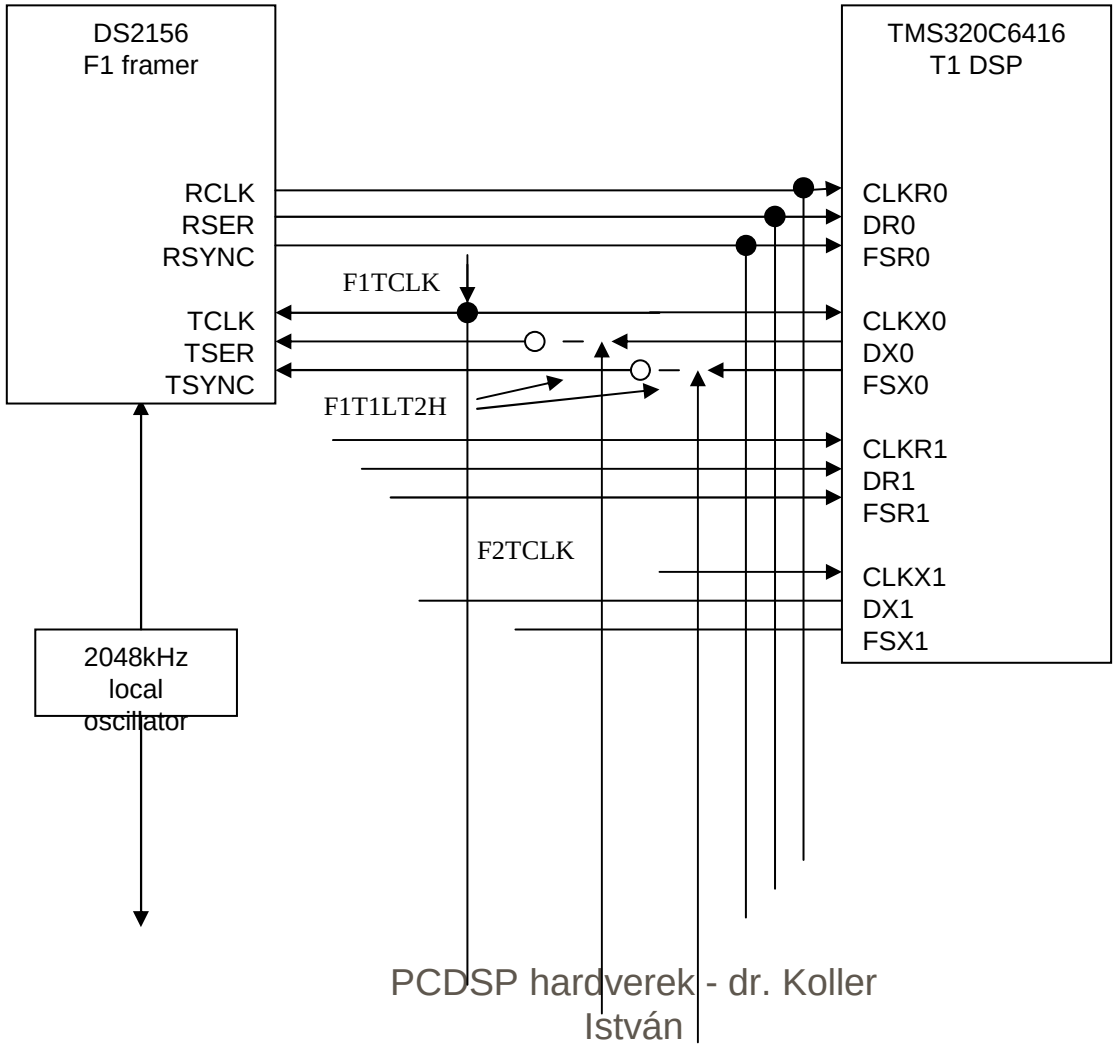
A/D, D/A – EMIFB CE2
16 bit

6800 0008– 6C00 0009	DSPP=1A0 00 0006– 00 0007	-	1W 2B	*SW_UPDATE1* Reading a dummy data from this address generates an SW_UPDATE1 command.	*D/A/1 16bit write*, The upper 14 bits are valid, the code format is two's complement
6800 000A– 6C00 000B	DSPP=1A0 00 0008– 00 0009	-	1W 2B	*SW_UPDATE2* Reading a dummy data from this address generates an SW_UPDATE2 command	*D/A/1 16bit write*, The upper 14 bits are valid, the code format is two's complement
6800 000C– 6C00 000D	DSPP=1A0 00 000A8– 00 000B	-	1W 2B	*SW_UPDATE1/SW_UP DATE2* Reading a dummy data from this address generates a simultaneous SW_UPDATE1 and SW_UPDATE2 command	-

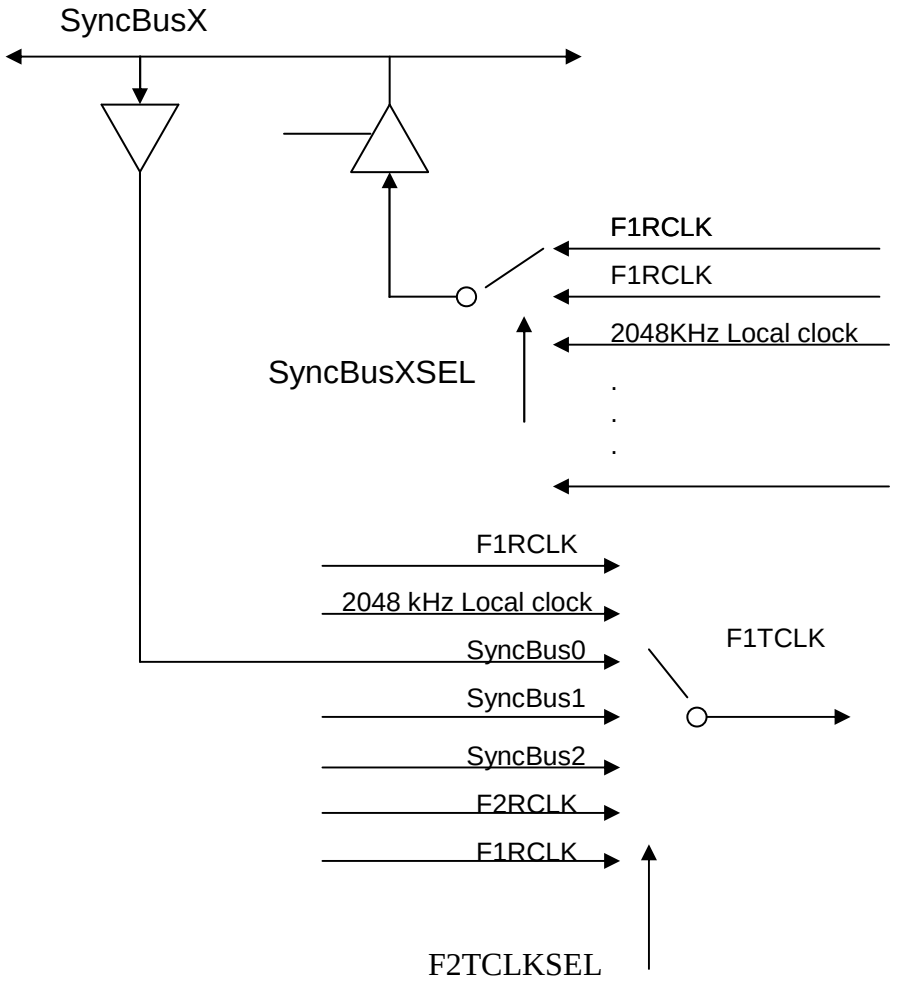
High-speed A/D, two-port memory, EMIFB CE3
16 bit

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Decoded in DSP1/ DSP2	Size (Bytes)	Description of Memory
6C00 0000–6C00 3FFF	DSPP=1B0 00 0000–00 3FFF	-	DSP1	8KW 16KB	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D1 FIFO*
6C00 4000–6C00 7FFF	DSPP=1B0 00 4000–00 7FFF	-	DSP1	8KW 16KB	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D 2 FIFO*
6C00 8000–6C00 FFFF	DSPP=1B0 00 8000–00 FFFF	-	DSP1 DSP2	16KW 32KB	External memory interface EMIFB CE3 as 16bit wide synchronous *Two-port memory*

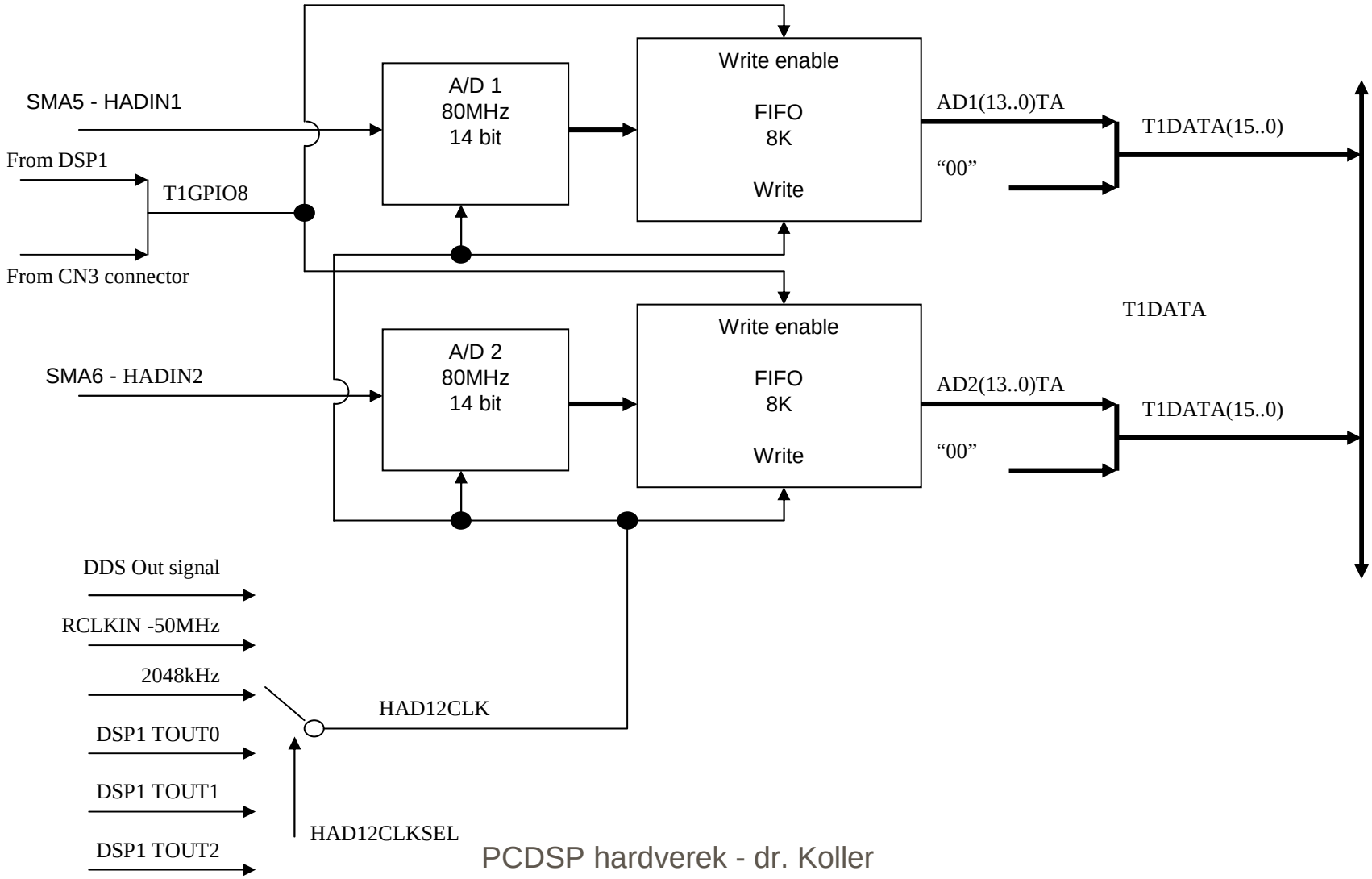
E1 framer - DSP összekapcsolása



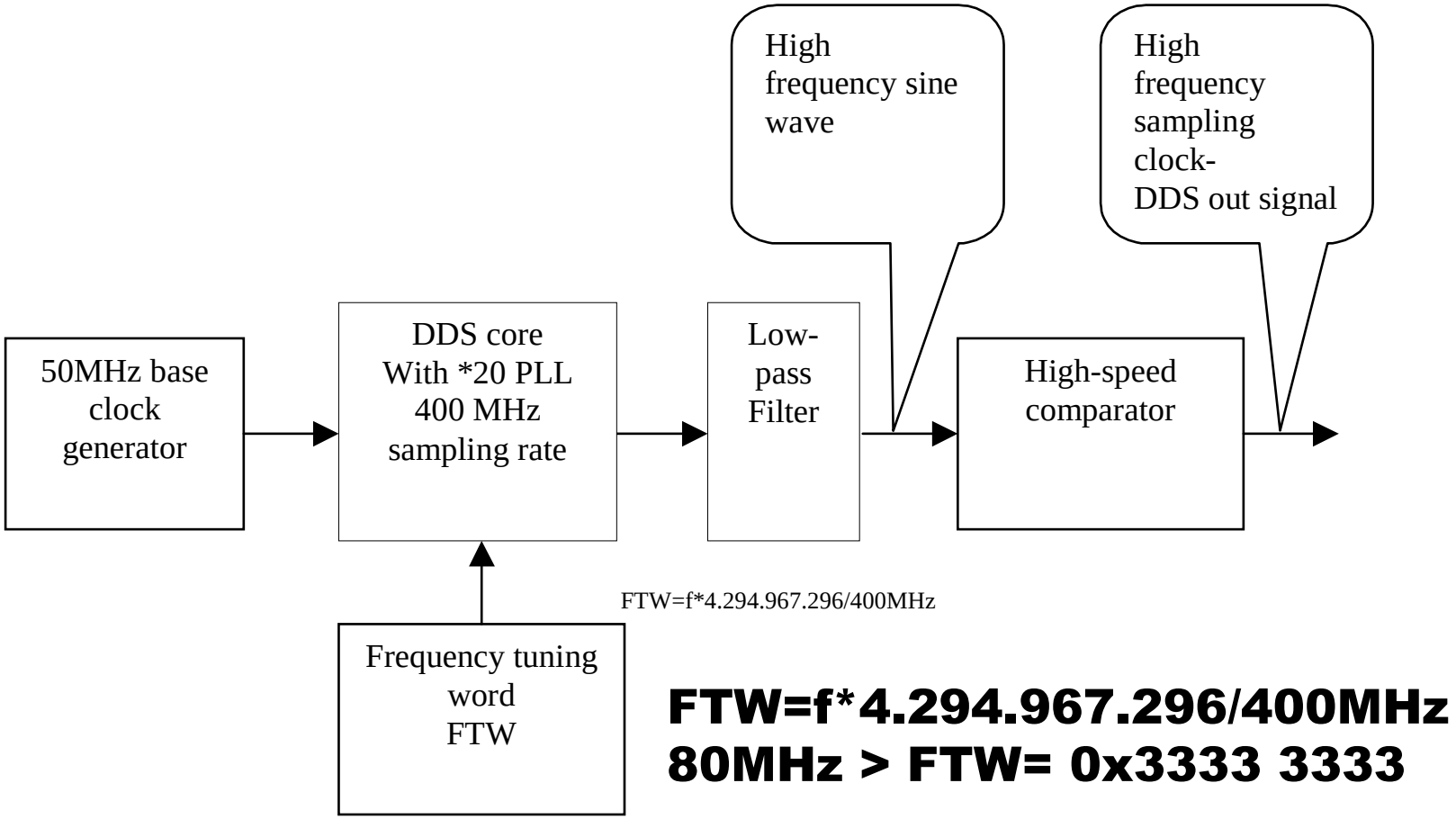
E1 adási órajel származtatása



High-speed A/D



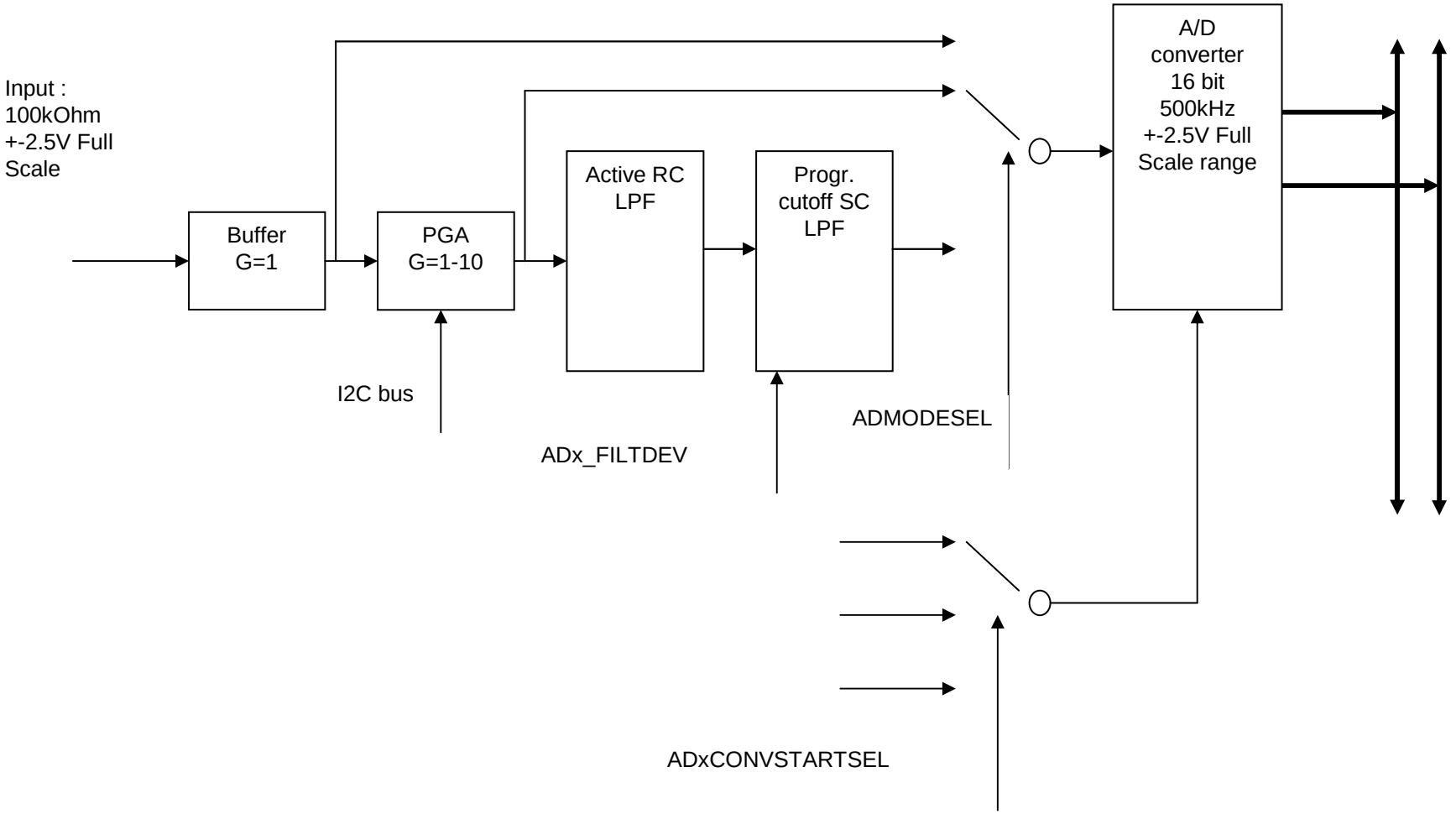
DDS órajelgenerátor



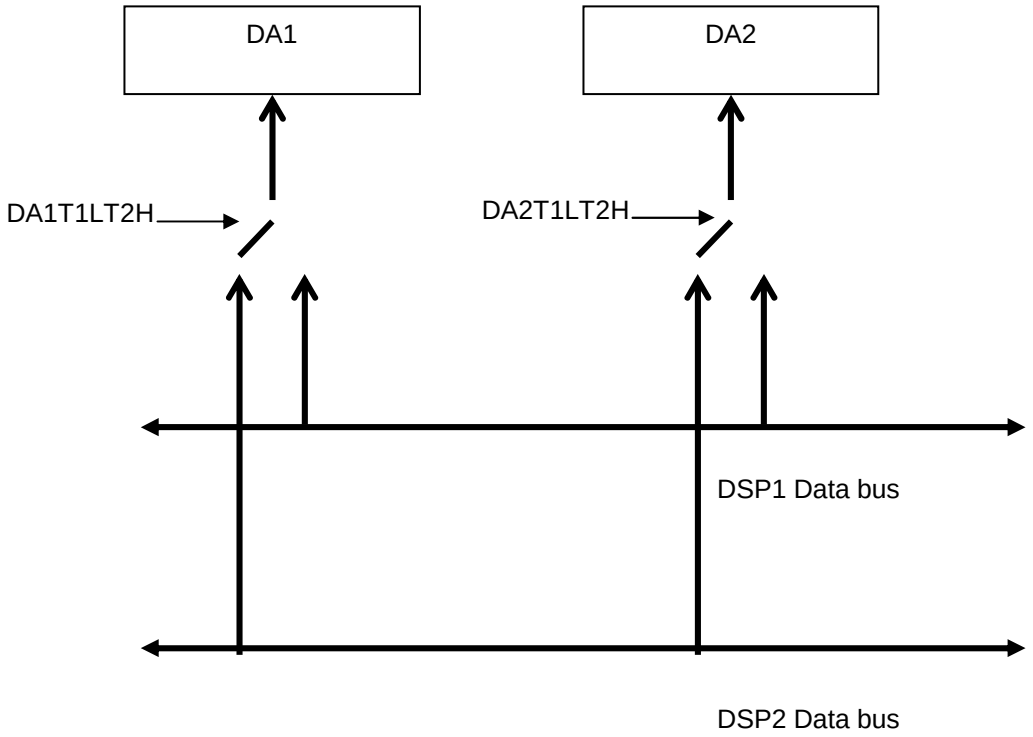
FTW=f*4.294.967.296/400MHz

80MHz > FTW= 0x3333 3333

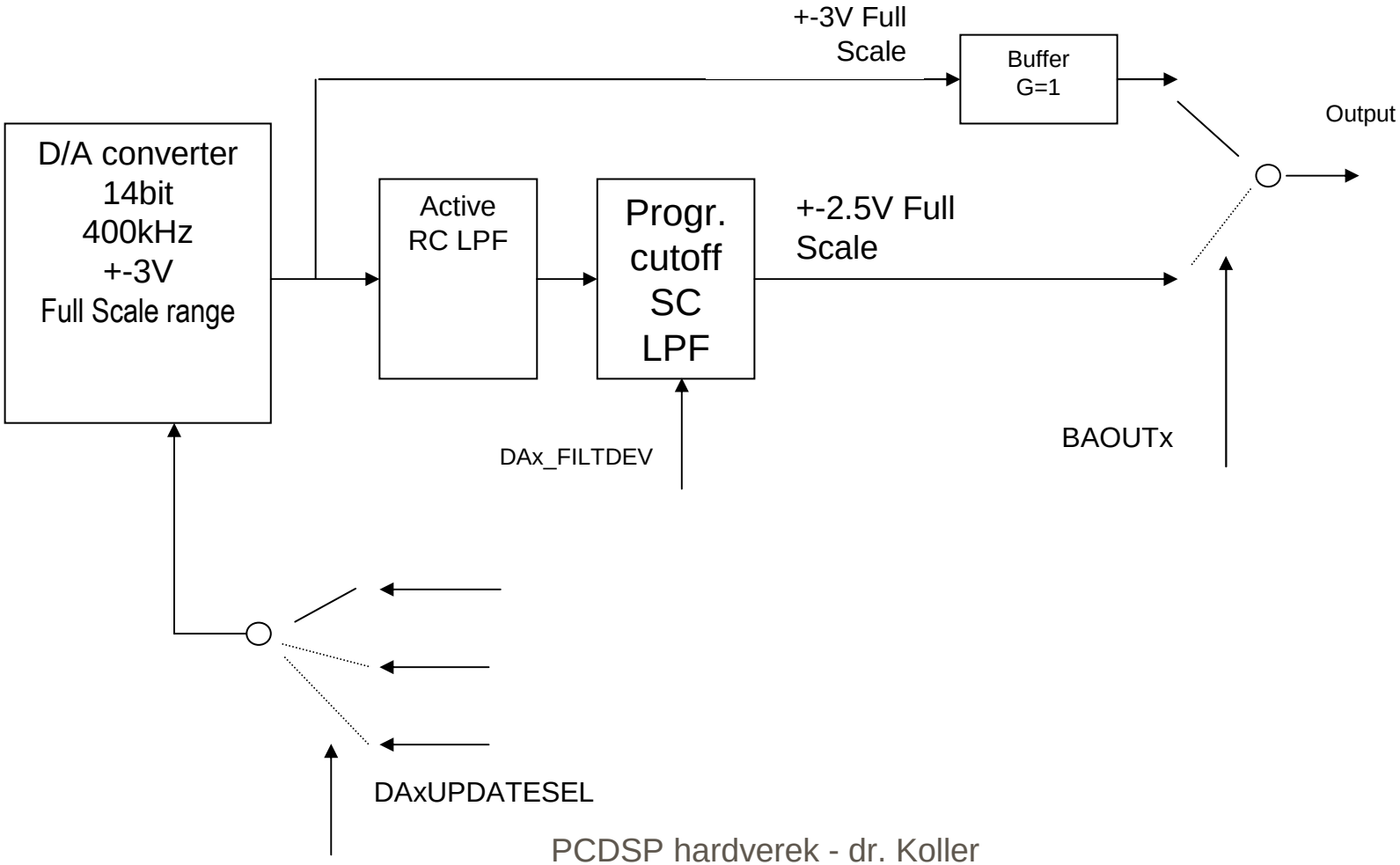
A/D és D/A fokozatok



D/A konverterek DSP-hez való rendelése



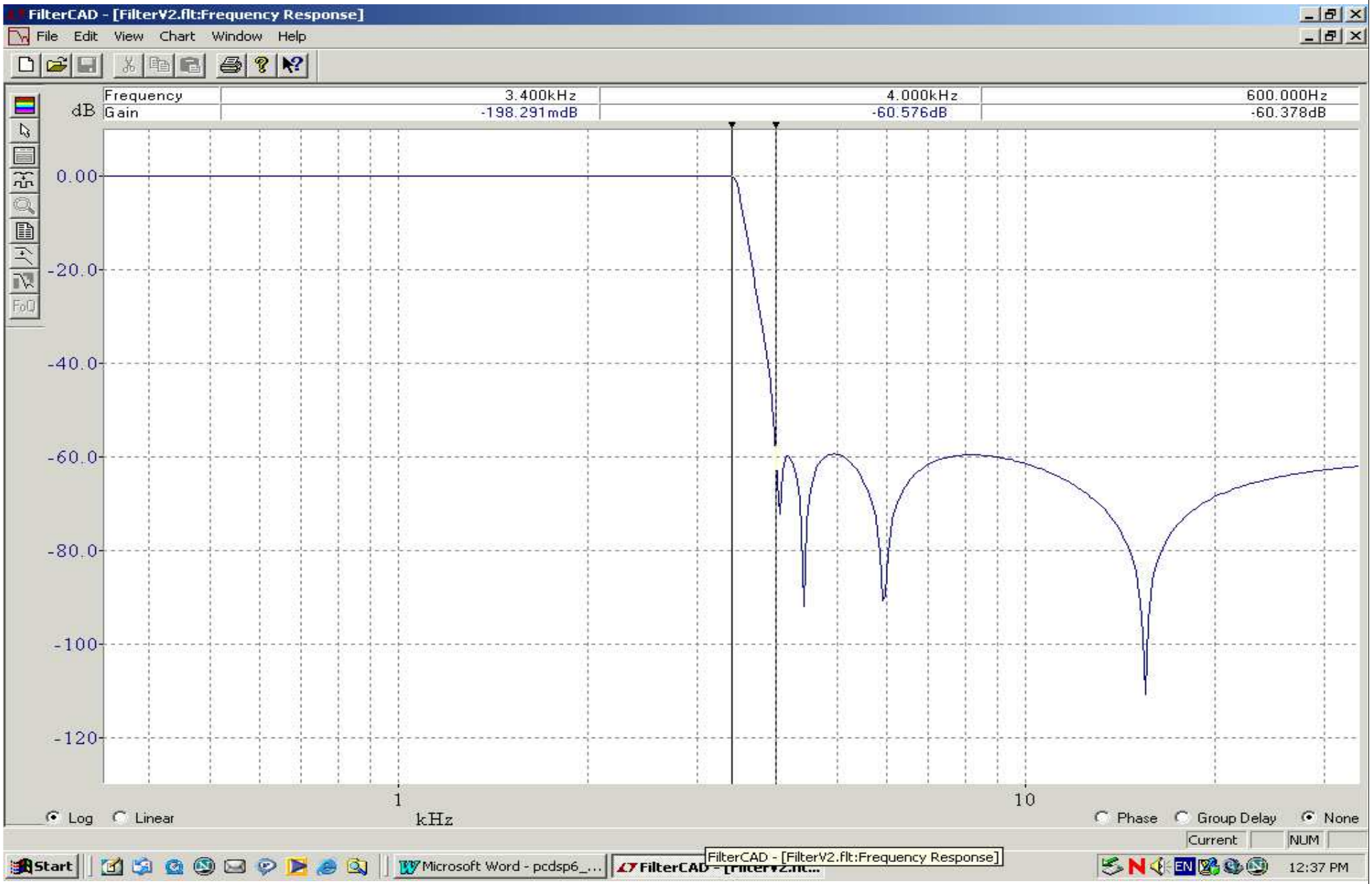
D/A konverterek DSP-hez való rendelése



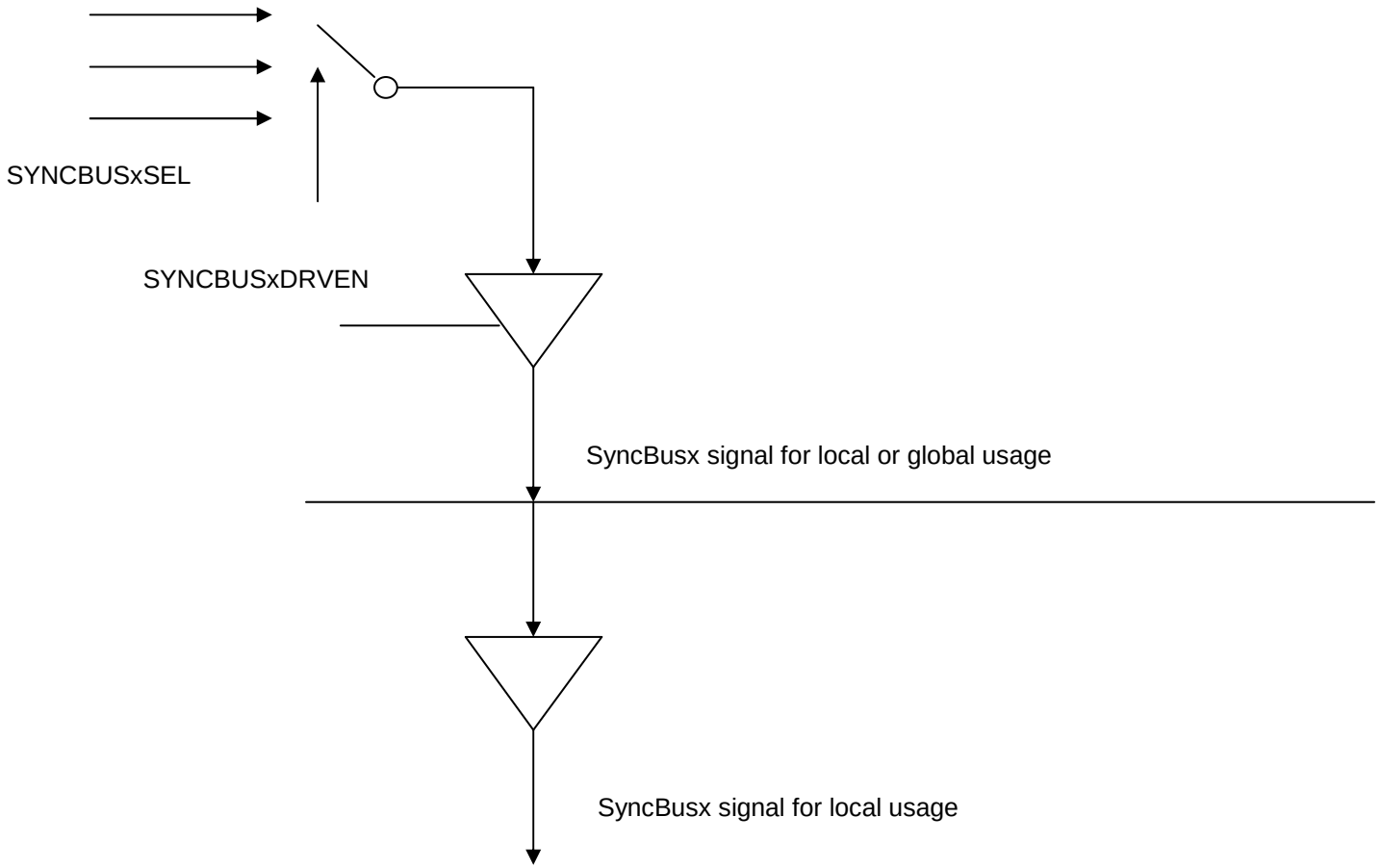
SC szűrő beállítása

ADxFILTDEV DAxFILTDEV	SC filter Clock Frequency	Cut-off frequency	50MHz CLKIN frequency – 1GHz DSP, the Cutoff Frequency =
4	5MHz	25 000Hz	
5	4.167MHz	20 833Hz	125000/(AD1_FILTDEV+1) [Hz].
6	3.571MHz	17 857Hz	
35	694kHz	3 472Hz	The power up reset state is ADx_FILTDEV=124, which means 1000Hz cutoff. ☜
36	675kHz	3 378Hz	
37	657kHz	3 289Hz	
124☜	200kHz☜	1000Hz☜	
255	97kHz	488Hz	

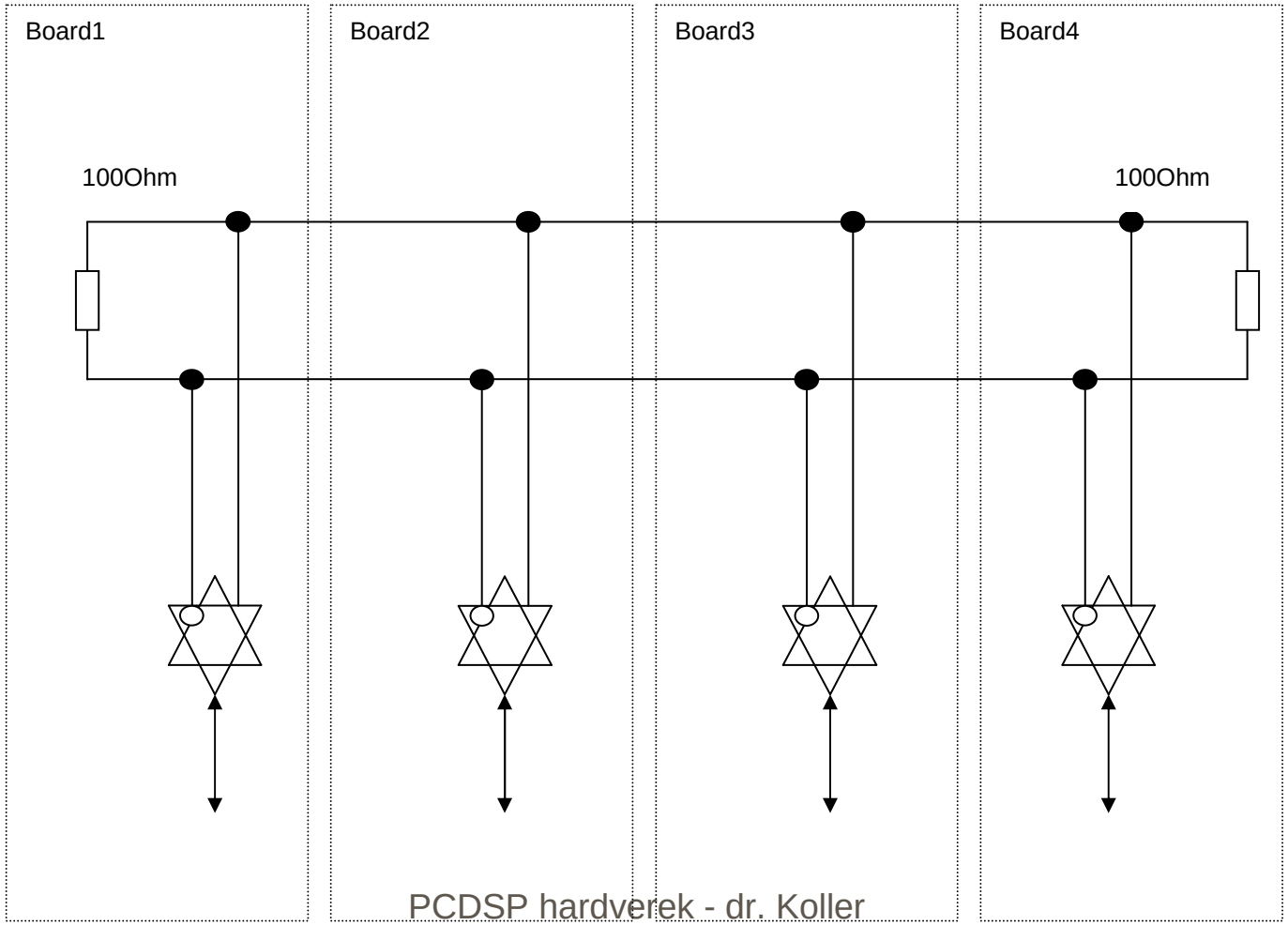
SC szűrő csillapítás menete



SyncBus


SYNCBUSxSEL
SYNCBUSxDRVEN
SyncBusx signal for local or global usage
SyncBusx signal for local usage

MLVDSbus



Host to DSP interrput

- A DSPINT bit a HDCR regiszterben

PCI Address	DSP address	Base 1 offset	Function
I/O Base Address + 00h	0x01C1 FFF0	0x41 FFF0	Host status register (HSR)
I/O Base Address + 04h	0x01C1 FFF4	0x41 FFF4	Host-to-DSP control register (HDCR)
I/O Base Address + 08h	0x01C1 FFF8	0x41 FFF8	DSP page register (DSPP)
I/O Base Address + 0Ch	Reserved	Reserved	Reserved

Külső DSP Interruptok

Interrupt	Interrupt source
DSP1 NMI	NMI command
DSP1 ExtInt4	Can be programmed by the DSP1_INT4_SEL register
DSP1 ExtInt5	Can be programmed by the DSP1_INT5_SEL register
DSP1 ExtInt6	Can be programmed by the DSP1_INT6_SEL register
DSP1 ExtInt7	Generated by writing doorbell register or by the external source connected to CN 3 Pin1

Interrupt	Interrupt source
DSP2 NMI	NMI command
DSP2 ExtInt4	Can be programmed by the DSP2_INT4_SEL register
DSP2 ExtInt5	Can be programmed by the DSP2_INT5_SEL register
DSP2 ExtInt6	Can be programmed by the DSP2_ INT6_SEL register
DSP2 ExtInt7	Generated by writing doorbell register or by the external source connected to CN3 Pin11

DSP to HOST interrupt
INTA#, INTB# Interruptok

- DSP1 - **INTA#**
- DSP2 - **INTB#**