PCDSP6

User's Manual

Version 1.2

Firmware version: CPLD Ver 1.0, FPGA Ver1.2

4/28/2006 02:25:00 PM

2006

Revision History

1.16.2006   New issued version

02.282006   V1.1.: Added serial port signals to SyncBus

                    Gated E1/T1/J1 serial port signal by RLOS

02.282006   V1.2.: Added clock signals to SyncBus

Additional Documents:

1. FPGA: http://direct.xilinx.com/bvdocs/publications/ds099.pdf

2. Ti DSP chip: http://focus.ti.com/lit/ds/symlink/tms320c6416t.pdf

3. E1 Transceiver / Framer: http://pdfserv.maxim-ic.com/en/ds/DS2156-DS2156LN.pdf

4. DDS chip: http://www.analog.com/UploadedFiles/Data_Sheets/35675155932219AD9952_0.pdf

5. Xicor Digital Pots: http://www.intersil.com/data/fn/fn8164.pdf

6. PCI to PCI bridge: http://www2.plxtech.com/TEMP/841/PCI6152_DataBook_v2.0.pdf

1. Overview

The PCDSP6 is high performance FPGA and dual DSP board with E1 interface, two-channel high-speed analog inputs plus DAQ quality base-band analog front-end for desktop PC compatible computers with 32bit/33MHz PCI bus.

1.1. Board features
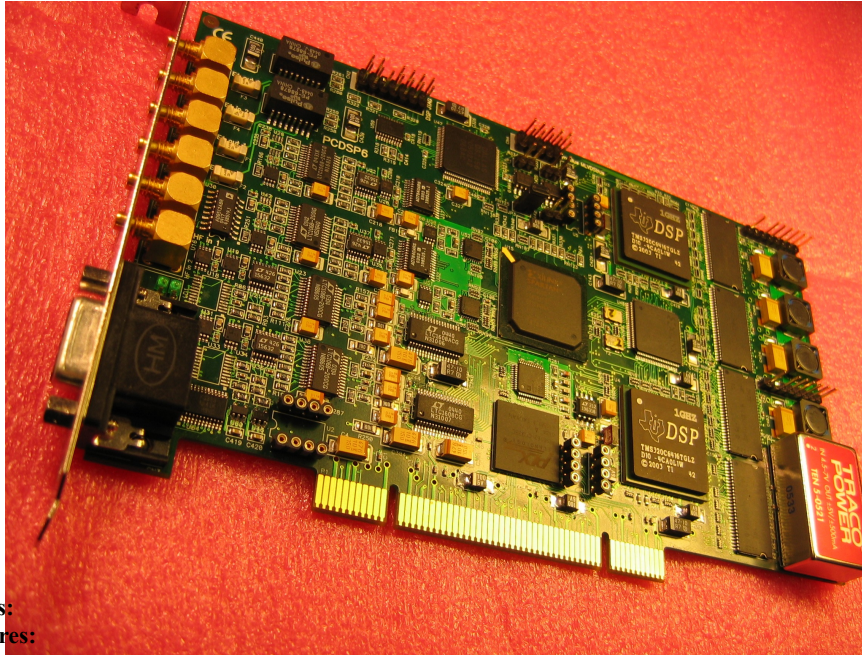
Main features:

Overall features:

- Universal structure for wide area of high-speed, complex signal processing applications
- 100% user defined resource allocation capability to fit with the application need
- Ideal tool for high-speed (FPGA), and lower speed but complex (DSP) signal processing applications
- Complete signal processing capability from 70MHz IF signal to multi-channel base band digital demodulation
- High resolution DDS based sampling signal generator
- LVDS clock/sync bus for multi-board synchronization
- Two channel DAQ quality analog input and output section with programmable antialiasing filters
- Complete two-channel E1 receive/transmit processing capability from
- Two highest speed DSPs of the world
- SPARTAN3 FPGA, which is freely programmable for the user

DSP section

- *two* TMS320C6416 Digital Signal Processors
- highest speed DSP of the world - *1GHz*
- 128 Mbyte 64 bit wide SDRAM for both processors
- Local PCI bus for internal data transfer
- very fast two port memory between DSPs
- all DSP resources can be accessed from the PCI bus
- configurable interrupt system allowing high level flexibility

FPGA section

- 1.5 Million gate FPGA, fully user programmable from host PC, with SelectMap real-time debug feature
- Digital Down Converter core, FIFO core, two-port memory core, etc. are implemented.

E1 input/output section:

- 2 independent framers with E1 line interface and framer units
- E1 interfaces can be assigned to DSPs freely
- Signal processing capability of E1/T1/J1 signals in the FPGA also

Low frequency analog input/output section:

- Two input channels with programmable gain and programmable cutoff frequency low pass filters
- Nonvolatile digital potmeters for gain and offset adjust
- 16 bit A/D converters with 500 kHz maximum sampling rate
- Versatile sampling signal sources containing external sampling source signal capability
- Two-channel 14 bit D/A converters with 500 kHz maximum update rate with programmable low pass filters

High frequency analog input section:

- Two channel *14 bit 80MHz* sampling rate A/D converter with simultaneous sampling capability on channels
- High resolution DDS based sampling clock generator
- LVDS clock bus for multiboard synchronous operation

Analog input path

Analog In1, In2 → Programmable Gain, Filter → Analog Input A/D 500kHz 16 bit → XILINX SPARTAN III FPGA (1,5 million gates)

Programmable Filter → Analog Output D/A 400kHz- 14 bit

High Frequency Analog In1, In2 → Signal Conditioning → High-frequency Analog Input A/D–80MHz 14 bit

Signal Conditioning → High-frequency Analog Input A/D–80MHz 14 bit

JTAG → JTAG connector → High-resolution DDS based clock generator

E1 I/O → Line Interface → E1 transceiver → Data, clock

E1 I/O → Line Interface → E1 transceiver → Data, clock

SyncBus → SyncBus LVDS BUS

PCDSP6 Ver. 1.2

Processing / memory

SDRAM 128MB

EMIFA
McBSP 1.. 0
PCI Interface
EMIFB
TMS320C6416T 1GHz

XILINX CPLD
FPGA programmer, Communiction register, Real-time debug

TMS320C6416T 1GHz
EMIFB
PCI Interface
McBSP 1-.. 0
EMIFA

SDRAM 128MB

Internal PCI bus

PCI-PCI bridge

PCI bus   6

1.2. Power up, reset

After power up, the board has neither FPGA, nor DSP codes. Before these codes are filled up, the first task is the DSP EMIF register initialization. The DSPs boot mode operation is the PCI boot mode. After power up, the DSPs are in PCI boot mode, which means waiting for a DSP program code, and after download a valid DSP code a DSPINT command (writing 0x2 to the HDCR register, 0x41FFF4 offset of Base 1) starts the program execution. The warm reset can be activated any time (writing 0x1 to the HDCR register, 0x41FFF4 offset of Base 1) to stop the DSP program execution.

After power up the first task is the EMFA and EMIFB registers setting. After that, the FPGA code can be downloaded via the EMIFB FPGA programming area of DSP1 by a host program, or by a DSP program, which is recommended, because the FPGA configuration data load is much faster by the DSP.

2. Hardware Installation

The PCDSP6 is a PCI slot board. To install the board you need to do the following steps:
- Make sure, that your PC is powered off
- Use electrostatic wrist tool
- Open your PC to get a free 32 bit bus master PCI slot
- Check the jumper settings on the PCDSP6 board
- Insert the PCDSP6 board into a free bus master PCI slot
- Close the PC box and power-up.

2.1. Jumpers and board layout

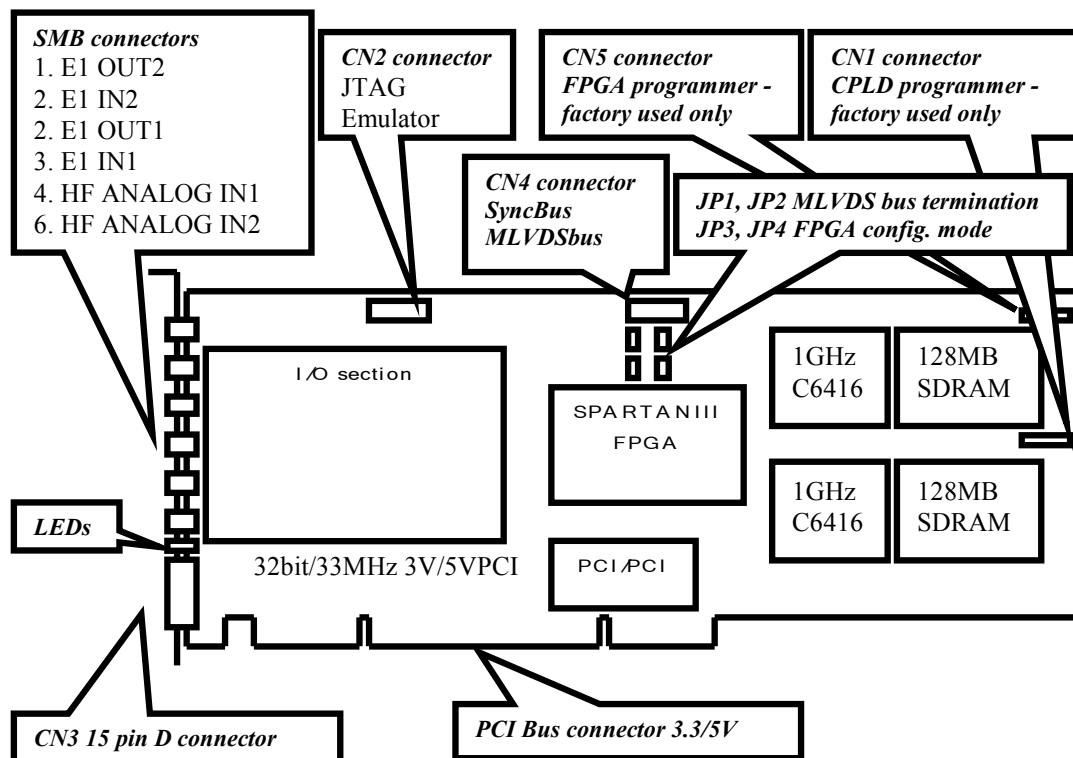The Figure 2.1. shows the PCDSP6 connectors and jumpers.

Figure 2.1.1

2.1.1 JP1, JP2 Jumpers

The JP1 and JP2 jumpers are used to terminate the MLVDS BUS by a 100Ohm resistor. The termination should be used at the ends of the lines. If JP1 and JP2 jumper is installed, the MLVDSBUS0 and the MLVDSBUS1 respectively are terminated by 100 Ohm resistors. In the case of more than two-board systems the middle boards may not have termination resistors installed.

2.1.2 JP3, JP4 Jumpers

The JP3 and JP4 jumpers are used to define the programming mode of the on board FPGA according to the Table 2.1.2.1.

JP4	JP3	Programming mode
on	off	JTAG (Factory test mode)
off	on	Slave parallel (SelectMap mode)

Table 2.1.2.1.

2.2. I/O Connectors

2.2.1. E1 SMB connectors

The SMB connectors from up to down:
1. E1 OUT 2 The F2 framer 75 Ohm output signal
2. E1 IN 2 The F2 framer 75 Ohm input signal
3. E1 OUT 1 - The F1 framer 75 Ohm output signal
4. E1 IN 1- The F1 framer 75 Ohm input signal.
5. HF ANALOG IN 1 - The high-speed A/D1 50 Ohm input signal
6. HF ANALOG IN 2 - The high-speed A/D2 50 Ohm input signal

2.2.2. The 15 pin D connector CN3

Signal name	No of pin	Signal name	No of pin	Signal name	No of pin
AIN2	15	AGND	10	AIN1	5
SWAOUT2	14	AGND	9	SWAOUT1	4
T2 DSP GPIO0 input/output 5V compliant	13	DGND	8	T1 DSP GPIO0 input/output 5V compliant	3
T2 DSP GPIO8 input/output 5V compliant	12	T2 DSP TIMER2 input 5V compliant	7	T1 DSP GPIO8 input/output 5V compliant	2
T2 DSP GPINT7 input 5V compliant	11	T1 DSP TIMER2 input 5V compliant	6	T1 DSP GPINT7 input 5V compliant	1

Table 2.2.2.

2.2.3. SyncBus, MLVDSbus – CN4

The MLVDSBUS is a two-wire low voltage differential high-speed bus for synchronous operation of multi-board systems.

The SyncBus is a 3.3V CMOS signaling level, NOT 5V compliant tri-state bus. The SyncBus can be used to trigger an analog front-end, or to receive signaling.

MLVDSBUS0A	1	2	MLVDSBUS0B
SyncBus0	3	4	GND
SyncBus1	5	6	GND
SyncBus2	7	8	GND
MLVDSBUS1A	9	10	MLVDSBUS1B

Table 2.2.3.

2.2.4. Factory used connectors (CN1, CN5)

The CN1 connector is used to program the on-board CPLD, while the CN5 is used for FPGA programming via JTAG port. See the jumper settings JP3 and JP4.

2.2.5. JTAG Emulator Connector – CN2

Using this connector the PCDSP6 DSPs can be debugged by JTAG emulator hardware supplied by several manufacturers. It is compatible with Texas Instruments XDS510 emulator with 3V cable.

TMS	1	2	TRST
TDI	3	4	GND
+3.3V	5	6	Key
TDO	7	8	GND
TCK	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1

Table 2.2.5.

3. Address Ranges of PCDSP6

The board resources can be accessed from the DSP side or from the PCI side. All resources can be accessed from both sides.

3.1. PCI Bus address ranges

The board has a PCI to PCI bridge with two on-board PCI bus master interfaces in the Ti DSPs.

The PCI port has full visibility into the DSP memory maps through three base address registers pro DSPs:

- Base 0: 4M-byte prefetchable maps to all of DSP memory with the DSP page register (DSPP). Prefetch reads have all bytes valid.
- Base 1: 8M-byte nonprefetchable maps to DSP memory-mapped registers. Non-prefetch supports byte enables.
- Base 2: 16-byte I/O contains I/O registers for the PCI host

These three registers belong to the group of PCI configuration registers.

PCI host accesses to DSP (prefetchable) memory are mapped to a 4M-byte window in the PCI memory space. The PCI port contains a PCI I/O register, the DSP page register (DSPP), that specifies the address mapping from the PCI address to the DSP address. This address mapping is used when the DSP is a slave on the PCI local bus.

The DSPP, is used to locate the 4M-byte window within the DSP memory map. Bits 21-0 of the PCI address are concatenated with bits 9-0 of DSPP to form the DSP address for PCI slave access to the DSP.

The PCI base 1 register on the DSP is configured for an 8M-byte nonprefetchable region. This memory is mapped into the DSP at a fixed location (0180 0000h – 01FF 0000h). Bits 22-0 of the PCI address are concatenated with a fixed offset to map the base 1 access into the memory-mapped registers. The top 9 address bits are 0000 0001 1.

Base Address Register 2 is configured for a 16-byte I/O region for the PCI host to access the PCI I/O registers:

PCI Address	DSP address	Base 1 offset	Function
I/O Base Address + 00h	0x01C1 FFF0	0x41 FFF0	Host status register (HSR)
I/O Base Address + 04h	0x01C1 FFF4	0x41 FFF4	Host-to-DSP control register (HDCR)
I/O Base Address + 08h	0x01C1 FFF8	0x41 FFF8	DSP page register (DSPP)
I/O Base Address + 0Ch	Reserved	Reserved	Reserved

Table 3.1.

These registers can be accessed via Base 1 register region according to the Table 3.1.

The PCI bus interface provides two access methods for PCI host access to DSP memory. The 4M-byte base 0 region is used for prefetchable data, and the 8M-byte base 1 region is used for non-prefetchable (register) access. All transfers to the non-prefetchable region transfer single words and then disconnect. Data access to the prefetchable region may be transferred in bursts limited mainly by the host system setup (PCI bridge latency timer, burst length count). Prior to transferring data, the PCI host must first write DSPP to locate the 4 Mbyte window within the DSP memory map. PCI master transactions issued by the DSP will attempt to use bursts. Through disconnects, however, the external slave can force the DSP master to perform single-word transfers. Internal to the DSP, all data transfers are handled by the auxiliary channel of the DMA controller.

For more detailed description please use SPRU581b.pdf Ti documentation.

3.2 DSP address ranges

The boot modes of the both DSPs are set to PCI boot mode.

The detailed memory map of the DSPs of PCDSP6 is on the Table 3.2.1. All I/O peripherals of the board is mapped into the memory regions of the DSPs according to the Table 3.2.1.

DSP	EMIF	Chip enable	Installed Memory
1	EMIFA	CE0	*Synchronous SDRAM interface* 128MB SDRAM 125MHz bus speed
		CE1	*Not used*
		CE2	*Not used*
		CE3	*Not used*
	EMIFB	CE0	*8 bit asynchronous interface:* DSP identification Digital Pot tuning FPGA programming area Board Setup Mailbox Register DDS Register access Interrupt configuration and command
		CE1	*8 bit asynchronous interface:* E1 interfaces
		CE2	*16 bit asynchronous interface:* Base-band A/D D/A
		CE3	*16 bit synchronous interface:* High-speed A/D Two-port memory
2	EMIFA	CE0	*Synchronous SDRAM interface* 128MB SDRAM 125MHz bus speed
		CE1	*Not used*
		CE2	*Not used*
		CE3	*Not used*
	EMIFB	CE0	DSP identification Mailbox Register Interrupt configuration and command
		CE1	*8 bit asynchronous interface:* E1 interfaces
		CE2	*16 bit Asynchronous interface:* Base-band A/D D/A
		CE3	*16 bit synchronous interface:* High-speed A/D Two-port memory

Table 3.2.1.

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Size (Bytes)	Description of Memory
0000 0000–000F FFFF	DSPP=0, 00 0000–0F FFFF	-	1M	Internal RAM L2
0010 0000–017F FFFF	-	-	23M	Reserved
0180 0000–0183 FFFF	DSPP=006 00 0000–3F FFFF	00 0000–03 FFFF	256K	External Memory Interface A- EMIFA registers
0184 0000–0187 FFFF	DSPP=006 04 0000–7F FFFF	04 0000–07 FFFF	256K	L2 registers
0188 0000–018B FFFF	DSPP=006 08 0000–BF FFFF	08 0000–0B FFFF	256K	HPI registers
018C 0000–018F FFFF	DSPP=006 0C 0000–FF FFFF	0C 0000–0F FFFF	256K	McBSP 0 registers
0190 0000–0193 FFFF	DSPP=006 04 0000–7F FFFF	10 0000–13 FFFF	256K	McBSP 1 registers
0194 0000–0197 FFFF	DSPP=006 14 0000–17 FFFF	14 0000–17 FFFF	256K	Timer 0 registers
0198 0000–019B FFFF	DSPP=006 18 0000–1B FFFF	18 0000–1B FFFF	256K	Timer 1 registers
019C 0000–019F FFFF	DSPP=006 1C 0000–1F FFFF	1C 0000–1F FFFF	256K	Interrupt selector registers
01A0 0000–01A3 FFFF	-	20 0000–23 FFFF	256K	EDMA RAM and registers
01A4 0000–01A7 FFFF	-	24 0000–27 FFFF	256K	McBSP2 registers
01A8 0000–01AB FFFF	-	24 0000–27 FFFF	256K	External Memory Interface B EMIFB registers
01AC 0000–01AF FFFF	-	24 0000–28 FFFF	256K	Timer2 registers
01B0 0000–013F FFFF	-	29 0000–2F FFFF	256K	GPIO registers
01B4 0000–01B7 FFFF	-	30 0000–33 FFFF	256K	UTOPIA registers
01B8 0000–01BB FFFF	-	34 0000–37 FFFF	256K	TCP/VCP registers
01BC 0000–01BF FFFF	-	38 0000–41 FFFF	256K	Reserved
01C0 0000–01C3 FFFF	-	42 0000–45 FFFF	256K	PCI registers
01C4 0000–01FF FFFF	-	-	4M-256K	Reserved
0200 0000–0200 0033	DSPP=008 00 0000–3F FFFF	-	52	QDMA registers
0200 0034–2FFF FFFF	-	-	736M-52	Reserved
3000 0000–33FF FFFF	DSPP=0C0 00 0000–3F FFFF ..	-	64M	McBSP0 Data
3400 0000–37FF FFFF	DSPP=0D0 00 0000–3F FFFF ..	-	64M	McBSP1 Data
3800 0000–3BFF FFFF	DSPP=0E0 00 0000–3F FFFF ..	-	64M	McBSP2 Data Not used

3C00 0000–3FFF FFFF	DSPP=0F0 00 0000–3F FFFF ..	-	64M	Utopia queues Not used
4000 0000–4FFF FFFF	-	-	256M	Reserved
5000 0000–5FFF FFFF	DSPP=140 00 0000–3F FFFF ..	-	256M	TCP/VCP
6000 0000–63FF FFFF	DSPP=180 00 0000–00 8FFF	-	64M 32KB is used	External memory interface EMIFB CE0 as 8bit wide asynchronous *CPLD and FPGA implemented controlregisters FPGA programming area*
6400 0000–67FF FFFF	DSPP=190 00 0000–00 1FF	-	64M 512B is used	External memory interface EMIFB CE1 as 8bit wide asynchronous *E1 interfaces*
6800 0000–6BFF FFFF	DSPP=1A0 00 0000–00 FFFF	-	64M 64KB is used	External memory interface - EMIFB CE2 as 16bit wide asynchronous *A/D-D/A*
6C00 0000–6FFF FFFF	DSPP=1B0 00 0000–00 FFFF	-	64M 64KB is used	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D FIFOs Two-port memory*
7000 0000–7FFF FFFF	-	-	256M	Reserved
8000 0000–87FF FFFF	DSPP=200.. 21F 00 0000–3F FFFF	-	128M	External memory interface EMIFA CE0 *128MB SDRAM*
8800 0000–8FFF FFFF	-	-	128M	*Not used*
9000 0000–9FFF FFFF	DSPP=240 00 0000–3F FFFF	-	256M	External memory interface EMIFA CE1 *Not used*
A000 0000–AFFF FFFF	DSPP=280 00 0000–3F FFFF	-	256M	External memory interface EMIFA CE2 *Not used*
B000 0000–BFFF FFFF	DSPP=2C0 00 0000–FF FFFF	-	256M	External memory interface EMIFA CE3 *Not used*
C000 0000–FFFF FFFF	-	-	1G	Reserved

Table 3.2.2. TMS320C6416T Memory Map Summary (For both DSP1 and DSP2)

4. EMIFA and EMIFB initialization of the PCDSP6

After power up the board needs initialization for EMIFA and EMIFB of DSPs and FPGA. The EMIF registers must be initialized first.

0180 0000–0183 FFFF	256K	External Memory Interface EMIFA registers for CE0 - SDRAM settings
01A8 0000–01AB FFFF	256K	External Memory Interface EMIFB registers for CE0.. CE3 settings

Table 4.1.

The PCDSP6 EMIFA registers are listed in Table 4.2.

Byte Address	Register Name	Initial setup in PCDSP6 100MHz AECLKOUT1
0180 0000h	EMIFA global control	0001 0038h
0180 0004h	EMIFA CE1 space control	Not used, leave reset status
0180 0008h	EMIFA CE0 space control	0000 00D0h
0180 000Ch	Reserved	Reserved
0180 0010h	EMIFA CE2 space control	Not used, leave reset status
0180 0014h	EMIFA CE3 space control	Not used, leave reset status
0180 0018h	EMIFA SDRAM control (SDCTL)	6311 6000h (after SDEXT programming)
0180 001Ch	EMIFA SDRAM timing register (SDTIM)	0030 D30Dh
0180 0020h	EMIFA SDRAM extension register (SDEXT)	0005 4539h
0180 0024h 0180 003Ch	Reserved	-
0180 0040h	EMIFA Peripheral device transfer control (PDTCTL)	Not used, leave reset status
0180 0044h	EMIFA SDRAM secondary control register (CESEC1)	Not used, leave reset status
0180 0048h	EMIFA SDRAM secondary control register (CESEC0)	Not used, leave reset status
0180 004Ch	Reserved	Not used, leave reset status
0180 0050h	EMIFA SDRAM secondary control register (CESEC2)	Not used, leave reset status
0180 0054h	EMIFA SDRAM secondary control register (CESEC3)	Not used, leave reset status
0180 0058h 0183 FFFFh	Reserved	-

Table 4.2.

Byte Address	Register Name	Initial setup in PCDSP6 100MHz BECLKOUT1
01A8 0000h	EMIFB global control	0005 07B8h
01A8 0004h	EMIFB CE1 space control	12A1 8A03h
01A8 0008h	EMIFB CE0 space control	2122 8402h
01A8 000Ch	Reserved	Reserved
01A8 0010h	EMIFB CE2 space control	1151 4511h
01A8 0014h	EMIFB CE3 space control	0000 00B0h
01A8 0018h	EMIFB SDRAM control (SDCTL)	Not used, leave reset status
01A8 001Ch	EMIFB SDRAM timing register (SDTIM)	Not used, leave reset status
01A8 0020h	EMIFB SDRAM extension register (SDEXT)	Not used, leave reset status
01A8 0024h 01A8 003Ch	Reserved	-
01A8 0040h	EMIFB Peripheral device transfer control (PDTCTL)	Not used, leave reset status
01A8 0044h	EMIFB SDRAM secondary control register (CESEC1)	Not used, leave reset status
01A8 0048Ch	EMIFB SDRAM secondary control register (CESEC0)	Not used, leave reset status
01A8 004Ch	Reserved	Not used, leave reset status
01A8 0050h	EMIFB SDRAM secondary control register (CESEC2)	Not used, leave reset status
01A8 0054h	EMIFB SDRAM secondary control register (CESEC3)	0000 0071h
01A8 0058h 01 AB FFFFh	Reserved	-

Table 4.3.

4.1. The EMIFA initialization

4.1.1. The EMIFA global control register

The EMIF global control register (shown in Figure 4.1.1.) configures parameters common to all EMIFA CE spaces.

31	20	19			18	17	16
Reserved		EK2RATE				EK2HZ	EK2EN
0000 0000 0000		00				0	1

15	14	13	12	11	10	9	8
Rsv	Rsv	BRMODE	Rsv	BUSREQ	ARDY	HOLD	HOLDA
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
NO HOLD	EK1HZ	EK1EN	CLK4EN	CLK6EN	Rsv	Rsv	Rsv
0	0	1	1	1	0	0	0

Figure 4.1.1. EMIFA Global Control Register

Field	Description
EK2RATE	0-3h ECLKOUT2 rate. ECLKOUT2 runs at: FULLCLK 0h 1× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. HALFCLK 1h 1/2× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. QUADCLK 2h 1/4× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. - 3h Reserved. PCDSP6: ECLKIN: 0h
EK2HZ	ECLKOUT2 high-impedance control bit. CLK 0 ECLKOUT2 continues clocking during Hold (if EK2EN = 1) HIGHZ 1 ECLKOUT2 is in high-impedance state during Hold. PCDSP6: EK2HZ = 0 for continues clocking
EK2EN	. ECLKOUT2 enable bit. DISABLE 0 ECLKOUT2 is held low. ENABLE 1 ECLKOUT2 is enabled to clock. PCDSP6: EK2EN = 1 for continues clocking
BRMODE	Bus request mode (BRMODE) bit indicates if BUSREQ shows memory refresh status. MSTATUS 0 BUSREQ indicates memory access pending or in progress. MRSTATUS 1 BUSREQ indicates memory access or refresh pending or in progress. PCDSP6: BUSREQ is not used, BRMODE = 0.
BUSREQ	Bus request (BUSREQ) output bit indicates if the EMIF has an access/refresh pending or in progress. LOW 0 BUSREQ output is low. No access/refresh pending. HIGH 1 BUSREQ output is high. Access/refresh pending or in progress. PCDSP6: BUSREQ is not used, BUSREQ = 0.
ARDY	ARDY = 0: ARDY input is low. ARDY = 1: ARDY input is high.
HOLD	HOLD = 0: HOLD input is low. HOLD = 1: HOLD input is high. PCDSP6 : always high
HOLDA	HOLDA = 0: HOLDA output is low. HOLDA = 1: HOLDA output is high.

	PCDSP6: HOLDA is not used
NOHOLD	External HOLD disable NOHOLD = 0: hold enabled NOHOLD = 1: hold disabled PCDSP6: NOHOLD = 1: hold disabled
EK1HZ	. ECLKOUT1 high-impedance control bit. CLK 0 ECLKOUT1 continues clocking during Hold (if EK1EN = 1). HIGHZ 1 ECLKOUT1 is in high-impedance state during Hold. PCDSP6: EK1HZ = 0 continues clocking during Hold (if EK1EN = 1).
EK1EN	ECLKOUT1 enable bit. DISABLE 0 ECLKOUT1 is held low. ENABLE 1 ECLKOUT1 is enabled to clock. PCDSP6: EK1EN = 1, ECLKOUT1 is enabled to clock.
CLK4EN	CLKOUT4 enable bit. CLKOUT4 pin is muxed with GP1 pin. Upon exiting reset, CLKOUT4 is enabled and clocking. After reset, CLKOUT4 may be configured as GP1 via the GPIO enable register (GPEN). DISABLE 0 CLKOUT4 is held high. ENABLE 1 CLKOUT4 is enabled to clock. PCDSP6: CLK4EN = 1 CLKOUT4 is enabled to clock.
CLK6EN	CLKOUT 6 enable bit. CLKOUT6 pin is muxed with GP2 pin. Upon exiting reset, CLKOUT6 is enabled and clocking. After reset, CLKOUT6 may be configured as GP2 via the GPIO enable register (GPEN). DISABLE 0 CLKOUT6 is held high. ENABLE 1 CLKOUT6 is enabled to clock. PCDSP6: CLK6EN = 1 CLKOUT6 is enabled to clock.

The valid value of EMIFA Global Control Register in PCDSP6:

Byte Address	Name	100MHz AECLKOUT1/2
0180 0000h	EMIFA global control	0001 0038h

4.1.2. The EMIFA CE Space control registers

The four CE space control registers have the same bit structure:

31	28	27	22	21	20	19	16
Write setup		Write strobe		Write hold		Read setup	
RW, -1111		RW, -11 1111		RW, -11		RW, -1111	

15 14	13	8	7	4	3	2	0
Reserved	Read strobe		MTYPE		WRHLDMSB	Read hold	
RW,-00	RW, -11 1111		RW, +0000		R, +00	RW, +011	

Note: R = Read, W = Write, +0 =Reset value

Field	Description
Read setup Write setup	Setup width. Number of ECLKOUT1 clock cycles of setup time for address (EA), chip enable (CE), and byte enables (BE[0-3]) before read strobe or write strobe falls. For asynchronous read accesses, this is also the setup time of AOE before ARE falls.
Read strobe Write strobe	Strobe width. The width of read strobe (ARE) and write strobe (AWE) in ECLKOUT1 clock cycles
Read hold Write hold	Hold width. Number of ECLKOUT1 clock cycles that address (EA) and byte strobes (BE[0-3]) are held after read strobe or write strobe rises. For asynchronous read accesses, this is also the hold time of AOE after ARE rising.
MTYPE	Memory type of the corresponding CE spaces for PCDSP6 MTYPE = Dh :64-bit SDRAM (at CE0)

4.1.2.1. SDRAM interface initialization (CE0)

The EMIF CE Space control register of CE0 is assigned to 64bit 128MB SDRAM interface.

0180 0008h	EMIF CE0 space control

In the case that MTYPE is set to SDRAM (MTYPE=1001), the remaining field of the CE the space control register does not have any effect.

31	28	27		22	21	20	19		16
Write setup		Write strobe			Write hold		Read setup		
0000		000000			00		0000		

15 14	13		8	7	4	3	2		0
Reserved	Read strobe			MTYPE		WRHLDMSB	Read hold		
00	000000			1101		0	000		

Note: R = Read, W = Write, +0 =Reset value

So the valid value of CE0 Space control register in PCDSP6:

Byte Address	Name	100MHz AECLKOUT1/2
0180 0008h	EMIF CE0 space control	0000 00D0h

4.1.3. The EMIFA SDRAM control register (SDCTL) initialization

The SDRAM control register controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of the associated CE space control register. The SDRAM type: MT48LC16M16A2TG-75

The fields in this register are:

31	30	29 28	27……..26	25	24	23 20	19 16
Reserved	SDBSZ	SDRSZ	SDCSZ	RFEN	INIT	TRCD	TRP
0	1	10	00	1	1	0001	0001

15	12	11		1	0
TRC		Reserved		SLFRFR	
0110		0000 0000 000		0	

Field	Description	Value in PCDSP6 dec-bin – 100MHz AECLOKOUT1
SDBSZ	SDRAM bank size bit. 2BANKS　0　One bank-select pin (two banks). 4BANKS　1　Two bank-select pins (four banks).	1 - 1
SDRSZ	0-3h　SDRAM row size bits. 11ROW　　0　　11row address pins (2048 rows per bank). 12ROW　　1h　　12 row address pins (4096 rows per bank). 13ROW　　2h　　13 row address pins (8192 rows per bank). -　　　3h　　Reserved	2 - 10
SDCSZ	0-3h　SDRAM column size bits. 9COL　　0　　9 column address pins (512 elements per row). 8COL　　1h　　8 column address pins (256 elements per row). 10COL　　2h　　10 column address pins (1024 elements per row). - 3h　Reserved	0 - 00
RFEN	Refresh enable bit. If SDRAM is not used, be sure RFEN = 0; otherwise, BUSREQ may become asserted when SDRAM timer counts down to 0. DISABLE 0 SDRAM refresh is disabled. ENABLE 1 SDRAM refresh is enabled.	1 – 1
INIT	INIT Initialization bit. This write-only bit forces initialization of all SDRAM present. Reading this bit returns an undefined value. NO　　0 No effect. YES　　1 Initialize SDRAM in each CE space configured for SDRAM. The CPU should initialize all of the CE space control registers and SDRAM extension register before setting INIT = 1.	1 – 1 (0->1)
TRC	Specifies the t_{RC} value of the SDRAM in AECLKOUT1 clock cycles TRC = t_{RC}/p − 1 (p: AECLKOUT1 period: 10ns, = t_{RC}=66ns)	6 – 0110
TRP	Specifies the t_{RP} value of the SDRAM in AECLKOUT1 cycles TRP = t_{RP}/p − 1 (t_{RP}=20ns)	1 – 0001
TRCD	Specifies the t_{RCD} value of the SDRAM in AECLKOUT1 cycles TRCD = t_{RCD}/p − 1 (t_{RCD}=20ns)	1 - 0001
RFEN	Refresh enable	1 - 1

	RFEN = 0: SDRAM refresh disabled RFEN = 1: SDRAM refresh enabled	
SLFRFR	Self-refresh mode, if SDRAM is used in the system: DISABLE 0 Self-refresh mode is disabled. ENABLE 1 Self-refresh mode is enabled.	0 - 0

So the valid value of EMIF SDRAM control register in PCDSP6:

Byte Address	Name	100MHz AECLKOUT1/2
0180 0018h	EMIFA SDRAM control SDCTL	6311 6000h

4.1.4. The EMIFA SDRAM timing register (SDTIM) initialization

The SDRAM timing register controls SDRAM refresh period.
The fields in this register are:

31 26	25 24	23 12	11 0
Reserved	XRFR	CNTR	PERIOD
0000 00	00	0011 0000 1101	0011 0000 1101

Field	Description	Value in PCDSP6 dec-bin
XRFR	Extra refreshes controls the number of refreshes performed to SDRAM when the refresh counter expires. 0 1 refresh. 1h 2 refreshes. 2h 3 refreshes. 3h 4 refreshes	0 -00
CNTR	Current value of the refresh counter.	
PERIOD	Refresh period in EMIF clock cycles. $PERIOD = t_{trefresh}/t_{CYC} = 64msec/8192 = 7.8us$	781 – 30D

So the valid value of EMIF SDRAM timing register in PCDSP6:

Byte Address	Name	100MHz AECLKOUT1/2
0180 001Ch	EMIFA SDTIM	0030 D30Dh

4.1.5. The EMIFA SDRAM extension register (SDEXT) initialization

The SDRAM extension register (SDEXT) allows programming of many parameters of SDRAM. The programmability offers two distinct advantages:

Allows an interface to a wide variety of SDRAMs and is not limited to a few configurations or speed characteristics.

Allows the EMIF to maintain seamless data transfer from external SDRAM due to features like hidden precharge and multiple open banks.

It should be noted that the SDRAM control register (SDCTL) must be set after configuring SDEXT.

Field name	Formula	Values from SDRAM Data Sheet (/t_{CYC}=10ns)	Value calculated
TCL	TCL=t_{CL}-2	CL=3	1
TRAS	TRAS=(t_{RAS}/t_{CYC})-1	t_{RAS}=44ns	4
TRRD	TRRD=(t_{RRD}/t_{CYC})-2	t_{RRD}=15ns	1
TWR	TWR=(t_{WR}/t_{CYC})-1	t_{WR}=17.5ns	1
THZP	THZP=t_{HZP}-1	t_{HZP}=3cycles	2

The fields in this register are:

31	21	20	19 18	17	16 15	14 12
Reserved		WR2RD	WR2DEAC	WR2WR	R2WDQM	RD2WR
0000 0000 000		0	01	0	10	100

11 10	9	8 7	6 5	4	3 1	0
RD2DEAC	RD2RD	THZP	TWR	TRRD	TRAS	TCL
01	0	10	01	1	100	1

Field	Description	Value in PCDSP6 dec-bin -
WR2RD	0-1 Specifies minimum number of cycles between WRITE to READ command of the SDRAM in ECLKOUT cycles. WR2RD = (# of cycles WRITE to READ) – 1	0 -0
WR2DEAC	0-3h Specifies minimum number of cycles between WRITE to DEAC/DCAB command of the SDRAM in ECLKOUT cycles. WR2DEAC = (# of cycles WRITE to DEAC/DCAB) - 1	1 - 01
WR2WR	0-1 Specifies minimum number of cycles between WRITE to WRITE command of the SDRAM in ECLKOUT cycles. WR2WR = (# of cycles WRITE to WRITE) - 1	0 - 0
R2WDQM	0-3h Specifies number of of cycles that BEx signals must be high preceding a WRITE interrupting a READ. R2WDQM = (# of cycles BEx high) – 1	2 - 10
RD2WR	0-7h Specifies number of cycles between READ to WRITE command of the SDRAM in ECLKOUT cycles RD2WR = (# of cycles READ to WRITE) – 1	4 - 100
RD2DEAC	0-3h Specifies number of cycles between READ to DEAC/DCAB of the SDRAM in ECLKOUT cycles RD2DEAC = (# of cycles READ to DEAC/DCAB) - 1	1 - 01
RD2RD	Specifies number of cycles between READ to READ command (same CE space) ofthe SDRAM in ECLKOUT cycles 0 READ to READ = 1 ECLKOUT cycle. 1 READ to READ = 2 ECLKOUT cycle.	0 – 0

THZP	0-3h Specifies tHZP (also known as tROH) value of the SDRAM in ECLKOUT cycles THZP = tHZP / tcyc – 1	2 - 10
TWR	0-3h Specifies tWR value of the SDRAM in ECLKOUT cycles. TWR = tWR / tcyc - 1	1 - 01
TRRD	Specifies tRRD value of the SDRAM in ECLKOUT cycles 0 TRRD = 2 ECLKOUT cycles. 1 TRRD = 3 ECLKOUT cycles.	1 - 1
TRAS	0-7h Specifies tRAS value of the SDRAM in ECLKOUT cycles TRAS = tRAS / tcyc - 1	4 -100
TCL	Specified CAS latency of the SDRAM in ECLKOUT cycles 0 CAS latency = 2 ECLKOUT cycles. 1 CAS latency = 3 ECLKOUT cycles.	1 - 1

So the valid value of EMIF SDEXT register in PCDSP6:

Byte Address	Name	100MHz AECLKOUT1/2
0180 0020h	EMIFA SDEXT	0005 4539h

4.2. The EMIFB initialization

The EMIFB ECLKIN frequency is 100MHz, the cycle time is 10ns for both DSPs.

4.2.1. The EMIFB global control register

The EMIFB global control register (shown in Figure 4.1.1.) configures parameters common to all EMIFA CE spaces.

31		20	19				18	17	16
Reserved			EK2RATE					EK2HZ	EK2EN
0000 0000 000			01					0	1

15	14	13	12	11	10	9	8
Rsv	Rsv	BRMODE	Rsv	BUSREQ	ARDY	HOLD	HOLDA
0	0	0	0	0	1	1	1

7	6	5	4	3	2	1	0
NO HOLD	EK1HZ	EK1EN	CLK4EN	CLK6EN	Rsv	Rsv	Rsv
1	0	1	1	1	0	0	0

Figure 4.2.1.1. EMIFB Global Control Register

Field	Description
EK2RATE	0-3h ECLKOUT2 rate. ECLKOUT2 runs at: FULLCLK 0 1× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. HALFCLK 1h 1/2× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. QUARCLK 2h 1/4× EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) rate. - 3h Reserved. PCDSP6: 1/2× EMIF input clock 01h
EK2HZ	ECLKOUT2 high-impedance control bit. CLK 0 ECLKOUT2 continues clocking during Hold (if EK2EN = 1) HIGHZ 1 ECLKOUT2 is in high-impedance state during Hold. PCDSP6: EK2HZ = 0 for continues clocking
EK2EN	. ECLKOUT2 enable bit. DISABLE 0 ECLKOUT2 is held low. ENABLE 1 ECLKOUT2 is enabled to clock. PCDSP6: EK2EN = 1 for continues clocking
BRMODE	Bus request mode (BRMODE) bit indicates if BUSREQ shows memory refresh status. MSTATUS 0 BUSREQ indicates memory access pending or in progress. MRSTATUS 1 BUSREQ indicates memory access or refresh pending or in progress. PCDSP6: BUSREQ is not used, BRMODE = 0.
BUSREQ	Bus request (BUSREQ) output bit indicates if the EMIF has an access/refresh pending or in progress. LOW 0 BUSREQ output is low. No access/refresh pending. HIGH 1 BUSREQ output is high. Access/refresh pending or in progress. PCDSP6: BUSREQ is not used, BUSREQ = 0.
ARDY	ARDY = 0: ARDY input is low. ARDY = 1: ARDY input is high.
HOLD	HOLD = 0: HOLD input is low. HOLD = 1: HOLD input is high. PCDSP6 : always high
HOLDA	HOLDA = 0: HOLDA output is low.

	HOLDA = 1: HOLDA output is high.
	PCDSP6: HOLDA is not used
NOHOLD	External HOLD disable
	NOHOLD = 0: hold enabled
	NOHOLD = 1: hold disabled
	PCDSP6: NOHOLD = 1: hold disabled
EK1HZ	. ECLKOUT1 high-impedance control bit.
	CLK 0 ECLKOUT1 continues clocking during Hold (if EK1EN = 1).
	HIGHZ 1 ECLKOUT1 is in high-impedance state during Hold.
	PCDSP6: EK1HZ = 0 continues clocking during Hold (if EK1EN = 1).
EK1EN	ECLKOUT1 enable bit.
	DISABLE 0 ECLKOUT1 is held low.
	ENABLE 1 ECLKOUT1 is enabled to clock.
	PCDSP6: EK1EN = 1, ECLKOUT1 is enabled to clock.
CLK4EN	CLKOUT4 enable bit. CLKOUT4 pin is muxed with GP1 pin. Upon exiting reset, CLKOUT4 is enabled and clocking. After reset, CLKOUT4 may be configured as GP1 via the GPIO enable register (GPEN).
	DISABLE 0 CLKOUT4 is held high.
	ENABLE 1 CLKOUT4 is enabled to clock.
	PCDSP6: CLK4EN = 1 CLKOUT4 is enabled to clock.
CLK6EN	CLKOUT 6 enable bit. CLKOUT6 pin is muxed with GP2 pin. Upon exiting reset, CLKOUT6 is enabled and clocking. After reset, CLKOUT6 may be configured as GP2 via the GPIO enable register (GPEN).
	DISABLE 0 CLKOUT6 is held high.
	ENABLE 1 CLKOUT6 is enabled to clock.
	PCDSP6: CLK6EN = 1 CLKOUT6 is enabled to clock.

The valid value of EMIFB Global Control Register in PCDSP6:

Byte Address	Name	100MHz BECLKIN
01A8 0000h	EMIFB global control	0005 07B8h

4.2.2. The EMIFB CE Space control registers

The four CE space control registers have the same bit structure:

31		28	27		22	21	20	19		16
Write setup			Write strobe			Write hold		Read setup		
RW, -1111			RW, -11 1111			RW, -11		RW, -1111		

15 14		13		8	7		4	3	2		0
TA		Read strobe			MTYPE			WRHLDMSB	RDHLD		
RW,-00		RW, -11 1111			RW, +0000			R, +0	RW, +011		

Note: R = Read, W = Write, +0 =Reset value

Field	Description
Read setup Write setup	Setup width. Number of ECLKOUT1 clock cycles of setup time for address (EA), chip enable (CE), and byte enables (BE[0-3]) before read strobe or write strobe falls. For asynchronous read accesses, this is also the setup time of AOE before ARE falls.
Read strobe Write strobe	Strobe width. The width of read strobe (ARE) and write strobe (AWE) in ECLKOUT1 clock cycles
Read hold Write hold	Hold width. Number of ECLKOUT1 clock cycles that address (EA) and byte strobes (BE[0-3]) are held after read strobe or write strobe rises. For asynchronous read accesses, this is also the hold time of AOE after ARE rising.
MTYPE	Memory type of the corresponding CE spaces for PCDSP6
TA	0-3h Minimum Turn-Around time. Turn-around time controls the minimum number of ECLKOUT cycles between a read followed by a write (same or different CE spaces), or between reads from different CE spaces. Applies only to asynchronous memory types.
WRHLDMSB	0-1 Write hold width MSB is the most-significant bit of write hold.

4.2.3. EMIFB CE0 initialization - CECTL0

The EMIFB CE Space control register of CE0 is assigned to 8bit asynchronous memory interface. The FPGA programmer, the board setup area and the DDS serial interface are mapped into the EMIFB CE0. This area is only used in DSP1, and is not used in DSP2.

01A8 0008h	EMIF CE0 space control

The MTYPE is set to 8- bit asynchronous memory (MTYPE=0000).

31	28	27	22	21	20	19	16
Write setup		Write strobe		Write hold		Read setup	
0010		000100		10		0010	

15	14	13	8	7	4	3	2	0
TA		Read strobe		MTYPE		WRHLDMSB	Read hold	
10		00 0100		0000		0	010	

So the valid value of CE0 Space control register in PCDSP6:

Byte Address	Name	100MHz BECLKIN
01A8 0008h	EMIFB CE0 space control	2122 8402h

4.2.4. EMIFB CE1 initialization - CECTL1

The EMIFB CE Space control register of CE1 is assigned to 8bit asynchronous memory interface. The E1 interface chips are mapped into the EMIFB CE1. The E1 interfaces can be reached from both DSPs depending of the initialization.

01A8 0004h	EMIF CE1 space control

The MTYPE is set to 8- bit asynchronous memory (MTYPE=0000).

31	28	27	22	21	20	19	16
Write setup		Write strobe		Write hold		Read setup	
0001		0010 10		10		0001	

15	14	13	8	7	4	3	2	0
TA		Read strobe		MTYPE		WRHLDMSB	Read hold	
10		00 1010		0000		0	011	

So the valid value of CE0 Space control register in PCDSP6:

Byte Address	Name	BECLKIN=100MHz
01A8 0004h	EMIFB CE1 space control	12A1 8A03h

4.2.5. EMIFB CE2 initialization – CECTL2

The EMIFB CE Space control register of CE2 is assigned to 16bit asynchronous memory interface. The base-band A/D D/A chips are mapped into the EMIFB CE2. The A/D D/A chips can be reached from both DSPs depending of the initialization.

01A8 0010h	EMIF CE2 space control

The MTYPE is set to 16- bit asynchronous memory (MTYPE=0001).

31	28	27	22	21	20	19	16
Write setup		Write strobe		Write hold		Read setup	
0001		0001 01		01		0001	

15	14	13	8	7	4	3	2	0
TA		Read strobe		MTYPE		WRHLDMSB	Read hold	
01		00 0101		0001		0	001	

So the valid value of CE0 Space control register in PCDSP6:

Byte Address	Name	100MHz BECLKIN
01A8 0010h	EMIFB CE2 space control	1151 4511h

4.2.6. EMIFB CE3 initialization – CECTL3

The EMIFB CE Space control register of CE3 is assigned to 16bit synchronous memory interface. The high-speed A/D converter FIFOs, and the two-port memories are mapped into the EMIFB CE3. Both devices can be reached from both DSPs.

01A8 0014h	EMIF CE3 space control

The MTYPE is set to 16- bit synchronous memory (MTYPE=1011).

31	28	27	22	21	20	19	16
Write setup		Write strobe		Write hold		Read setup	
0000		0000 00		00		0000	

15 14	13	8	7	4	3	2	0
TA	Read strobe		MTYPE		WRHLDMSB	Read hold	
00	00 0000		1011		0	000	

So the valid value of CE0 Space control register in PCDSP6:

Byte Address	Name	100MHz BECLKIN
01A8 0014h	EMIFB CE3 space control	0000 00B0h

4.2.7. The EMIFB secondary control register CESEC3 initialization

This register is added for the programmable synchronous interface, and control the cycle timing of programmable synchronous memory accesses and the clock, used for synchronization for the specific CE space.

The CESEC3 is used for controlling the EMIFB CE3 synchronous interface for the high-speed A/D FIFOs, and the two-port memories. The fields in this register are:

31						16
Reserved						
0000 0000 0000 0000						

15 7	6	5	4	3 2	1 0
Reserved	SNCCLK	RENEN	CEEXT	SYNCWL	SYNCRL
0000 0000 0	1	1	1	00	01

Field	Description	Value in PCDSP6 dec-bin – 100MHz BECLKIN
SNCCLK	Synchronization clock selection bit. ECLKOUT1 0 Control/data signals for this CE space are synchronized to ECLKOUT1. ECLKOUT2 1 Control/data for this CE space are synchronized to ECLKOUT2. – 100MHz	1-1
RENEN	Read Enable enable bit. ADS 0 ADS mode. SADS/SRE signal acts as SADS signal. SADS goes active for reads, writes, and deselect. Deselect is issued after a command is completed if no new commands are pending from the EDMA. (used for SBSRAM or ZBT SRAM interface). READ 1 Read enable mode. SADS/SRE signal acts as SRE signal. SRE goes low only for reads. No deselect cycle is issued. (used for FIFO interface).	1 - 1
CEEXT	CE extension register ENABLE BIT. INACTIVE 0 CE goes inactive after the final command has been issued (not necessarily when all the data has been latched). ACTIVE 1 On read cycles, the CE signal will go active when SOE goes active and will stay active until SOE goes inactive. The SOE timing is controlled by SYNCRL. (used for synchronous FIFO reads with glue, where CE gates OE).	1 - 1
SYNCWL	0-3h Synchronous interface data write latency. 0CYCLE 0 0 cycle write latency. 1CYCLE 1h 1 cycle write latency. 2CYCLE 2h 2 cycle write latency. 3CYCLE 3h 3 cycle read latency.	0 - 00
SYNCRL	0-3h Synchronous interface data read latency. 0CYCLE 0 0 cycle read latency. 1CYCLE 1h 1 cycle read latency. 2CYCLE 2h 2 cycle read latency. 3CYCLE 3h 3 cycle read latency.	1 - 01

So the valid value of EMIF CESEC3 register in PCDSP6:

Byte Address	Name	100MHz BECLKIN
01A8 0054h	EMIFB CESEC3	0000 0071h

5. DSP memory mapped devices

5.1. FPGA programming area, board setup, DDS programming, etc. – EMIFB CE0

The EMIFB CE0 of DSP1 is an 8-bit asynchronous interface. This is used for some setup functions of the board, to program the FPGA, and to control the DDS via its serial interface.
The EMIFB CE0 area in DSP2 is only used at address 4 and 5 to decode the LED function and the doorbell function. The sign "☜ " the power up reset state.

Absolute DSP Address (hex)	EMIFB CE0, DSPP= 180 Base0 offset Address Hexa	Decoded function in DSP1/ DSP2 By CPLD/ FPGA	Function
6000 0000	00	DSP1 DSP2 CPLD	DSP identification - read only The 8 LSB bits read value of this register is 0x01 from DSP1, while 0x02 form DSP2.
6000 0001	01	DSP1 CPLD	I2C Data read/write I2C data is a 1bit wide data bus. It can be written/read via LSB bit of data bus. The power-up state of this bit is zero. ☜
6000 0002	02	DSP1 CPLD	I2C Data Bus Drive Enable - read/write Data Bus Drive Enable The I2C data bus driver 0 disabled - I2C device drives the bus ☜ 1 enabled - I2C device is driven by the CPLD
6000 0003	03	DSP1 CPLD	I2C SERCLK - read/write SERCLK is an LSB valuable register. SERCLK is the clock signal of the I2C bus. It can be written/read via LSB bit of this register. The power-up state of this bit is zero. ☜
6000 0004	04	DSP1 DSP2 CPLD	LED switch - read/write The DSP1 can switch the LED1, while DSP2 can switch the LED2. LED switch is an LSB valuable register. LED state LED 0 on ☜ 1 off
6000 0005	05	DSP1 DSP2 CPLD	Doorbell - read/write Doorbell is an 8-bit wide register (LSB byte), which can be read and written from both DSPs. This register is implemented in the nonvolatile CPLD and is ready to use after power up before FPGA programming. A write cycle of the doorbell register may generate a low to high transition on EXTINT7, generating an interrupt in the other DSP. The written data can be read by the other DSP. See address 6000 0011. The power-up state of this byte is zero. ☜
6000 0006	06	DSP1 CPLD	FPGA PROG_B - read/write FPGA PROG_B is an LSB valuable register, which is used to control the FPGA PROG_B signal. The power-up state of this bit is high. ☜

6000 0007	07	DSP1 CPLD	FPGA INIT_B - read only FPGA INIT_B is an LSB valuable register, which is used to read the FPGA INIT_B signal.
6000 0008	08	DSP1 CPLD	FPGA CS_B - read/write FPGA CS_B is an LSB valuable, which is used to control the FPGA CS_B signal. The chip select CS_B signal is active low. The power-up state of this bit is one. ☞
6000 0009	09	DSP1 CPLD	FPGA RDWR_B - read/write FPGA RDWR_B is an LSB valuable register, which is used to control the FPGA RDWR_B signal. Low means write. The power-up state of this bit is zero. ☞
6000 000A	0A	DSP1 CPLD	FPGA data port - read/write FPGA data port is an 8-bit register for writing and reading the FPGA configuration memory. The power-up state of this byte is zero. ☞
6000 000B	0B	DSP1 CPLD	FPGA BUSY - read only FPGA BUSY is an LSB valuable register, used to monitor the status of FPGA BUSY signal.
6000 000C	0C	DSP1 CPLD	FPGA DONE - read only FPGA DONE is an LSB valuable register, used to monitor the status of FPGA DONE signal. FPGA DONE goes high, when the configuration is ready.
6000 000D	0D	DSP1 CPLD	SWAOUT1 - read/write SWAOUT1 is 2 LSB bit valuable register used to control the base-band analog output signal: SWAOUT1 SWAOUT1 00 is driven by BAOUT1☞ 01 is driven. FAOUT1 10 is not driven. 11 is not driven.
6000 000E	0E	-	Not used
6000 000F	0F	DSP1 CPLD	SWAOUT2 - read/write SWAOUT2 is 2 LSB bit valuable register used to control the base-band analog output signal: SWAOUT2 SWAOUT2 00 is driven by BAOUT2☞ 01 is driven. FAOUT2 10 is not driven. 11 is not driven.
6000 0010	10	DSP1 DSP2 CPLD	NMI command - write only Writing a dummy value to this address, an NMI interrupt is generated in the DSP.
6000 0011	11	DSP1 DSP2 CPLD	EXTINT7 Doorbell WRITE register - read/write EXTINT7 Doorbell WRITE register is an LSB bit valuable register used to control the source of EXTINT7 interrupt line driving source: EXTINT7 Doorbell WRITE EXTINT7 source 0 can be driven by CTx_GPINT7☞ 1 is driven by mailbox write See Chapter 16.
…	…	…	

6000 4000	4000	DSP1 FPGA	DA1T1LT2H - read/write DA1T1LT2H is an LSB valuable register, used to assign base-band D/A1 to DSP1 or DSP2. If DA1T1LT2H = 0 the D/A1 is assigned to DSP1☜ If DA1T1LT2H = 1 the D/A1 is assigned to DSP2
6000 4001	4001	DSP1 FPGA	DA2T1LT2H - read/write DA2T1LT2H is an LSB valuable register, used to assign base-band D/A2 to DSP1 or DSP2. If DA2T1LT2H = 0 the D/A2 is assigned to DSP1☜ If DA2T1LT2H = 1 the D/A2 is assigned to DSP2
6000 4002	4002	DSP1 FPGA	F1T1LT2H - read/write F1T1LT2H is an LSB valuable register, used to assign F1 framer to DSP1 or DSP2. If F1T1LT2H = 0 the F1 framer is assigned to DSP1☜ If F1T1LT2H = 1 the F1 framer is assigned to DSP2
6000 4003	4003	DSP1 FPGA	F2T1HT2L - read/write F2T1HT2L read/write F2T1HT2L is an LSB valuable register, used to assign F1 framer to DSP1 or DSP2. If F2T1HT2L = 1 the F2 framer is assigned to DSP1 If F2T1HT2L = 0 the F2 framer is assigned to DSP2☜
6000 4004	4004	DSP1 FPGA	F1TCLKSEL - read/write F1TCLKSEL is a 4bit (D3, D0) register, used to define F1 framer TCLK source. F1TCLKSEL F1 TCLK 0000 F1RCLK. ☜ 0001 Local 2048KHz signal 0010 SYNCBUS0 0011 SYNCBUS1. 0100 SYNCBUS2. 0101 F2RCLK.
6000 4005	4005	DSP1 FPGA	F2TCLKSEL - read/write F2TCLKSEL is a 4bit (D3, D0) register, used to define F2 framer TCLK source. F2TCLKSEL F2 TCLK 0000 F2RCLK. ☜ 0001 Local 2048KHz signal 0010 SYNCBUS0 0011 SYNCBUS1. 0100 SYNCBUS2. 0101 F1RCLK.
6000 4006	4006	DSP1 FPGA	DDSSDIO - read/write DDSSDIO is an LSB valuable register, used as a one bit wide serial data bus to control the DDS chip. The power up reset state is zero. ☜
6000 4007	4007	DSP1 FPGA	DDSSDIO_DRVENH - read/write DDSSDIO_DRVENH is an LSB valuable register, used to enable to drive the DDSDIO one bit wide bus by the FPGA. If DDSSDIO_DRVENH = 0 then the DDSDIO is driven by the DDS chip☜ If DDSSDIO_DRVENH = 1 then the DDSDIO is driven by the FPGA with the content of DDSDIO register

6000 4008	4008	DSP1 FPGA	DDSCSL - read/write DDSCSL is an LSB valuable register, used to generate the Chip select signal of the DDS chip. The power up reset state is high. ✎
6000 4009	4009	DSP1 FPGA	DDSSCLK - read/write DDSSCLK is an LSB valuable register, used to generate the serial clock signal of the DDS chip. The power up reset state is zero. ✎
6000 400A	400A	DSP1 FPGA	DDSIOUPDATE - read/write DDSIOUPDATE is an LSB valuable register, used to update of the DDS chip. After filling up the DDS registers via the serial port, using the clock and data registers, a low to high transition updates the new values. The power up reset state is zero. ✎
6000 400B	400B	DSP1 FPGA	AD1_FILTDEV - read/write The AD1_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band A/D1 input filter. The Cutoff Frequency = 125000 / (AD1_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ✎
6000 400C	400C	DSP1 FPGA	AD2_FILTDEV - read/write The AD2_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band A/D2 input filter. The Cutoff Frequency = 125000 / (AD2_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ✎
6000 400D	400D	DSP1 FPGA	DA1_FILTDEV - read/write The DA1_FILTDEV is an 8-bit register, used to define the cutoff frequency of D/A1 filter. The Cutoff Frequency = 125000 / (DA1_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ✎
6000 400E	400E	DSP1 FPGA	DA2_FILTDEV - read/write The DA2_FILTDEV is an 8-bit register, used to define the cutoff frequency of base-band D/A2 filter. The Cutoff Frequency = 125000 / (DA2_FILTDEV+1) [Hz] (The FPGA CLKIN is 50MHz) The power up reset state is 124, which means 1000Hz cutoff. ✎
6000 400F	400F	DSP1 FPGA	MLVDSBUS0_DRIVE - read/write MLVDSBUS0_DRIVE is an LSB valuable register, used to enable the drive of MLVDSBUS0 signal. If MLVDSBUS0_DRIVE = 0 then MLVDSBUS0 is not driven✎ If MLVDSBUS0_DRIVE = 1 then MLVDSBUS0 is driven by the signal which is selected by MLVDSBUS0_DRIVE_SELECT
6000 4010	4010	DSP1 FPGA	MLVDSBUS1_DRIVE - read/write MLVDSBUS1_DRIVE is an LSB valuable register, used to enable the drive of MLVDSBUS1 signal. If MLVDSBUS1_DRIVE = 0 then MLVDSBUS1 is not driven✎ If MLVDSBUS1_DRIVE = 1 then MLVDSBUS1 is driven by the signal which is selected by MLVDSBUS1_DRIVE_SELECT

6000 4011	4011	DSP1 FPGA	MLVDSBUS0_DRIVE_SELECT - read/write The MLVDSBUS0_DRIVE_SELECT is a 4-bit register, used to define the MLVDSBUS0 drive source: MLVDSBUS0_DRIVE_SELECT MLVDSBUS0 0000 DDS output signal ✆ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal 0110 DSP2 TOUT0 signal 0111 DSP2 TOUT1 signal 1000 DSP2 TOUT2 signal
6000 4012	4012	DSP1 FPGA	MLVDSBUS1_DRIVE_SELECT - read/write The MLVDSBUS1_DRIVE_SELECT is a 4-bit register, used to define the MLVDSBUS1 drive source: MLVDSBUS1_DRIVE_SELECT MLVDSBUS1 0000 DDS output signal✆ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal 0110 DSP2 TOUT0 signal 0111 DSP2 TOUT1 signal 1000 DSP2 TOUT2 signal
6000 4013	4013	DSP1 FPGA	FPGAT1T2CLKIN_SELECT - read/write The FPGAT1T2CLKIN_SELECT is a 4-bit register, used to define the FPGAT1T2CLKIN signal: FPGAT1T2CLKIN_SELECT FPGAT1T2CLKIN 0000 RBMLVDSBUS0 signal✆ 0001 RBMLVDSBUS1 signal 0010 DDS out signal
6000 4014	4014	DSP1 FPGA	HAD12CLKSEL - read/write The HAD12CLKSEL is a 4-bit register, used to define the HAD12CLK signal: HAD12CLKSEL HAD12CLK 0000 DDS out signal ✆ 0001 RCLKIN signal (50MHz) 0010 2048KHz clock signal 0011 DSP1 TOUT0 signal 0100 DSP1 TOUT1 signal 0101 DSP1 TOUT2 signal

6000 4015	4015	DSP1 DSP2 FPGA	INT4_SEL - read/write Writing this register from DSP1 means the setting of DSP1_INT4_SEL, while from the DSP2 means the setting of DSP2_INT4_SEL register. The INT4_SEL is a 4-bit register, used to define the INT4 source: INT4_SEL INT4 0000 INT4_SEND of the other DSP ☜ 0001 RBMLVDSBUS0 signal 0010 RBMLVDSBUS1 signal 0011 SYNCBUS0 signal 0100 SYNCBUS1 signal 0101 SYNCBUS2 signal 0110 AD1BUSYL signal 0111 AD2BUSYL signal 1000 FRAMER1INT signal 1001 FRAMER2INT signal 1010 HAD1OVERLOAD signal 1011 HAD2OVERLOAD signal
6000 4016	4016	DSP1 DSP2 FPGA	INT5_SEL - read/write Writing this register from DSP1 means the setting of DSP1_INT5_SEL, while from the DSP2 means the setting of DSP2_INT5_SEL register. The INT5_SEL is a 4-bit register, used to define the INT5 source: INT5_SEL INT5 0000 INT5_SEND of the other DSP ☜ 0001 RBMLVDSBUS0 signal 0010 RBMLVDSBUS1 signal 0011 SYNCBUS0 signal 0100 SYNCBUS1 signal 0101 SYNCBUS2 signal 0110 AD1BUSY signal 0111 AD2BUSY signal 1000 FRAMER1INT signal 1001 FRAMER2INT signal 1010 HAD1OVERLOAD signal 1011 HAD2OVERLOAD signal

6000 4017	4017	DSP1 DSP2 FPGA	INT6_SEL - read/write Writing this register from DSP1 means the setting of DSP1_INT6_SEL, while from the DSP2 means the setting of DSP2_INT6_SEL register. The INT6_SEL is a 4-bit register, used to define the INT6 source: INT6_SEL INT6 0000 INT6_SEND of the other DSP ☞ 0001 RBMLVDSBUS0 signal 0010 RBMLVDSBUS1 signal 0011 SYNCBUS0 signal 0100 SYNCBUS1 signal 0101 SYNCBUS2 signal 0110 AD1BUSYL signal 0111 AD2BUSYL signal 1000 FRAMER1INT signal 1001 FRAMER2INT signal 1010 HAD1OVERLOAD signal 1011 HAD2OVERLOAD signal
6000 4018	4018	DSP1 DSP2 FPGA	INT4_SEND - write only Writing a dummy data to this address generates a TINT4SEND in the other DSP.
6000 4019	4019	DSP1 DSP2 FPGA	INT5_SEND - write only Writing a dummy data to this address generates a TINT5SEND in the other DSP.
6000 401A	401A	DSP1 DSP2 FPGA	INT6_SEND - write only Writing a dummy data to this address generates a TINT6SEND in the other DSP.
6000 401B	401B	DSP1 FPGA	HAD12_FIFO_STATUS - read only Reading this 4-bit register the high-speed A/D1 and A/D2 FIFO status can be read: D3 D2 D1 D0 HAD2 Empty HAD2 Full HAD1 Empty HAD1 Full *FIFO status bits are only valid after an active write enable and FIFO write signal.*

6000 401C	401C	DSP1 FPGA	AD1CONVSTARTSEL - read/write The AD1CONVSTARTSEL is a 4-bit register, used to define the AD1CONVSTARTsource: AD1CONVSTARTSEL AD1CONVSTARTsource 0000 DSP1 SW1_START command ☞ 0001 DSP1 SW2_START command 0010 DSP2 SW1_START command 0011 DSP2 SW2_START command 0100 RBMLVDSBUS0 signal 0101 RBMLVDSBUS1 signal 0110 SYNCBUS0 signal 0111 SYNCBUS1 signal 1000 SYNCBUS2 signal 1001 DSP1 TOUT0 signal 1010 DSP1 TOUT1 signal 1011 DSP1 TOUT2 signal 1100 DSP2 TOUT0 signal 1101 DSP2 TOUT1 signal 1110 DSP2 TOUT2 signal 1111 DDS out signal
6000 401D	401D	DSP1 FPGA	AD2CONVSTARTSEL - read/write The AD2CONVSTARTSEL is a 4-bit register, used to define the AD2CONVSTARTsource: AD2CONVSTARTSEL AD2CONVSTARTsource 0000 DSP1 SW1_START command ☞ 0001 DSP1 SW2_START command 0010 DSP2 SW1_START command 0011 DSP2 SW2_START command 0100 RBMLVDSBUS0 signal 0101 RBMLVDSBUS1 signal 0110 SYNCBUS0 signal 0111 SYNCBUS1 signal 1000 SYNCBUS2 signal 1001 DSP1 TOUT0 signal 1010 DSP1 TOUT1 signal 1011 DSP1 TOUT2 signal 1100 DSP2 TOUT0 signal 1101 DSP2 TOUT1 signal 1110 DSP2 TOUT2 signal 1111 DDS out signal
6000 401E	401E	-	Not used
6000 401F	401F	-	Not used
6000 4020	4020	DSP1 FPGA	AD1MODESEL - read/write The AD1MODESEL is a 4-bit register, used to define the AD1MODE: AD1MODESEL AD1MODE 0000 A/D1 Gain = off Filter off ☞ 0001 A/D1 Gain = on Filter off 0010 A/D1 Gain = on Filter on

6000 4021	4021	DSP1 FPGA	AD2MODESEL - read/write The AD2MODESEL is a 4-bit register, used to define the AD2MODE: AD2MODESEL AD2MODE 0000 A/D2 Gain = off Filter off☜ 0001 A/D2 Gain = on Filter off 0010 A/D2 Gain = on Filter on
6000 4022	4022	DSP1 FPGA	SYNCBUS0SEL - read/write The SYNCBUS0SEL is an 8-bit register, used to define the SYNCBUS0SEL source: SYNCBUS0SEL SYNCBUS0 source 0- 0000 0000 RDDSCOMPOUT ☜ 1- 0000 0001 C2048K 2- 0000 0010 F1_RCLK 3- 0000 0011 F2_RCLK 4- 0000 0100 T1_TIMER_OUT0 5- 0000 0101 T1_TIMER_OUT1 6- 0000 0110 T1_TIMER_OUT2 7- 0000 0111 T2_TIMER_OUT0 8- 0000 1000 T2_TIMER_OUT1 9- 0000 1001 T2_TIMER_OUT2 A- 0000 1010 AD1SCCLK B- 0000 1011 AD2SCCLK C- 0000 1100 DA1SCCLK D- 0000 1101 DA2SCCLK E- 0000 1110 AD1CONVSTARTL F- 0000 1111 AD2CONVSTARTL 10-0001 0000 DA1LDACL 11-0001 0001 DA2LDACL 12-00010010 T1_GP_INT4 13-00010011 T1_GP_INT5 14-00010100 T1_GP_INT6 15-00010101 T2_GP_INT4 16-00010110 T2_GP_INT5 17-00010111 T2_GP_INT6 18-00011000 T1_GPIO8 19-00011001 T2_GPIO8 1A-00011010 F1_RCLK 1B-00011011 F2_RCLK 1C-00011100 F1_TCLK 1D-00011101 F2_TCLK 1E-00011110 T1 DSP clock freq. /6= 167MHz 1F-00011111 T2 DSP clock freq. /6= 167MHz 20-00100000 T1 DSP EMIF_B_ECLK_OUT1 21-00100001 T1 DSP EMIF_B_ECLK_OUT2 22-00100010 T2 DSP EMIF_B_ECLK_OUT1 23-00100011 T2 DSP EMIF_B_ECLK_OUT2 24-00100100 T1 DSP clock freq. /6= 167MHz 25-00100101 T2 DSP clock freq. /6= 167MHz 26-00100110 T2 DSP BSOE3

6000 4023	4023	DSP1 FPGA	SYNCBUS1SEL - read/write The SYNCBUS1SEL is an 8-bit register, used to define the SYNCBUS1SEL source: SYNCBUS1SEL SYNCBUS1 source 0- 0000 0000 RDDSCOMPOUT ☞ 1- 0000 0001 C2048K 2- 0000 0010 F1_RCLK 3- 0000 0011 F2_RCLK 4- 0000 0100 T1_TIMER_OUT0 5- 0000 0101 T1_TIMER_OUT1 6- 0000 0110 T1_TIMER_OUT2 7- 0000 0111 T2_TIMER_OUT0 8- 0000 1000 T2_TIMER_OUT1 9- 0000 1001 T2_TIMER_OUT2 A- 0000 1010 AD1SCCLK B- 0000 1011 AD2SCCLK C- 0000 1100 DA1SCCLK D- 0000 1101 DA2SCCLK E- 0000 1110 AD1CONVSTARTL F- 0000 1111 AD2CONVSTARTL 10-0001 0000 DA1LDACL 11-0001 0001 DA2LDACL 12-0001 0010 T1_GP_INT4 13-0001 0011 T1_GP_INT5 14-0001 0100 T1_GP_INT6 15-0001 0101 T2_GP_INT4 16-0001 0110 T2_GP_INT5 17-0001 0111 T2_GP_INT6 18-0001 1000 T1_GPIO8 19-0001 1001 T2_GPIO8 1A-00011010 F1_RSER 1B-00011011 F2_RSER 1C-00011100 F1_TSER 1D-00011101 F2_TSER 1E-00011110 T1 DSP clock freq. /6= 167MHz 1F-00011111 T2 DSP clock freq. /6= 167MHz 20-00100000 T1 DSP EMIF_B_ECLK_OUT1 21-00100001 T1 DSP EMIF_B_ECLK_OUT2 22-00100010 T2 DSP EMIF_B_ECLK_OUT1 23-00100011 T2 DSP EMIF_B_ECLK_OUT2 24-00100100 T1 DSP clock freq. /6= 167MHz 25-00100101 T2 DSP clock freq. /6= 167MHz 26-00100110 T2 DSP BSOE3

6000 4024	4024	DSP1 FPGA	SYNCBUS2SEL - read/write The SYNCBUS2SEL is an 8-bit register, used to define the SYNCBUS2SEL source: SYNCBUS2SEL SYNCBUS2 source 0- 0000 0000 RDDSCOMPOUT ☜ 1- 0000 0001 C2048K 2- 0000 0010 F1_RCLK 3- 0000 0011 F2_RCLK 4- 0000 0100 T1_TIMER_OUT0 5- 0000 0101 T1_TIMER_OUT1 6- 0000 0110 T1_TIMER_OUT2 7- 0000 0111 T2_TIMER_OUT0 8- 0000 1000 T2_TIMER_OUT1 9- 0000 1001 T2_TIMER_OUT2 A- 0000 1010 AD1SCCLK B- 0000 1011 AD2SCCLK C- 0000 1100 DA1SCCLK D- 0000 1101 DA2SCCLK E- 0000 1110 AD1CONVSTARTL F- 0000 1111 AD2CONVSTARTL 10-0001 0000 DA1LDACL 11-0001 0001 DA2LDACL 12-00010010 T1_GP_INT4 13-00010011 T1_GP_INT5 14-00010100 T1_GP_INT6 15-00010101 T2_GP_INT4 16-00010110 T2_GP_INT5 17-00010111 T2_GP_INT6 18-00011000 T1_GPIO8 19-00011001 T2_GPIO8 1A-00011010 F1_RSYNC 1B-00011011 F2_RSYNC 1C-00011100 F1_TSYNC 1D-00011101 F2_TSYNC 1E-00011110 T1 DSP clock freq. /6= 167MHz 1F-00011111 T2 DSP clock freq. /6= 167MHz 20-00100000 T1 DSP EMIF_B_ECLK_OUT1 21-00100001 T1 DSP EMIF_B_ECLK_OUT2 22-00100010 T2 DSP EMIF_B_ECLK_OUT1 23-00100011 T2 DSP EMIF_B_ECLK_OUT2 24-00100100 T1 DSP clock freq. /6= 167MHz 25-00100101 T2 DSP clock freq. /6= 167MHz 26-00100110 T2 DSP BSOE3
6000 4025	4025	DSP1 FPGA	SYNCBUS0DRVEN - read/write SYNCBUS0DRVEN is an LSB valuable register used to control the drive source of SYNCBUS0 signal. If SYNCBUS0DRVEN = 1 then the SYNCBUS0 is driven by the SYNCBUS0SEL selected signal. If SYNCBUS0DRVEN = 0 ☜ then the SYNCBUS0 is not driven on the board. SYNCBUS0 may be driven by only one source.

6000 4026	4026	DSP1 FPGA	SYNCBUS1DRVEN - read/write SYNCBUS1DRVEN is an LSB valuable register used to control the drive source of SYNCBUS10 signal. If SYNCBUS1DRVEN = 1 then the SYNCBUS1 is driven by the SYNCBUS1SEL selected signal. If SYNCBUS1DRVEN = 0 ☞ then the SYNCBUS1 is not driven on the board. SYNCBUS1 may be driven by only one source.
6000 4027	4027	DSP1 FPGA	SYNCBUS2DRVEN - read/write SYNCBUS2DRVEN is an LSB valuable register used to control the drive source of SYNCBUS2 signal. If SYNCBUS2DRVEN = 1 then the SYNCBUS2 is driven by the SYNCBUS2SEL selected signal. If SYNCBUS2DRVEN = 0 ☞ then the SYNCBUS2 is not driven on the board. SYNCBUS2 may be driven by only one source.
6000 4028	4028	DSP1 FPGA	DA1UPDATESEL - read/write The DA1UPDATESEL is a 4-bit register, used to define the DA1UPDATE source: DA1UPDATESEL DA1UPDATE source 0000 DSP1 SW_UPDATE1 command ☞ 0001 DSP1 SW_UPDATE2 command 0010 DSP2 SW_UPDATE1 command 0011 DSP2 SW_UPDATE2 command 0100 RBMLVDSBUS0 signal 0101 RBMLVDSBUS1 signal 0110 SYNCBUS0 signal 0111 SYNCBUS1 signal 1000 SYNCBUS2 signal 1001 DSP1 TOUT0 signal 1010 DSP1 TOUT1 signal 1011 DSP1 TOUT2 signal 1100 DSP2 TOUT0 signal 1101 DSP2 TOUT1 signal 1110 DSP2 TOUT2 signal 1111 DDS out signal

6000 4029	4029	DSP1 FPGA	DA2UPDATESEL - read/write The DA2UPDATESEL is a 4-bit register, used to define the DA2UPDATE source: DA2UPDATESEL DA2UPDATE source 0000 DSP1 SW_UPDATE1 command ☜ 0001 DSP1 SW_UPDATE2 command 0010 DSP2 SW_UPDATE1 command 0011 DSP2 SW_UPDATE2 command 0100 RBMLVDSBUS0 signal 0101 RBMLVDSBUS1 signal 0110 SYNCBUS0 signal 0111 SYNCBUS1 signal 1000 SYNCBUS2 signal 1001 DSP1 TOUT0 signal 1010 DSP1 TOUT1 signal 1011 DSP1 TOUT2 signal 1100 DSP2 TOUT0 signal 1101 DSP2 TOUT1 signal 1110 DSP2 TOUT2 signal 1111 DDS out signal

☜: Power up reset Reset state

5.2. E1 Interfaces – EMIFB CE1

The Dallas 2156 E1 interfaces are mapped into the EMIFB CE1 area as 8 bit asynchronous devices. The Framer 1 is mapped into the first 256 byte, the second one is mapped into the second 256 byte area. See the E1 interface chapter. The framers can be assigned to DSP1 or DSP2. The power up assignments is the DSP1 framer1 and DSP2 Framer 2 assignments. The assignments of Framer1, and Framer2, to DSP1 or DSP2 can be set in DSP1 CE0 area.

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Size (Bytes)	Description of Memory
6400 0000–6400 00FF	DSPP=190 00 0000–00 00FF	-	256	*Framer1 E1 interface* External memory interface EMIFB CE1 as 8bit wide asynchronous memory
6400 0100–6400 01FF	DSPP=190 00 0100–00 01FF	-	256	*Framer2 E1 interface* External memory interface EMIFB CE1 as 8bit wide asynchronous memory

Table 5.2.1

5.3. Base-band A/D, D/A - EMIFB CE2

The base-band analog input/output circuitry is mapped into the EMIFB CE2 area as 16 bit asynchronous device. See the base-band analog input/output chapter. These registers are decoded in both DSP1 and DSP2. The assignment of the A/Ds and D/As are set in DSP1 CE0 area.

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 Offset Address	Size (Bytes)	Read access to memory	Write access to memory
6800 0000– 6C00 0001	DSPP=1A0 00 0000– 00 0001	-	1W 2B	*A/D1 16bit read*	*SW1_START* Writing a dummy data to this address generates an SW1_START command.
6800 0002– 6C00 0003	DSPP=0D0 00 0002– 00 0003	-	1W 2B	*A/D2 16bit read*	*SW2_START* Writing a dummy data to this address generates an SW2_START command.
6800 0004– 6C00 0005	DSPP=1A0 00 0004– 00 0005	-	1W 2B	-	*SW1/SW2_START* Writing a dummy data to this address generates a simultaneous SW1_START and SW2_START command.
6800 0006– 6C00 0007	DSPP=1A0 00 0006– 00 0007	-	-	-	-
6800 0008– 6C00 0009	DSPP=1A0 00 0006– 00 0007	-	1W 2B	*SW_UPDATE1* Reading a dummy data from this address generates an SW_UPDATE1 command.	*D/A/1 16bit write,* The upper 14 bits are valid, the code format is two's complement
6800 000A– 6C00 000B	DSPP=1A0 00 0008– 00 0009	-	1W 2B	*SW_UPDATE2* Reading a dummy data from this address generates an SW_UPDATE2 command	*D/A/1 16bit write,* The upper 14 bits are valid, the code format is two's complement
6800 000C– 6C00 000D	DSPP=1A0 00 000A8– 00 000B	-	1W 2B	*SW_UPDATE1/SW_UP DATE2* Reading a dummy data from this address generates a simultaneous SW_UPDATE1 and SW_UPDATE2 command	-

Table 5.3.1

5.4 High-speed A/D, two-port memory CE3

The high-speed analog input circuitry and the two-port memory are mapped into the EMIFB CE3 area as 16 bit synchronous devices. See the high-speed analog input circuitry and the two-port memory chapters.

DSP access Address Range	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Decoded in DSP1/ DSP2	Size (Bytes)	Description of Memory
6C00 0000–6C00 3FFF	DSPP=1B0 00 0000–00 3FFF	-	DSP1	8KW 16KB	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D1 FIFO*
6C00 4000–6C00 7FFF	DSPP=1B0 00 4000–00 7FFF	-	DSP1	8KW 16KB	External memory interface EMIFB CE3 as 16bit wide synchronous *High-speed A/D 2 FIFO*
6C00 8000–6C00 FFFF	DSPP=1B0 00 8000–00 FFFF	-	DSP1 DSP2	16KW 32KB	External memory interface EMIFB CE3 as 16bit wide synchronous *Two-port memory*

Table 5.4.1.

6. E1 interfaces

The F1 and F2 framer can be connected to T1 and/or T2 DSPs via serial ports. The T1 and T2 DSPs can reach both framers, depending the F1T1LT2H, and the F2T1HT2L control bits. The Figure 6.1. shows the connection between the F1, F2 framers and the T1 and T2 DSPs.
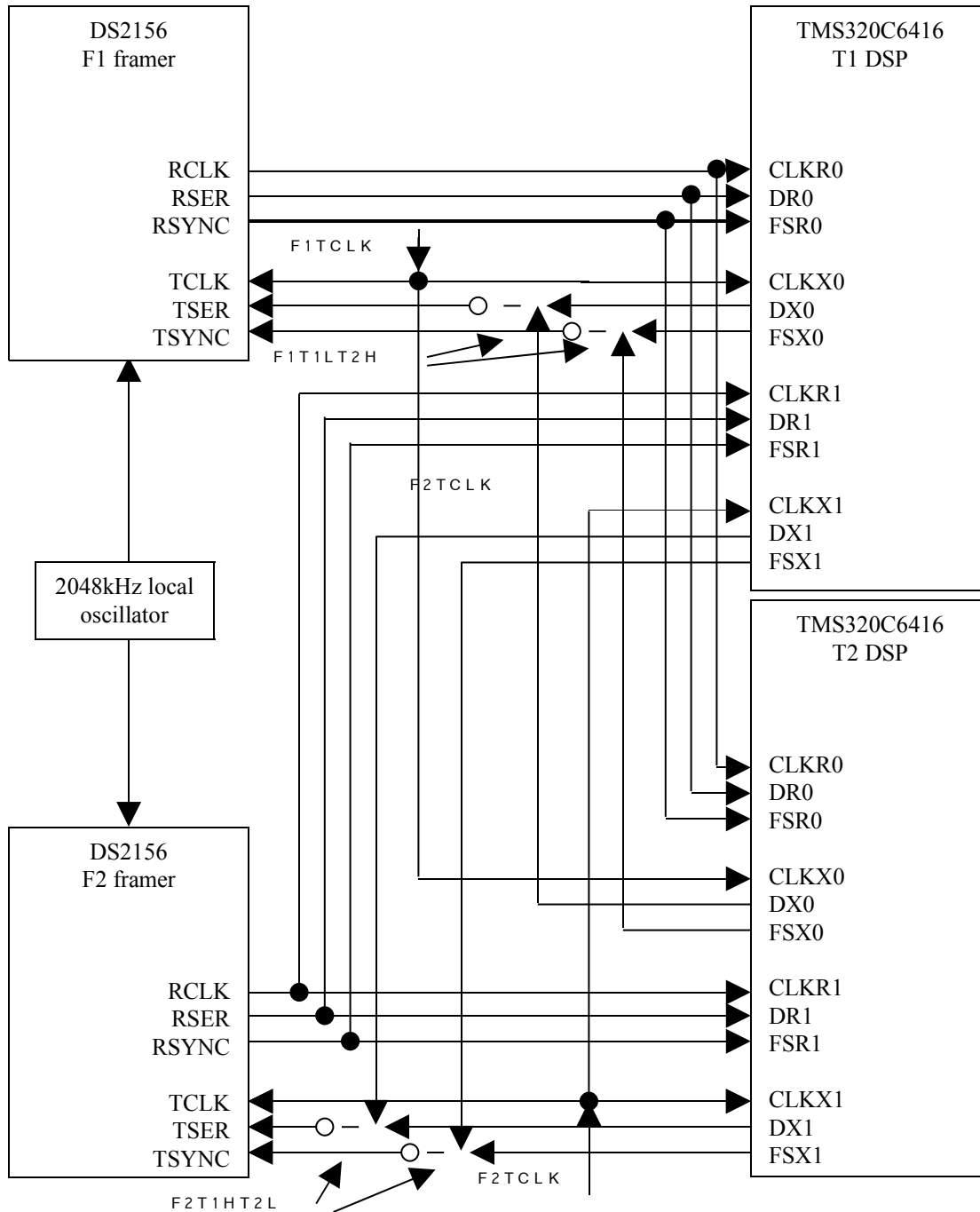
6.1. ábra

The transmitter clocks of the framers are generated according to the Figure 6.2.

SyncBusXXX

F1RCLK

F1RCLK

2048KHz Local clock

.
.
.

SyncBusXSEL

F1RCLK

2048 kHz Local clock

SyncBus0

SyncBus1

SyncBus2

F2RCLK

F1RCLK

F1TCLK

F2TCLKSEL
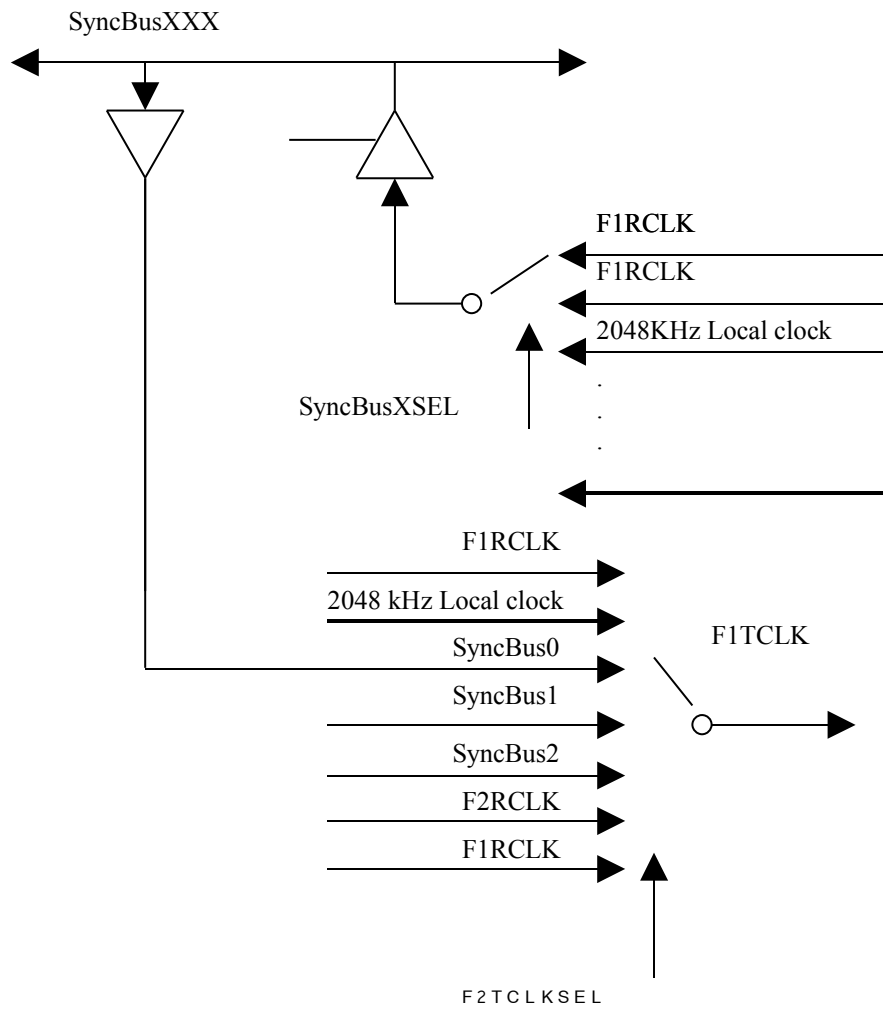
6.2. ábra

7. High-speed A/D

The conversion rate must be in the range 1MHz up to 80 MHz. The sampling – The FIFO write enable signal can be controlled from the DSP1 or leaving the GPIO8 in reset state input, it can be driven by an external signal at CN3 connector.
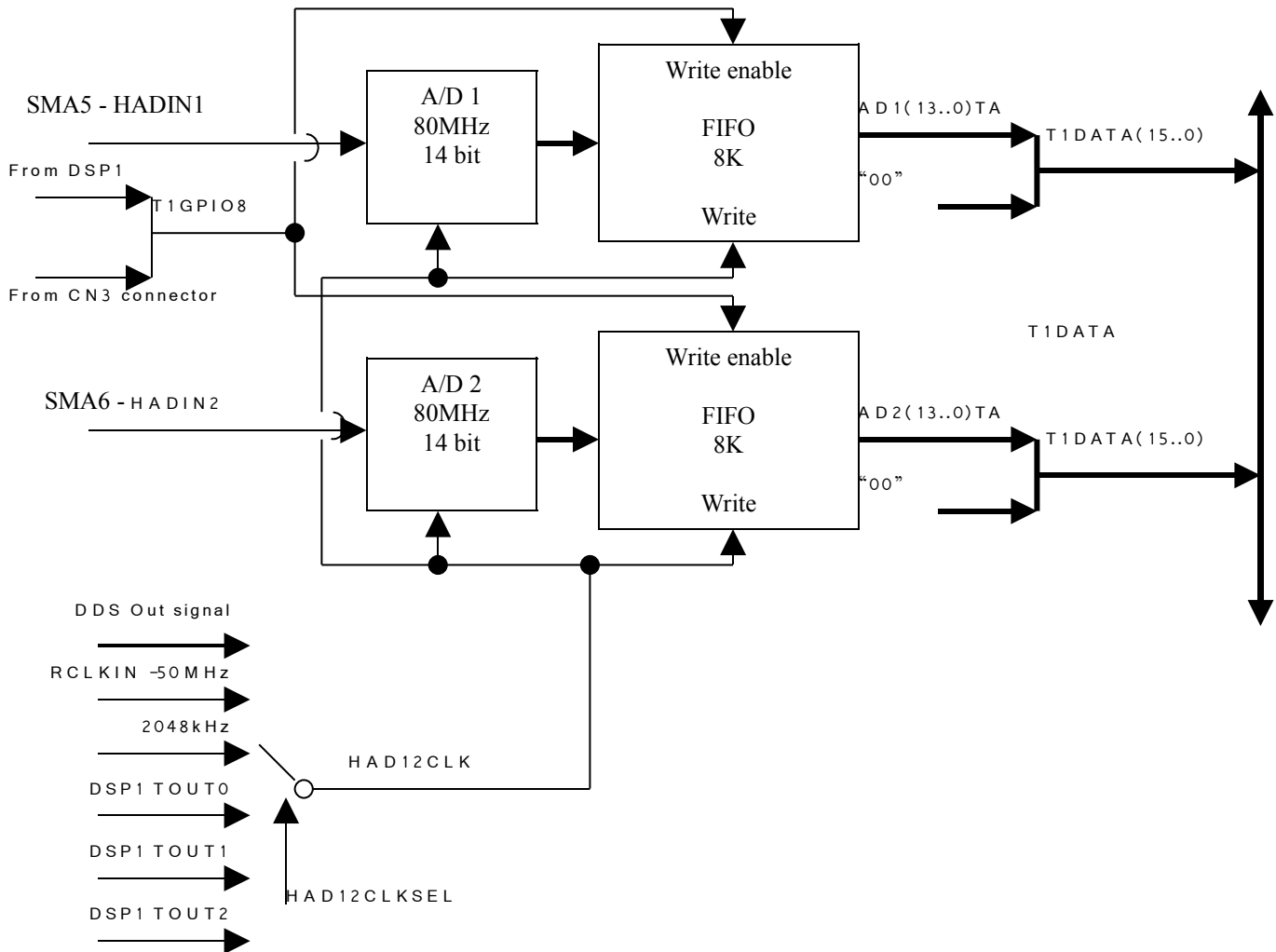
Figure 7.1.

The A/D1 and A/D2 FIFOs are mapped into the DSP1 memory map according to the Table 5.4.1. The 14 bit two's complement data is aligned to the DSP's MSB bits, while the lower two bits are always zero.

8. DDS High-speed A/D sampling clock generator

The block diagram of the DDS circuitry is on the Figure 8.1. The board has two A/D converters, with programmable cut-off frequency anti-aliasing filters.
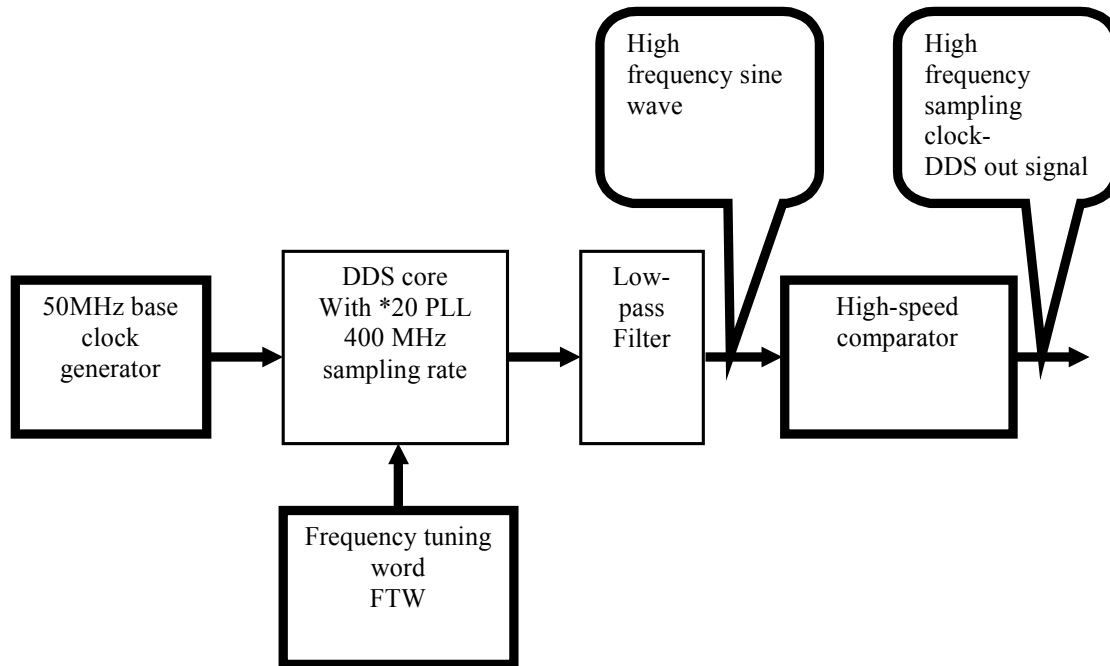
Figure 8.1.

The generated sampling frequency:

f=FTW*400MHz/4.294.967.296

So the FTW=f*4.294.967.296/400MHz

The FTW is 32 bit long. For example the maximum 80MHz sampling clock needs the FTW= 858.993.459, in hexadecimal format:3333 3333.

For the proper operation the DDS register map is according to the Table.

Register Name Serial Address	Internal byte address	Bit range	MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0
CFR1 00	00	7:0	0	0	0	0	0	0	0	0
	01	15:8	0	0	0	0	0	0	0	0
	02	23:16	0	0	0	0	0	0	0	0
	03	32:24	0	0	0	0	0	0	0	0
CFR2 01	04	7:0	0	1	0	0	0	0	0	0
	05	15:8	0	0	0	0	0	0	0	0
	06	23:16	0	0	0	0	0	0	0	0
ASF 02	07	7:0	0	0	0	0	0	0	0	0
	08	15:8	0	0	0	0	0	0	0	0
ARR 03	09	7:0	0	0	0	0	0	0	0	0
FTW 04	0A	7:0	FTW 7:0							
	0B	15:8	FTW 8:15							
	0C	23:16	FTW 23:16							
	0D	32:24	FTW 31:24							
FOW 05	0E	7:0	0	0	0	0	0	0	0	0
	0F	15:8	0	0	0	0	0	0	0	0

Table 8.1.

Use Analog Devices AD9952 data sheet to access registers via the serial port. PCDSP6 uses the serial port in two-wire mode. The serial clock signal is mapped into the DSP1 CE0 address range.

These one-bit registers can be written and read back to form the appropriate signals.
Before the write/read cycles, the DDDSCSL should be written to low.

At the end of cycle the DDSIOUPDATE low to high transition updates the register content.

9. Base-band analog inputs

The block diagram of the base-band analog input circuitry is on the Figure 9.1. The board has two input channels with programmable gain and filter.
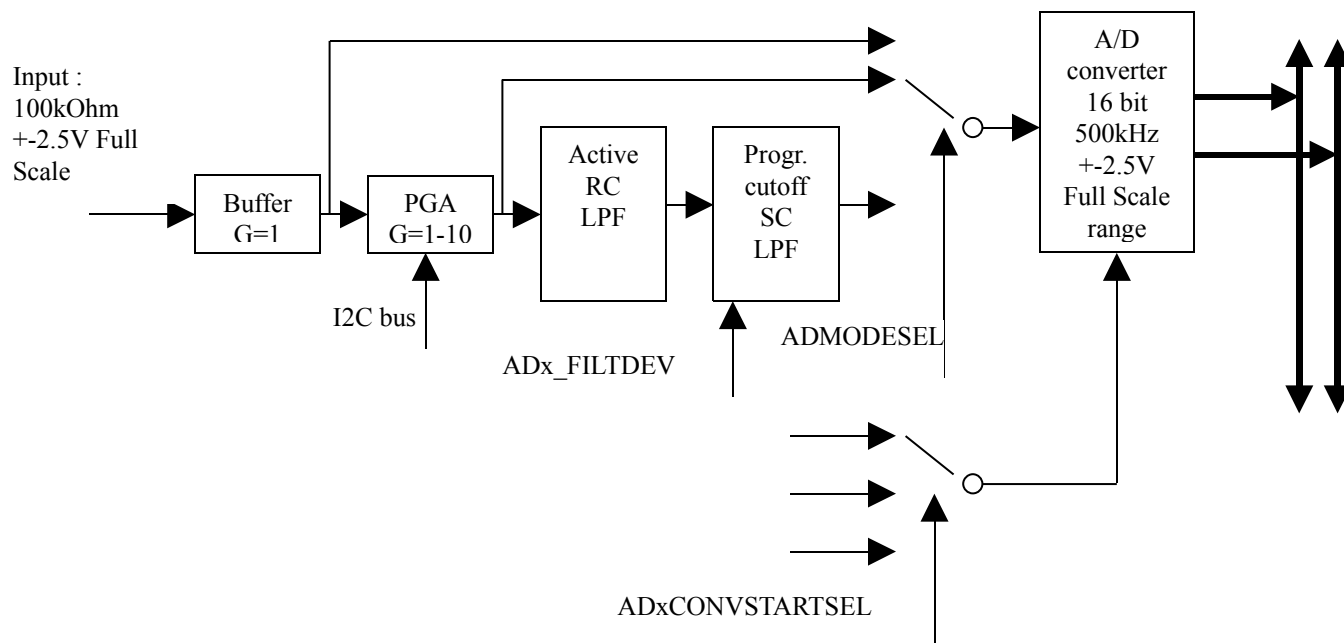
Figure 9.1

The Active RC filter is a fixed cut-off frequency LPF, and is used to band limit the input signal of SC filter. The RC filter is 4th order Butterworth LPF with –3dB gain at 30kHz. The gain error at 20kHz is smaller than 0.3dB.The programmable cut-off frequency SC filter is an 8th order elliptic filter with 0.1 dB pass-band ripple, and 60 dB stop-band attenuation. See Figure 9.2. The transition range is 600 Hz. The Table 9.1 shows some typical values of SC filters.

The A/D input signal can be selected by ADMODESEL register. The A/D conversion start signal can be selected by ADxCONVSTARTSEL register.

The converted data can be read by either the DSP1 or the DSP2.

ADxFILTDEV	SC filter Clock Frequency	Cut-off frequency	Supposing 50MHz CLKIN frequency – 1GHz DSP, the Cutoff Frequency =
4	5MHz	25 000Hz	
5	4.167MHz	20 833Hz	125000/(AD1_FILTDEV+1) [Hz].
6	3.571MHz	17 857Hz	
35	694kHz	3 472Hz	The power up reset state is
36	675kHz	3 378Hz	ADx_FILTDEV=124, which means
37	657kHz	3 289Hz	1000Hz cutoff. ☞
124☞	200kHz☞	1000Hz☞	
255	97kHz	488Hz	

Table 9.1

The Figure 9.2 shows the 3.4kHz cutoff frequency setup with ADxFILTDEV=34.
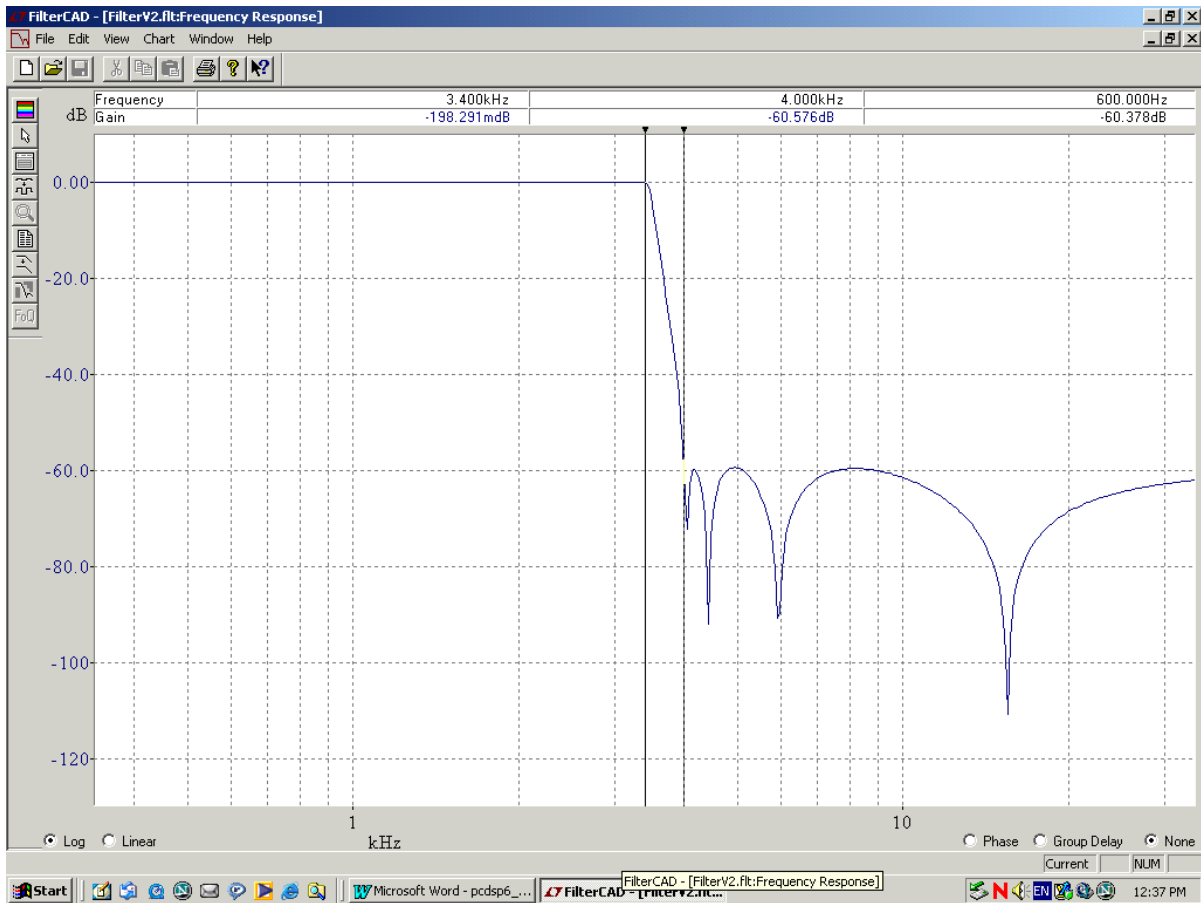
Figure 9.2.

10. Base-band analog outputs

The two channel base-band analog outputs can be accessed from both DSP1 and DSP2, according to the Figure 10.1. The two's complement 14 bit D/A data are aligned to the MSB of DSP data bus. The two LSB bits do not care.
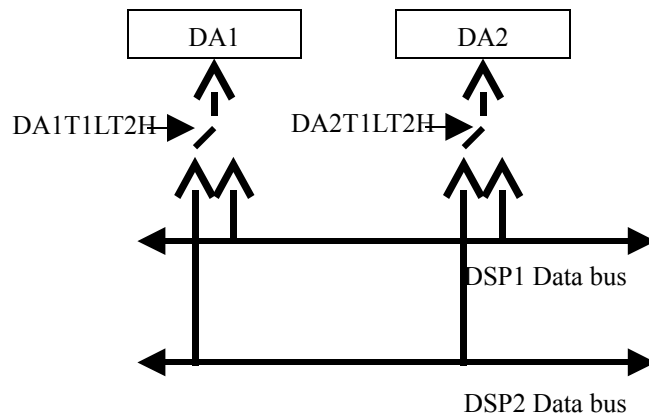
Figure 10.1

The block diagram of the base-band analog output is according to the Figure 10.2. The filter section is the same as in the analog input section.
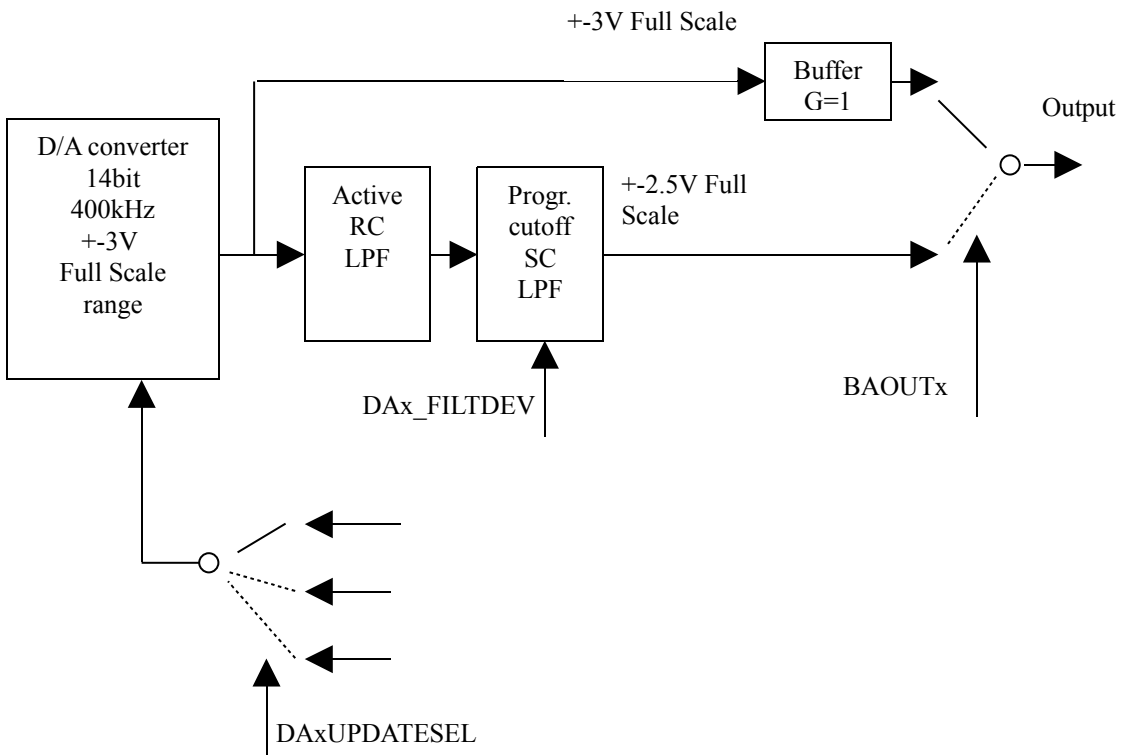
Figure 10.2

11. Two-port memory

The 16KW – 32KB two-port memory is used to communicate between the DSPs very fast.

The memory (after the EMIF initialized) can be accessed from both DSPs at the same address region, according to the memory map on the Table 11.1.

DSP access Address Range In DSP1 and DSP2	PCI access DSPP, Base0 offset address	PCI access Base1 offset address	Size (Bytes)	Description of Memory
6C00 8000–6C00 FFFF	DSPP=1B0 00 8000–00 FFFF	-	16KW 32KB	*Two-port memory* External memory interface EMIFB CE3 as 16bit wide synchronous

Table 11.1.

12. SyncBus, MLVDSbus

These signals share the CN4 connector. The SyncBus signals are asymmetrical, while the MLVDSbus signals are symmetrical.

12.1. The SyncBus

The SyncBus is a 3-line asymmetrical synchronization bus that synchronizes the operation of a multi-board system equipped by SyncBuses. The source of signals can be from the same board, or from other boards. One line must be driven by one source. The SyncBus line must be enabled by writing the SYNCBUSxDRVEN register. The source of the SyncBus line can be selected by the SYNCBUSxSEL register. The SyncBus lines are 3.3VCMOS compatible, are NOT 5V tolerant.

SYNCBUSxSEL

SYNCBUSxDRVEN

SyncBusx signal for local or global usage

SyncBusx signal for local usage
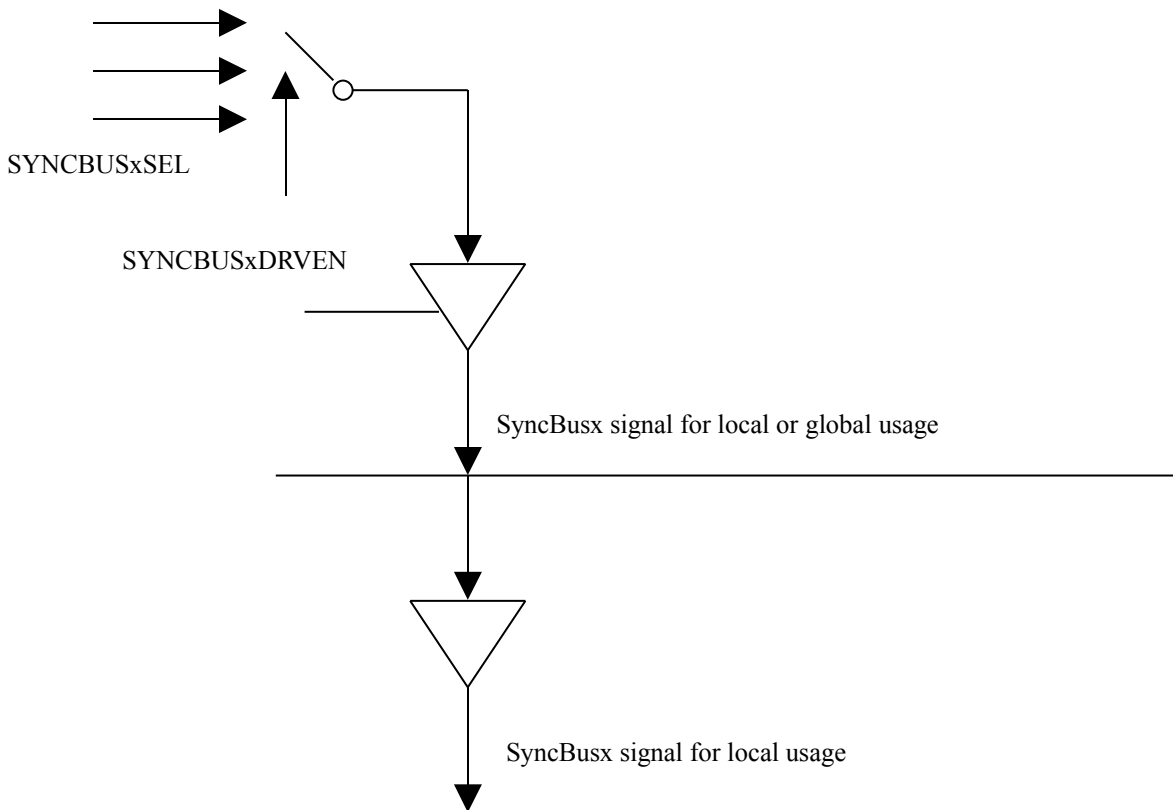
Figure 12.1.1

12.2. The MLVDSbus

The MLVDSbus has two symmetrical signal pairs. This synchronization purpose bus is used to synchronize multi-board systems. High frequency signals, the DDS output signal, the RCLKIN (50MHz) signal, the 2048kHz local clock signal, and the DSPs TOUTx signals can be sent to the bus.

Using this bus more than two channels can be sampled simultaneously at the high-speed A/Ds, etc.

The Figure 12.1. shows the point-to-point structure M-LVDS driver/receiver pairs.

The Figure 12.2. shows multi-point mode, when the middle boards have no termination resistors. The 100 Ohm termination should be inserted at the ends of the line. The termination resistors can be inserted by the JP1 and JP2 jumpers, for the MLVDSBUS0 and MLVDSBUS1 respectively.

Figure 12.2.1.

Board1   Board2   Board3   Board4

100Ohm   100Ohm
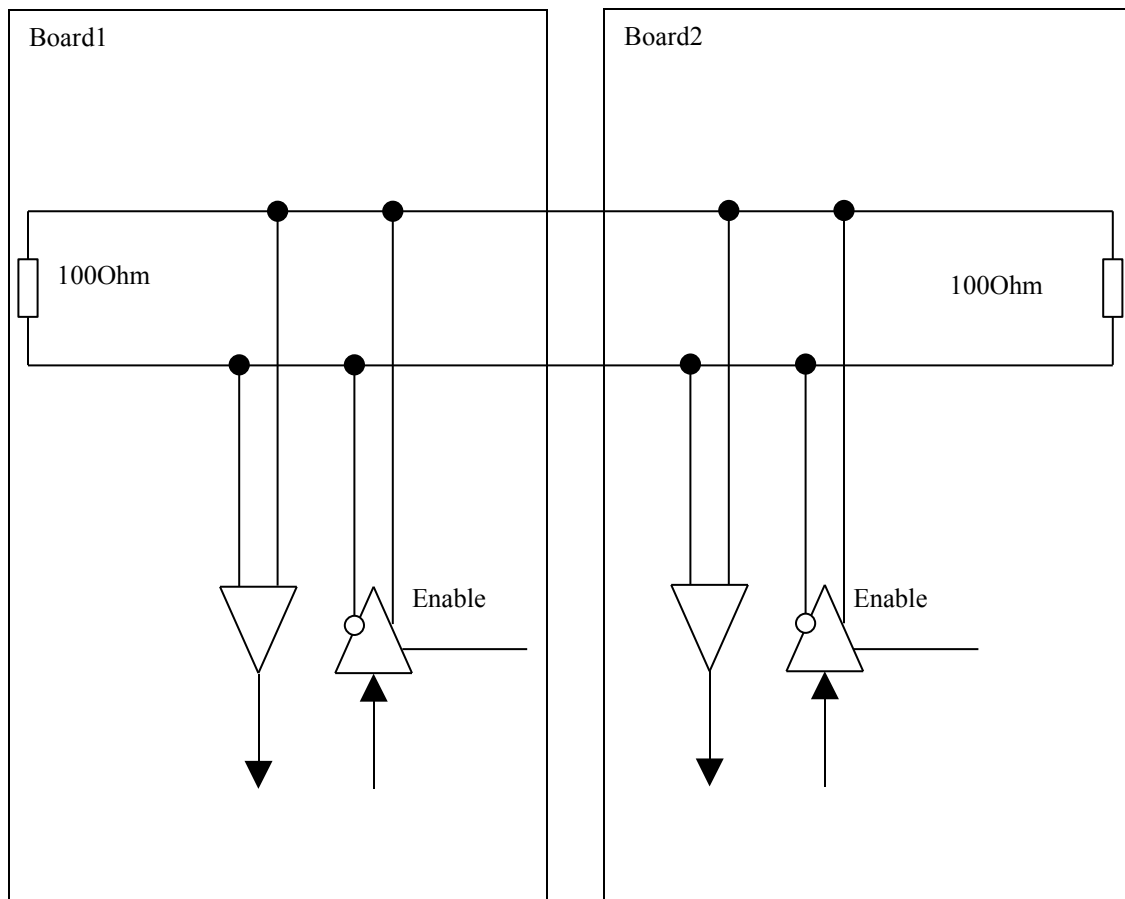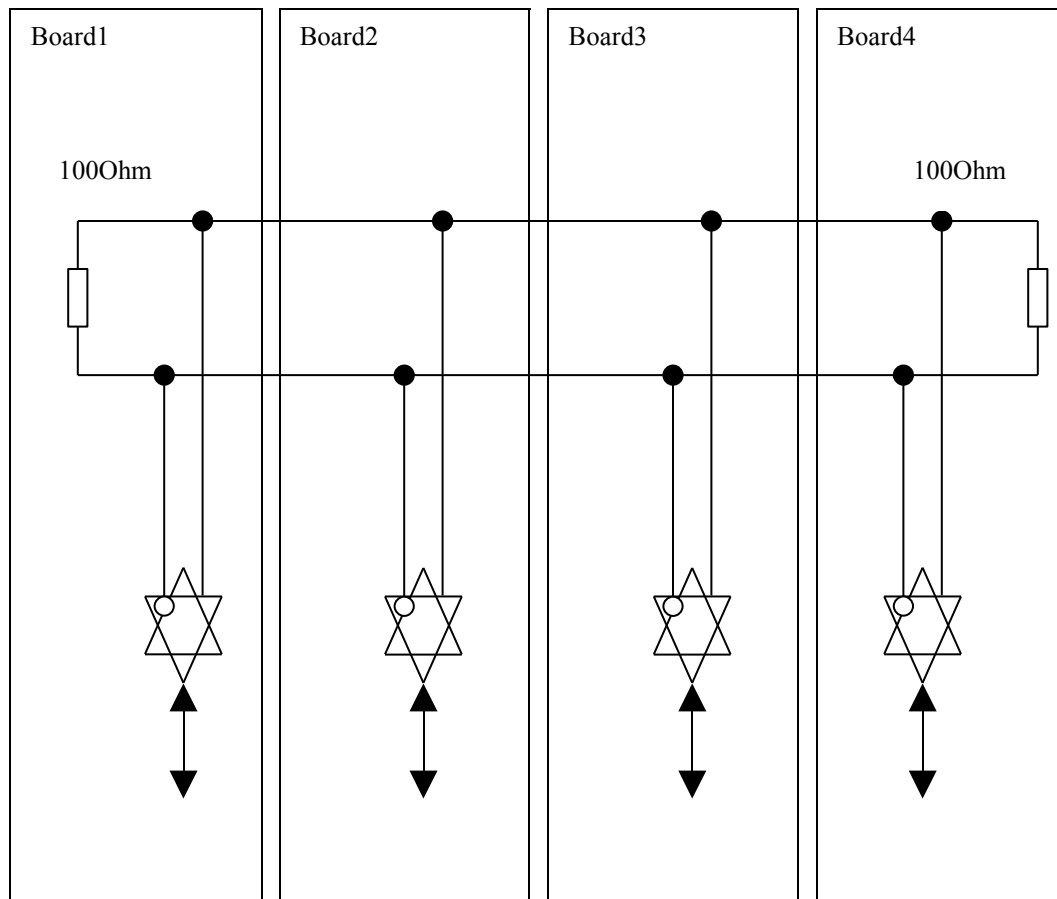
Figure 12.2.2

13. Clocking of the DSPs

The clocking scheme of PCDSP6 makes it possible to run DSPs on the same clock base in different boards. The power up state of the clocking switches is the local 50 MHz (25ppm) oscillator. The right sequence of changing the clock source to a different one:

1. Program the PGPIO0 and PGPIO1 to output in PCI/PCI bridge.
2. Put the DSP in hardware reset state writing zero to the PGPIO0 or PGPIO1 for the DSP1 and DSP2 respectively.
3. Program the PGPIO2 bit to output in the PCI/PCI bridge, and set them to zero.
4. Select the clock source in the FPGA by writing the FPGAT1T2CLKIN_SELECT bit.
5. Change the clock source in the CPLD to the FPGA source by writing the PGPIO2 to 1.
6. Write ones to the PGPIO0 and PGPIO1 to deassert the reset lines.
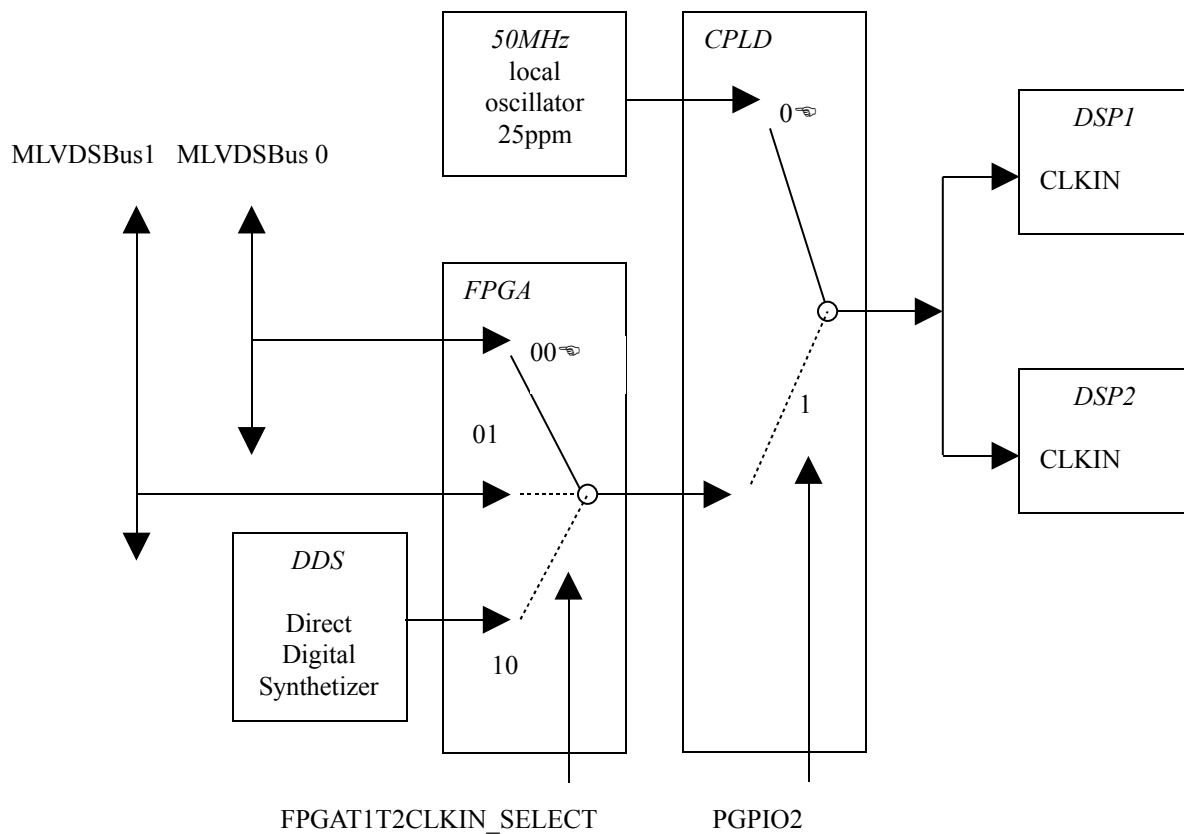
Figure 13.1.

14. Hardware RESET signals of DSPs

The hardware RESET signals of DSPs are generated according to the Figure 14.1.
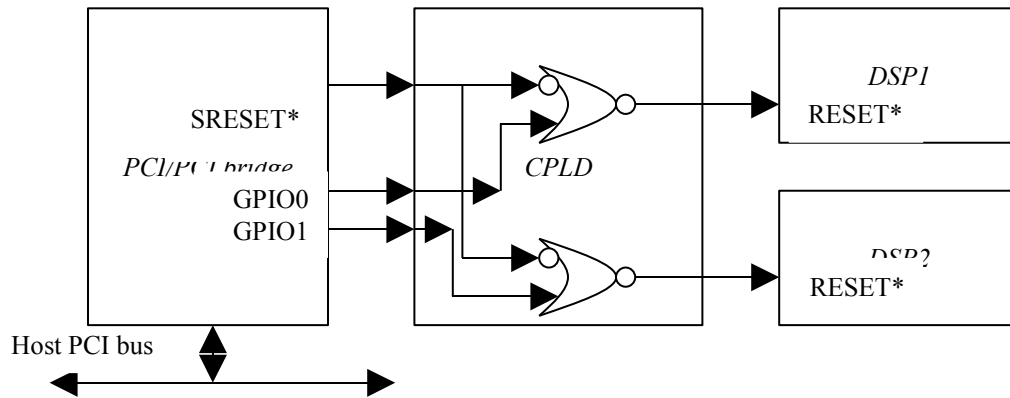
Figure 14.1.

The GPIO0 and GPIO1 signals are pulled down, because the GPIO1 and GPIO2 signals are in tri-state after power up. The RESET signals are active low signals, so the power up states of that are reset. Programming GPIO signals to output, and putting them into high, the DSPs go to hardware reset state. After the needed active reset pulse duration the GPIO lines must be set to low ending the hardware reset cycle. The PCI reset always generates a secondary bus SRESET*, which generates hardware resets for DSPs.

15. Interrupt

The board has a versatile interrupt structure with interrupts from the PC to DSP and the DSP to PC directions.

15.1. DSP Interrupts

The source of the NMI and the ExtInt4.. 7 External Interrupts can be programmed according to the following Table 15.1. and Table 15.2. for DSP1 and DSP2 respectively.

Interrupt	Interrupt source
DSP1 NMI	NMI command
DSP1 ExtInt4	Can be programmed by the DSP1_INT4_SEL register
DSP1 ExtInt5	Can be programmed by the DSP1_INT5_SEL register
DSP1 ExtInt6	Can be programmed by the DSP1_INT6_SEL register
DSP1 ExtInt7	Generated by writing doorbell register or by the external source connected to CN 3 Pin1

Table 15.1.

Interrupt	Interrupt source
DSP2 NMI	NMI command
DSP2 ExtInt4	Can be programmed by the DSP2_INT4_SEL register
DSP2 ExtInt5	Can be programmed by the DSP2_INT5_SEL register
DSP2 ExtInt6	Can be programmed by the DSP2_ INT6_SEL register
DSP2 ExtInt7	Generated by writing doorbell register or by the external source connected to CN3 Pin11

Table 15.2.

The EXTINT7 is generated according to the Figure 15.1.1.
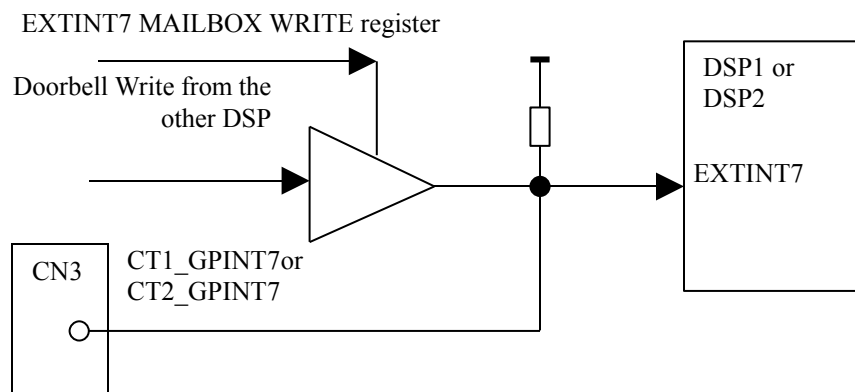
Figure 15.1.1

15.2. INTA#, INTB# Interrupts

The DSP1 and DSP2 DSPs can generate INTA# and INTB# interrupts respectively by writing a 1 to INTREQ bit in the DSP reset source/status register (RSTSRC). This causes the PINTA#, or PINTB# pin to be asserted on the PCI bus, if the INTAM bit in the host status register (HSR) is 0. The PINTA pin is negated by writing a one to the INTRST bit in RSTSRC. The interrupt must be cleared, by writing one into the INTRST, before another interrupt can be requested via INTREQ.

16. Doorbell registers

The doorbell register is an 8-bit register implemented in the nonvolatile CPLD, ready to use after power up before FPGA programming. The operation is demonstrated in Figure 16.1.

Read the 0x6000 0005 address in DSP1

Write the 0x6000 0005 address in DSP1

Read the 0x6000 0005 address in DSP2

Write the 0x6000 0005 address in DSP2

DSP1

8 bit register
D   Q

DSP2

ExtINT7

8 bit register
Q…   ………D

ExtINT7

CN3
Pin1

0   1

1

0   CN3
Pin11

EXTINT7 Doorbell WRITE
DSP1 address 6000 0011

EXTINT7 Doorbell WRITE
DSP2 address 6000 0011
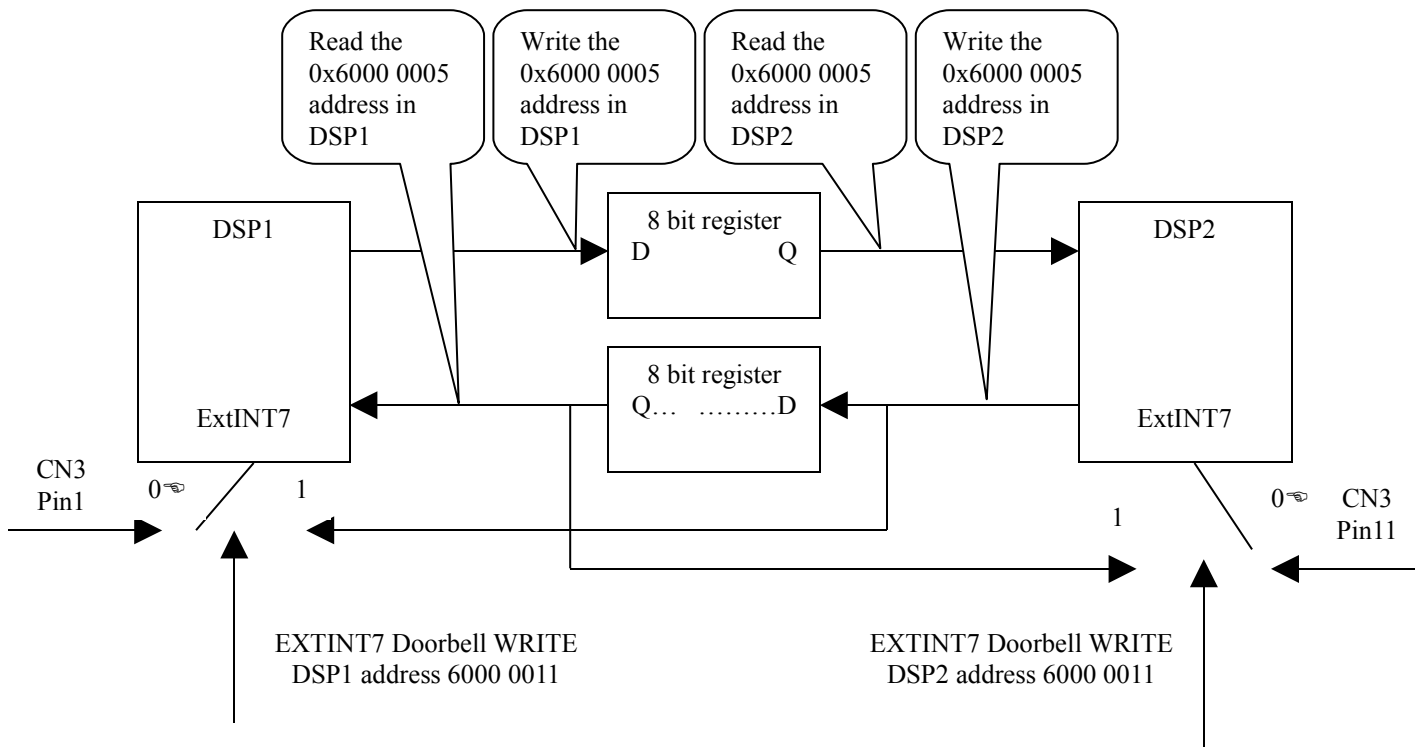
Figure 16.1.

17. General purpose I/Os of DSP1 and DSP2

CN3 pin3

DSP1

GPIO0
GPIO1/CLKOUT4**
GPIO2/CLKOUT6**
GPIO3
GPIO4/EXT_INT4*
GPIO5/EXT_INT5*
GPIO6/EXT_INT6*
GPIO7/EXT_INT7*
GPIO8

FPGA

Not used in FPGGA ver1
Not used in FPGGA ver1

Programmable sources
Programmable sources
Programmable sources

Not used in FPGGA ver1

CN3 pin2
See Chapter 7

See chapter 15

CN3 pin13

DSP2

GPIO0
GPIO1/CLKOUT4**
GPIO2/CLKOUT6**
GPIO3
GPIO4/EXT_INT4*
GPIO5/EXT_INT5*
GPIO6/EXT_INT6*
GPIO7/EXT_INT7*
GPIO8

Not used in FPGGA ver1
Not used in FPGGA ver1

Programmable sources
Programmable sources
Programmable sources

Not used in FPGGA ver1

CN3 pin12   See chapter 15

*: These pins are driven by selected sources of interrupts. These signals can be used as GPIO input, or can be used as normal interrupt source. After power up these DSP pins are GPIO inputs.

**: GPIOx/CLKOUTx are connected to FPGA, but not used in FPGA ver1.

18. Digital pots in the base-band input/output

The A/D section has two-two digital pots. One is for A/D gain, the other is for the programmable filter offset.

The pots can be reached on the I2C serial bus. The bus contains a clock and a data line. The bus clock and data line can be programmed accessing the I2C* Data, I2C* Data Bus Drive Enable, I2C SERCLK registers.

The nonvolatile digital pots are packed into one XICOR X9241W chip.

The U18 digital pot (Address is 0 on I2C bus):
Pot0 – Offset setting of analog input 1- PGA, GAIN1 offset
Pot1 – Offset setting of analog input 1 - SC filter offset FAIN1
Pot2 – Gain setting of analog input 1 - Gain=1.. 10.
Pot3 – Offset setting of analog output 1 SC filter offset FAOUT1

The U33 digital pot (Address is 1 on I2C bus):
Pot0 – Offset setting of analog input 2- PGA, GAIN2 offset
Pot1 – Offset setting of analog input 2 - SC filter offset FAIN2
Pot2 – Gain setting of analog input 2 - Gain=1.. 10.
Pot3 – Offset setting of analog output 2 SC filter offset FAOUT2

19. Configuration of on-board FPGA

The Onboard FPGA can be configured from the FPGA JTAG connector, or via the CPLD from the PCI bus (slave parallel) depending of the JP3 JP4 jumpers.
If the slave parallel is selected, the FPGA can be configured according to the Xilinx documentation Figure 7.
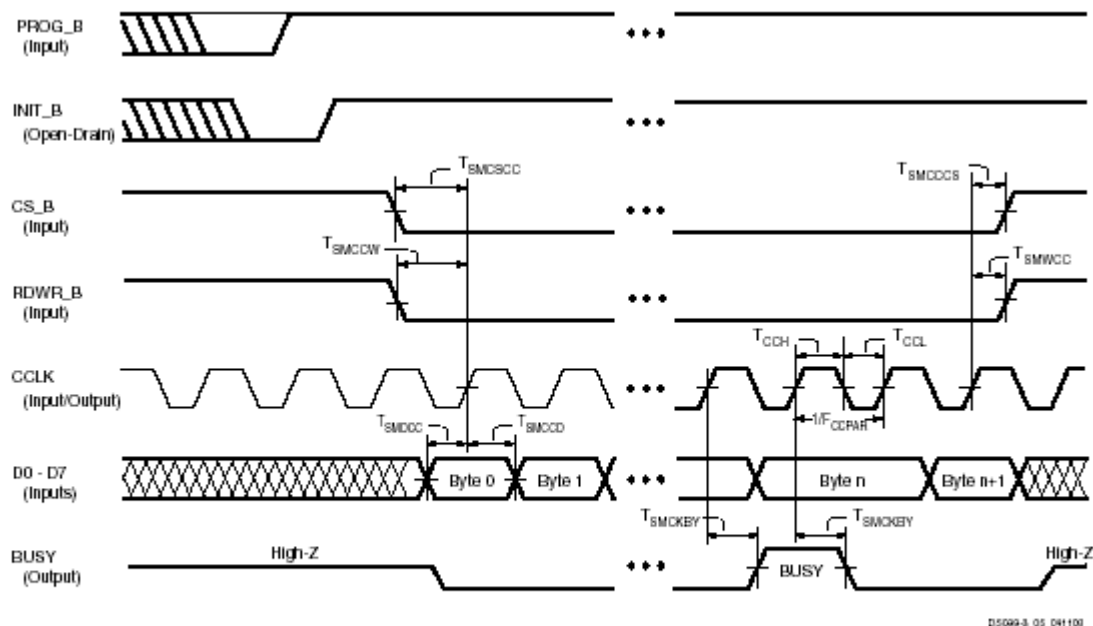
Notes:
1. Switching RDWR_B High or Low while holding CS_B Low asynchronously aborts configuration.

Figure 7: Waveforms for Master and Slave Parallel Configuration

From Xilinx document DS099.pdf

The configuration process starts writing PROG_B from the initial zero to one, by writing a one to the FPGA PROG_B (6000 0006h) DSP address in DSP1. The FPGA answers this command by setting the INIT_B output to one. This signal can be read by reading the address FPGA INIT_B (6000 0007h). Then the CS_B FPGA configuration chip select should be activated, by writing a zero to FPGA CS_B (6000 0008h). The FPGAWR_B should be set to zero signing the write cycle of configuration data. This can be done, by writing the FPGA RDWR_B (6000 0009h) to zero. After these configuration initialization the configuration bytes can be written into the FPGA data port 6000 000Ah. The CCLK signal is generated by the CPLD hardware automatically during the access to the FPGA data port. Before each write the BUSY status should be checked by reading FPGA BUSY (6000 000Bh) address. The one means busy. After the last configuration byte write, the FPGA signals the ready configuration by setting DONE signal high. This can be monitored by reading the FPGA DONE (6000 000Ch).
The configuration area can be read back by a similar cycle, but with an FPGAWR_B high bit.

20. Specification

20.1. DSP section

2 pieces 1GHz TMS320C6416 DSPs
128MB SDRAM pro DSPs
125MHz SDRAM clock speed
16KW two-port memory between DSPs

20.2. FPGA section

1.5 Million Gate SPARTANIII FPGA
32 dedicated multipliers
208Kbit distributed RAM
576Kbit Block RAM

20.3. Base-band Analog Input Channels

Number of analog inputs:	2
Input impedance at both channels:	100kOhm
Full-scale input range (Gain=1):	+-2.5V
Maximum over-voltage at input:	+-6V
Input gain:	0dB.. 20dB
Anti-aliasing filter cut-off frequency range:	400Hz.. 25kHz
Passband ripple:	typ. 0.1dB
Stopband attenuation f>1.18fc	>60dB
Anti-aliasing filter gain:	0dB
A/D converter resolution:	16bit
A/D converter code format:	two's complement
Maximum sample rate:	500kHz

20.4. Base-band Analog Output Channels

Output impedance:	100Ohm
Full-scale output range in buffered, *unfiltered* case:	+-3V
Full-scale output range in *filtered* case:	+-2.5V
Reconstruction filter cut-off frequency range at outputs:	400Hz.. 25KHz
Passband ripple:	typ. 0.23dB
Stopband attenuation f>1.18 fc:	>60dB
D/A converter resolution:	14bit
D/A converter code format:	two's complement, 14bit word MSB fitted
Maximum update rate:	400kHz

20.5. High-speed Analog Input Channels

Number of analog inputs: 2
Input impedance at both channels: 50Ohm
Full-scale input range :   +-0.5V
Maximum over-voltage at input: +-6V
A/D converter resolution: 14bit
A/D converter code format: two's complement, 16bit MSB fitted
Maximum sample rate: 80MHz

20.6. E1 interfaces

Number of E1inputs/outputs: 2/2
Input impedance at both channels: 75Ohm

Appendix A - The TMS320C6416 DSP PCI EEPROM (AT93C66) content

Serial EEPROM Word Offset	Value (Hex)	Description
00	104C	Vendor ID
01	6001	Device ID
02	0001	PCICCR; Class Code rev
03	FF00	PCICCR; Class Code
04	104C	Subsystem Vendor ID, Texas Instruments
05	6416	Subsystem ID,
06	0000	Maximum Latency, Minimum Grant
07	0000	PD 3/PD 2
08	0000	PD 3/PD 2
09	0000	PD 3/PD 2
0A	0000	PD 3/PD 2
0B	0100	Data scale
0C	0000	PMC[14-9]
0D	50BC	Checksum

Table A 1 - DSP1 and DSP2 EEPEROM

Appendix B - The PCI6152 EEPROM (AT24C02) content

Serial EEPROM Byte Address	Value (Hex)	Description
00	16	EEPROM Signature
01	15	EEPROM Signature
02	1E	Region Enable
03	00	Secondary Clock Enable SCLKOUT0 enabled SCLKOUT1 enabled SCLKOUT2 enabled SCLKOUT3 enabled SCLKOUT4 enabled
04	4C	Subsystem Vendor ID, Texas Instruments,
05	10	Subsystem Vendor ID, Texas Instruments,
06	16	Subsystem ID,
07	64	Subsystem ID,
08	00	Misc.
09	00	Misc.
0A	B5	Vendor ID,
0B	10	Vendor ID,
0C	52	Device ID,
0D	61	Device ID,
0E	00	Misc.
0F	00	Misc.
10	00	PMC
11	00	PMC
12	00	PMC
13	00	PMC
14	00	Test
15	00	Test
16	00	Test
17	00	Test