



Task 1. Let us consider a cache memory of 256 bytes. The block size is 64 bytes. The cache content is assumed to be invalid initially.

A program reads from the following memory blocks (in the given order):

- 1, 3, 8, 4, 3, 6, 8, 1

Compute the number of cache misses and provide the final content of the cache

- (a) in case of direct mapped organization,
- (b) in case of fully associative organization with LRU block replacement strategy,
- (c) in case of 2-way set associative organization with LRU block replacement strategy.

Task 2. Assume the total size of the cache memory is 512 bytes and the block size is 64 byte. The addresses of the CPU are 16 bit wide.

A program reads from the following memory *addresses* (in the given order):

- 13, 136, 490, 541, 670, 74, 581, 980

- (a) What are the "tag", "index" and "offset" values of the given addresses
 - in case of fully associative organization,
 - in case of direct mapped organization,
 - in case of 2-way set associative organization.
- (b) What is the final content of the cache (in all three cases)? The cache content is assumed to be invalid initially.

Task 3. The size of the cache memory of a CPU is 1kB, the block size is 64 byte. The CPU executes the following program:

```
short int t[32][32];
int sum = 0;

for (int i=0; i<32; i++)
    for (int j=0; j<32; j++)
        sum += t[i][j];
```

Assumptions: the size of the `short int` type is 2 byte, array `t` starts at a block boundary in the memory, the two-dimensional array is arranged in a row-continuous way in the memory, the cache uses a direct mapped organization. Variables `i, j` are stored in registers, using them does not involve the cache memory.

- (a) How many cache misses occur during the execution of the given algorithm? Compute the cache miss ratio!
- (b) How many cache misses occur if the two for loops are swapped? Compute the cache miss ratio!
- (c) How large cache memory is needed to achieve the same cache miss ratio with the swapped variant as with the original variant?