Computer Architecture

Exercises: Virtual Memory

Task 1. Assume that the memory of a computer is based on single channel DDR1-SDRAM technology with 64 bit data units. The burst size is set to 8. Let us ignore the presence of multiple banks and ranks.

The timing values of the memory modules are as follows (given in clocks):

- T_{RP} = 4 (the delay of the PRECHARGE command)
- T_{RCD} = 5 (the time needed to activate a row)
- T_{CAS} = 9 (the time needed to read/write a column in the active row)

The memory controller receives the following read requests (of 64 bytes, hence one burst), given by row and column coordinates:

- (row 3, column 8), (row 3, column 2), (row 7, column 9)

Row 7 is active initially. After the last command the memory controller does not close the active row.

(a) List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling!

(b) According to the FCFS scheduling, in which clock cycle does the first data appear on the data bus? And when does the last data corresponding to request (row 3, column 2) appear?

Task 2. Let the virtual addresses be 16 bit wide, and the physical addresses 15 bit wide. The page size is 2^{12}byte = 4 kB, and the page table is a simple single-level page table with 8 bit wide entries.

(a) In the virtual address, how many bits correspond to the page number and the position inside the page (offset)?

(b) What is the total size of the page table?

(c) How many pages fit into the physical memory?

(d) Assume the current state of the page table is as follows.
Where is page 3, 6, and 11 located?

(e) Modify the content of the page table according to the following.

- Page 6 is on the disk
- Page 11 is in the physical memory, in frame 1
- Page 8 is on the disk
- Page 2 is in the physical memory, in frame 6

(f) If there is no page fault, how many memory operations are required for address translation

- in case of TLB hit?
- in case of TLB miss?

Page table:

	Valid:	Frame:
0:	1	5
1:	1	7
2:	0	?
3:	1	2
4:	0	?
5:	0	?
6:	1	1
7:	0	?
8:	1	6
9:	0	?
10:	0	?
11:	0	?
12:	1	0
13:	1	3
14:	0	?
15:	1	4

Task 3. Let the virtual addresses be 14 bit wide, and the physical addresses 13 bit wide. The page size is 2^{10}byte = 1 kB, and the page table is a two-level hierarchical page table with 16 bit wide entries. To accelerate the address translation the CPU has a TLB with 4 entries and LRU content management.

(a) In the virtual address, how many bits correspond to the page number, the page table indices, and the position inside the page (offset)?

(b) How many pages fit into the physical memory?

(c) What is the total size of the page table?

(d) What is the minimal size of the page table? How much less is it compared to a single-level page table?

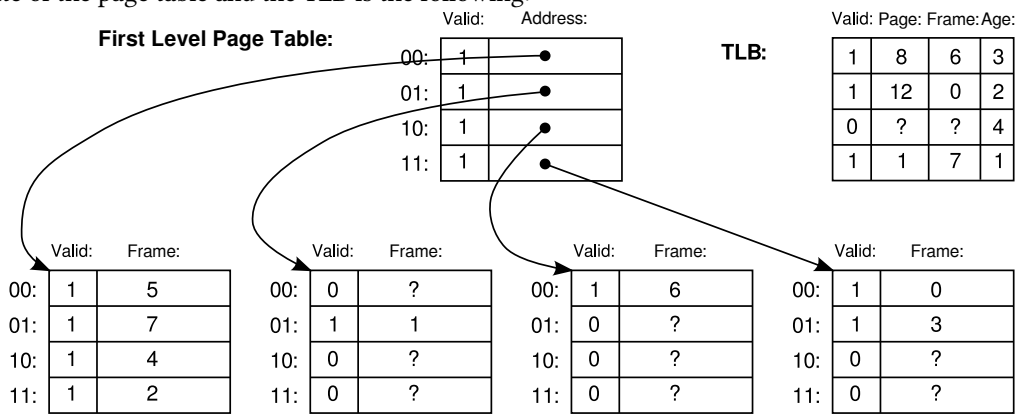
(e) If there is no page fault, how many memory operations are required for address translation

- in case of TLB hit?
- in case of TLB miss?

(f) Assume that the current program executed by the CPU refers to the following pages (in this order):

- 13, 12, 7, 2, 13.

The initial state of the page table and the TLB is the following:



- Follow the evolution of the page table and the TLB with the given memory references! When the operating system needs to accommodate a new page in the physical memory, it has to through out an other page to make place. The next victims are pages 1 and 5. After modifying the page table the operating system invalidates the entire TLB.
- What is the number of TLB hits?
- What is the number of page faults?