# A Practical ADSL Technology Following a Decade of Effort

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## ABSTRACT

This article offers a behind the scenes glimpse of a successful ADSL transceiver development, completed over the last decade while the ADSL standard evolved. It discusses the pitfalls experienced by designers and describes how a pragmatic and unconventional design solution was found.

## OVERVIEW

Without attempting to be complete in a historical sense, this article describes the findings of a team of engineers after a decade of activity in asymmetric digital subscriber line (ADSL) technology. It shows how they built an unconventional ADSL modem with micro-coded modules slaved by a simple microcontroller. We list their options and choices. Their approach is compared with a more common variant: using a platform with a general-purpose digital signal processor (DSP) at its center.

The solution proposed by the authors was paralleled in many DSL companies. In the 1990s several teams of engineers worked on ADSL system design to achieve affordable complexity. Eventually, only a few particular transceiver designs became successful. This was due to designer ingenuity in combination with other nontechnical factors such as company culture and marketing conditions.

In order to help the reader understand the logic behind the final technical choices of this ADSL solution, this article will present the most important design steps taken in chronological order as related to the dynamics of standards and markets. First, we give a brief review of the digitization trends in telecommunications and review some background necessary to understand this topic. Next, the article focuses on a particular way to solve the MIPS problem and how it was formed into hardware, software, firmware, and silicon.

## DIGITIZATION OF THE TELEPHONE NETWORK

At the end of the 20th century, the digitization of telephony and an immense growth of digital data transmission came about. The deployment of DSL technology was part of this evolution. Today, worldwide business and residential customers can enjoy high-speed DSL access on old telephone wires. Whether underground or hanging overhead, these copper cables have been reused successfully for digital transmission. The exemplary reutilization of the copper infrastructure is a main factor responsible for the success of digital data transmission in the access network.

Telephone twisted pair wires have been around for more than a century and were originally intended to transport analog telephone signals invented by Graham Bell at the end of the 19th century.[1] These copper wires constitute the most widely deployed access network, with more than 800 million fixed telephone subscribers worldwide. Most likely, they will be in use for at least a few more decades in the 21st century.

In the late 1960s and early 1970s, after 70 years of analog telephony, the interconnection of computers required means for digital data transport via the telephone networks. Voiceband modems were born. Inside the analog telephone networks, these new modem signals were still limited to the 3.2 kHz bandwidth used internationally for voice.

At the end of the 1970s, pulse code modulated (PCM) trunks were introduced, starting the digitization of the telephone networks interconnecting central offices. This was a first example of efficient reuse of the analog infrastructure. These trunks had served as the interconnection of the older analog exchanges. Composed of multiple twisted copper pairs, each pair used to transport one voice call in one direction. For digital interconnections the voice was sampled at 8 kHz and

[1] *Another, however far more limited use of these twisted pairs was the transport of telex signals.*


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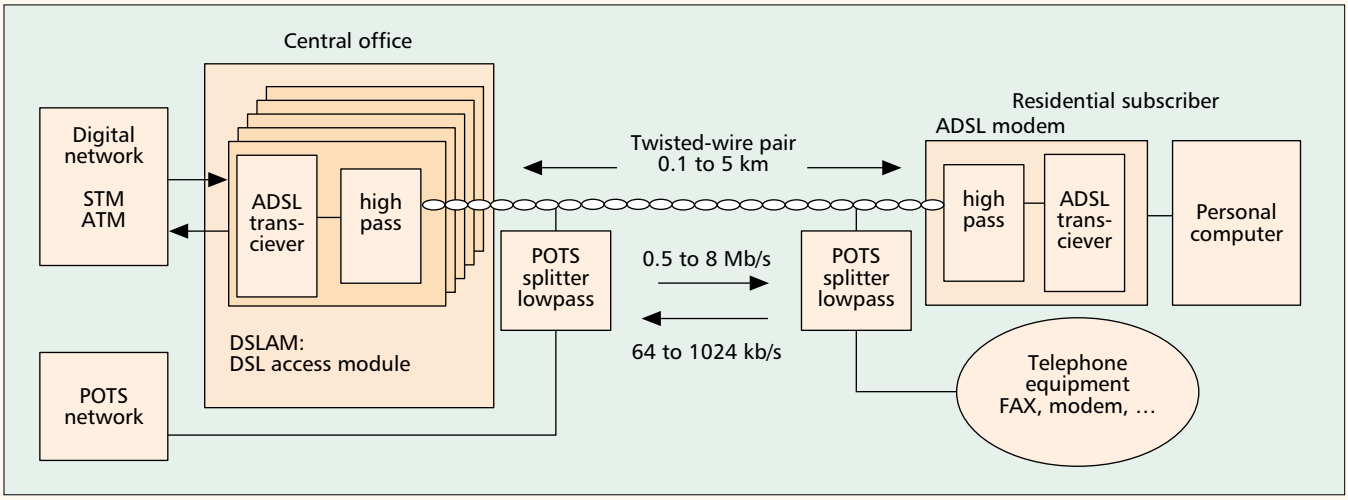


**Figure 1.** *A block diagram of ADSL access, with splitters, DSLAM, and POTS network.*

digitized into PCM channels at 64 kb/s. With *digital* repeaters every 1.8 km, one twisted pair could now carry 24 to 32 multiplexed digital PCM channels. The reuse of the available analog trunks reduced the need to invest in new cables. Moreover, digital PCM over the existing cables combined higher capacity with quality improvement since PCM transmission is free of analog noise.

In the early 1980s, the concept of an integrated services digital network (ISDN) appeared. Voice and data coexist in the digital network, each on 64 kb/s PCM B-channels. Immediately there was a need for a digital subscriber line (DSL) standard toward the customer. ISDN-BA (basic access) offered two data or voice calls in parallel.

After PCM and ISDN, the evolution of digital data transport accelerated. Digital trunk networks evolved from the early PCM-based links to optical transmission with synchronous optical network (SONET) and synchronous signal digital hierarchy (SDH) technologies. In the copper access network, ISDN-BA evolved to high-rate DSL (HDSL) in the 1980s and signal pair DSL (SDSL) in the 1990s, offering megabit-per-second access to business customers, on one, two, or three parallel pairs.

In the early 1990s a younger child of the DSL family was born: ADSL, intended initially for offering video on demand (VoD) services to residential customers. *IEEE Communications Magazine* describes ADSL standardization in [1].

More recently, single pair HDSL (SHDSL) and very high rate DSL (VDSL) were standardized, in 2000 and 2001, respectively. SHDSL is a single pair evolution of the HDSL standard. VDSL can be viewed as the higher-speed short-haul variant of ADSL, but with both asymmetrical and symmetrical bit rates as options [2, 3]. Additional background information on ADSL — and other DSL variants — can be found in multiple textbooks such as [4, 5].

## Fundamentals of ADSL

Although ADSL was originally intended for VoD, the video-over-DSL hype in the first half of the 1990s was not successful due to the need for large investments in centralized video equipment and major upgrades of the backbone network. Other factors were the relatively poor quality of early MPEG-1 digital video, the high price of set-top boxes, the lack of an easy-to-use service control and management system, the limited video offering in early field trials, and competition with video rental stores. In the end there was no viable business case.

Already standardized in the North American T1E1.4 committee in 1995, ADSL was retargeted for Internet access in 1997. The data rates for VoD at multiples of 1.5 Mb/s and a narrow upstream (from the end user to the network) command channel could easily be adapted. The standard was indeed very flexible. Rather than being limited to a fixed bit rate, ADSL can indeed be tuned dynamically to deliver any predefined rate (if attainable), or even the maximum available bit rate on the line.

At the higher end, ADSL can transport more than 8 Mb/s to the customer (downstream) and more than 1 Mb/s upstream. Moreover, by making the transceivers more sensitive, ADSL could transport an impressive 0.5 Mb/s over more than 5 km on 0.4 mm cable and still offer over 128 kb/s upstream.

### Basics of ADSL Access

ADSL allows for simultaneous transmission of digital data and the plain old telephone system (POTS) signal[2] on a single copper pair. The network elements for ADSL access are shown in Fig. 1. The transmission is in frequency overlay, that is, at frequencies above the existing telephony band. At both ends of the telephone pair, a splitter-combiner filter multiplexes the POTS signals with the ADSL signals. These filters also prevent mutual interference of both signals [4, 5].

### Two Duplexing Variants

In order to combine the up- and downstream signals on a single telephone line, the ADSL standard allows for two variants. The first one, depicted in Fig. 2a, has a downstream signal overlapping the upstream and requires echo can-

[2] *Although the acronym POTS is not very respectful, it is commonly used, even in standardization.*

celing (EC) to separate both signals. The second one uses frequency-division duplexing (FDD) with separate bands for the up- and downstream, as shown in Fig. 2b.

## Importance of ASIC Expertise

Telecommunication companies building telephony equipment have evolved over the years. In the past they owned as much of the complete technology chain as possible. Once the digitization of telephone switches started, the percentage of the hardware that was fully internally manufactured dropped, and the added value was mostly in software.

Despite this evolution, ownership of intellectual property and mastering of key components and technologies remained important. The ownership of essential integrated circuits (ICs) and application-specific ICs (ASICs) proved to be the key to success for many telecom companies.

## Building an ADSL Modem

At the beginning of the design phase, some essential choices had to be made with respect to the mode of operation and the partitioning in modules, hardware, and ASICs.

### An Early Preference for FDD

As described above, the standard allows for a difficult EC implementation or an easier FDD variant. The FDD implementation can be made with filters and requires a much smaller dynamic range of the analog components. An early decision was to start with an FDD implementation. The system could evolve later to a more complex EC structure.

The choice of FDD was reasonable since for VoD, FDD-based ADSL has only a slightly shorter reach than the EC variant. In theory EC has a higher downstream bandwidth, but can achieve this only on shorter lines. Indeed, on longer lines there is a critical point where FDD can support a higher data rate than EC. The performance on the longest lines was a precise major concern of the ADSL operators.

Furthermore, the FDD variant turned out to be more robust in deployment due to the reduced self-crosstalk.[3] Installing additional FDD ADSL modems hardly harms the performance of the existing ones. In the end, operators tended to forbid the use of overlapping ADSL spectra.

### Basic Hardware Choices

Consider the top-level block diagram of the ADSL transceiver in Fig. 3. This diagram is similar to most DSL transceivers used in other xDSL implementations. At the top level, the transceiver consists of three main functional blocks: the driver, the analog functions, and the digital functions. The choice of FDD simplified each of these functions.

### The Analog ASIC

The main analog functions, with the exception of the line driver, were integrated in an analog ASIC. Given the long time to design and optimize an analog ASIC, early choices had to be made. In order to limit the design effort, the same analog component was used at either side of the line. In upstream the component used a sampling speed higher than the minimal requirement. Two filters were included for FDD separation. The component could switch the filters from upstream receive and downstream transmit to the reverse operation [6].

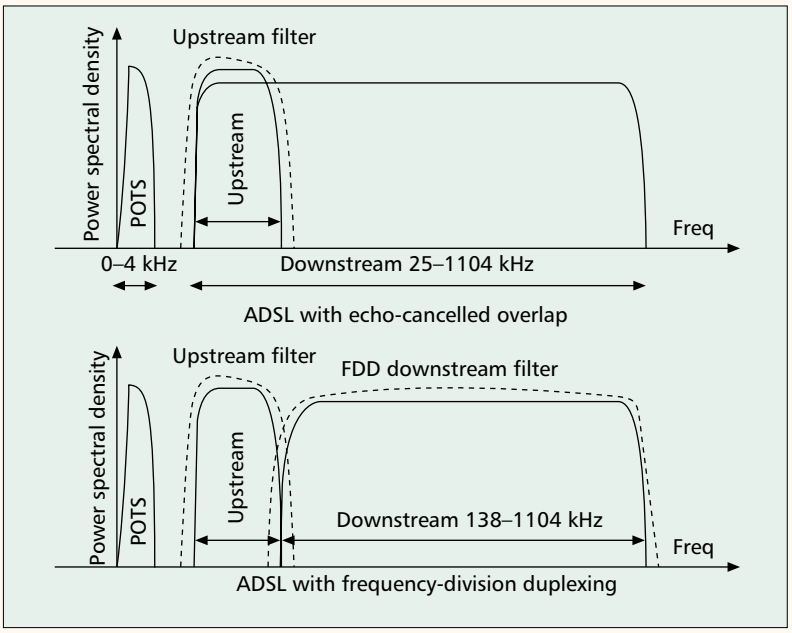


**Figure 2.** *a) Spectral use in EC-ADSL; b) spectral use in FDD-ADSL.*

### The ADSL Emulator

In order to investigate various concepts for discrete multitone (DMT) ADSL transceivers, an early emulator was built using off-the-shelf components: a few general-purpose DSPs plus standard components such as dedicated ICs for fast Fourier transform (FFT), a Reed/Solomon encoder and decoder, analog-to-digital and digital-to-analog converters, and a line driver. The complete transceiver fit on two VME-sized boards, one implementing the analog front-end and the other the digital functionality. A PC card was used to control the configuration. The digital board contained RAM buffers and custom logic between the DSPs and the other blocks. The custom logic was burned in field programmable gate arrays (FPGAs).

Back in 1992, the use of a programmable hardware emulator was very appropriate for the following reasons:

- The ADSL standard was not stable, with main parts of system initialization still undefined.
- The necessary algorithms for synchronization, symbol alignment, and equalization needed further design and optimization.
- The required processing power in terms of millions of instructions per second (MIPS) was overwhelming; for example, the necessary FFT could not be executed in most DSPs commercially available at the time.

On this emulator all algorithms could be developed, tested, and optimized to synchronize, equalize, measure noise and performance, track signal changes, and detect error conditions. Also,

*[3] FDD systems only suffer from far-end crosstalk (FEXT), not from the more damaging near-end crosstalk (NEXT).*

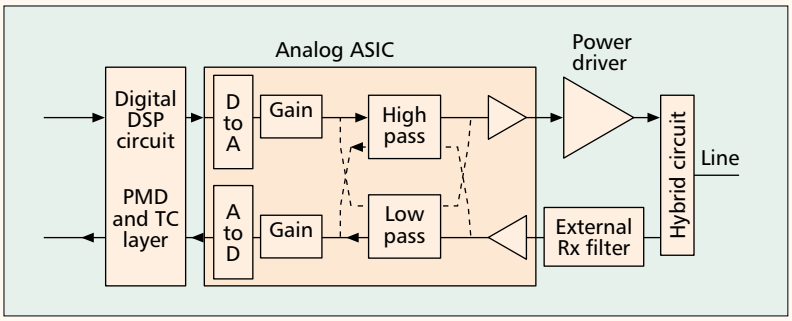


**Figure 3.** *A top-level block diagram of the ADSL modem.*

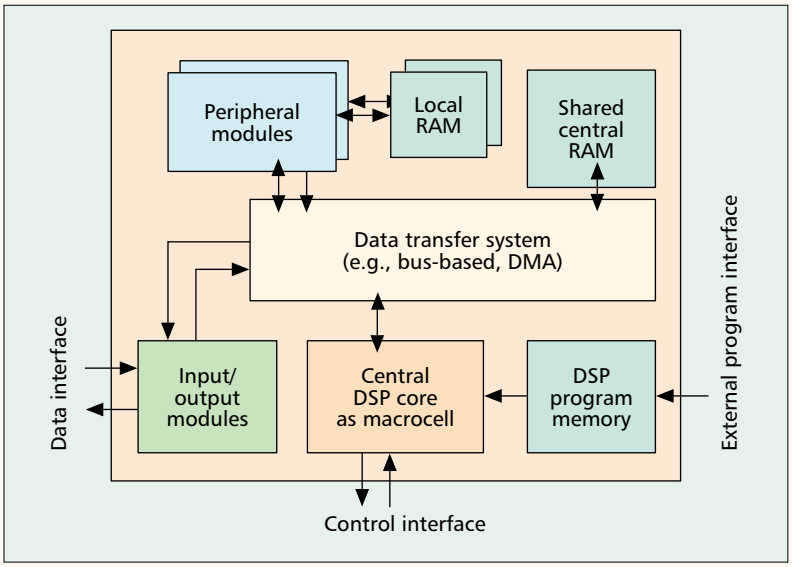


**Figure 4.** *The concept of an ASIC composed with a DSP core at its center.*

for the optimization of the analog front-end the emulator proved to be of high value.

## Building the Digital Component

Based on the emulator results, two ICs were necessary to implement the digital functionality. The first component had to realize the physical medium-dependent (PMD) layer, that is, mainly the DMT (de)modulator. The second one would contain the transmission convergence (TC) layer functions, including forward error correction and interleaving as well as the composition of asynchronous transfer mode (ATM) and synchronous transfer mode (STM) data frames.

In *IEEE Communications Magazine*'s May 2000 issue [7] a programmable implementation is proposed for DSL systems in general. Today this is indeed a valid approach. However, in 1992 this was not feasible. Even today the adopted unconventional approach as described in the following sections turns out to be highly competitive.

### Searching for a DMT ASIC Architecture

A feasibility study showed that it was impossible to map all PMD functions on a single general-purpose DSP processor. It had insufficient MIPS to run an entire DMT "bit-pump." Moreover, the available off-the-shelf processors were still large, power-hungry, and quite expensive.

### Considering an Extended DSP Platform

Thus, in addition to a general-purpose DSP engine, several dedicated "peripheral functions" were needed to reduce the load of the central processor. This would result in an architecture in which the DSP would be integrated as a cell or a core element, as depicted in Fig. 4.

The steps to be taken for such a platform design are:

- Search for a partner that can deliver the main DSP engine.
- Validate that the processor technology has the required performance at the right price: cost and size per DSP core, MIPS per mm$^2$ and per mW.
- Other key elements that have to be analyzed are the reliability of the technology and the available software and hardware design tools.
- Subdivide or partition the problem in dedicated hardware blocks and software on the DSP.
- Design the hardware blocks as extra peripherals and link their outputs to the DSP core.
- Write the algorithms that run onto the DSP core(s).

However, an ASIC containing a DSP core was an exposure to an external vendor. Due to the company culture of owning the full solution, there was no strong incentive to use a DSP machine from an external partner. This situation forced the design team into an *unconventional* path.

### A Pragmatic Solution

A solution was found based on the following logical sequence:

- If the ASIC cannot contain a DSP core, it should contain efficient hardware modules executing all dedicated DSP functions (e.g., FFT) as in the emulator.
- Each of the DSP modules would need some programmability, which could be achieved by making the modules like reduced instruction set computers (RISCs), programmed with a micro-code.
- External to the ASIC there should be a control element with firmware to control the top-level operation of the ASIC during system initialization and *showtime*.[4] This element should load the micro-code into the on-chip modules. To allow for a slower *microcontroller*, no requirements were imposed on it for *real-time* control of the ASIC.
- Inside the chip a central dedicated real-time control or scheduling unit would govern the start of the execution of the micro-programs in each module.

### DASP: Digital ADSL Signal Processor

The PMD component was named *digital ADSL signal processor* (DASP). It has three major parts shown in Fig. 5: the DSP front-end, the FFT block, and the block with mapper, demapper, and monitor. The modules communicate via RAM buffers. These buffers contain time samples and DMT symbols in the time domain, DMT carriers in the frequency domain, and user data bits in the digital data domain.

- In the DSP front-end the time data are filtered: in transmit to shape the spectra, and

[4] *Showtime is the name commonly used for the phase of data transmission after modem initialization.*

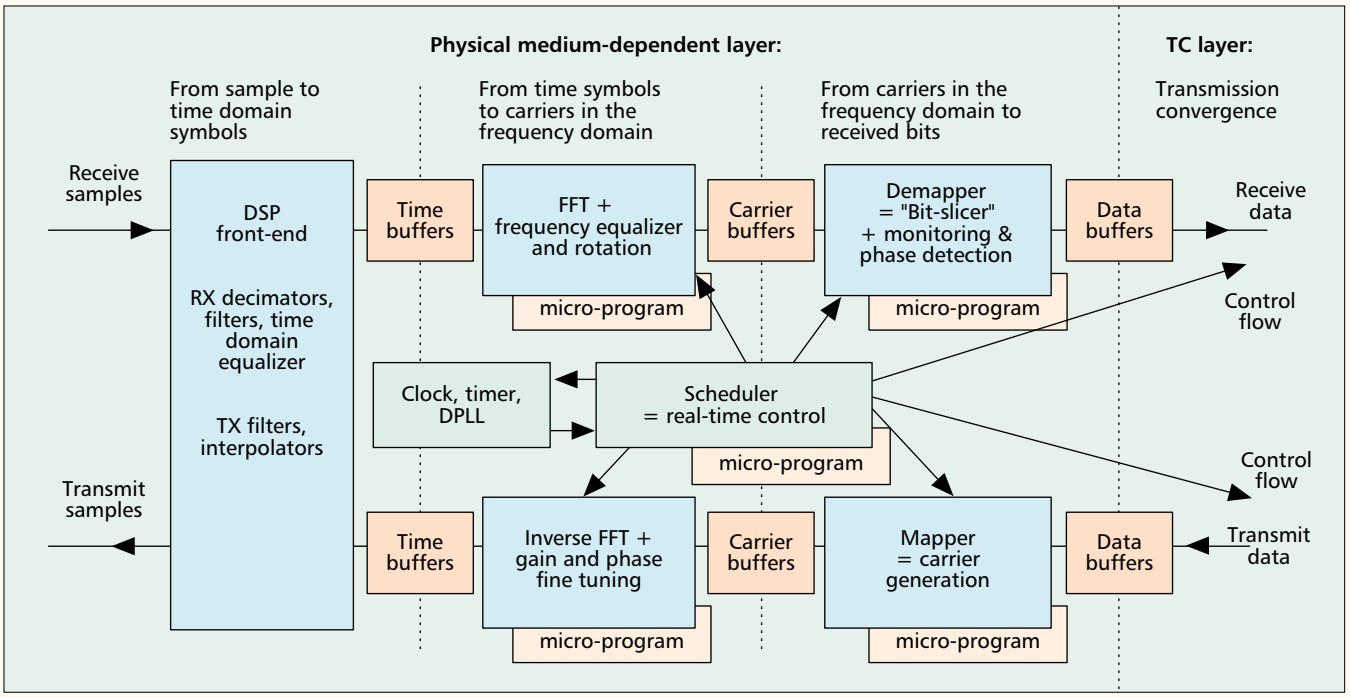


**Figure 5.** *The block diagram of the digital ADSL signal processor.*

in receive to equalize the signals distorted by the line. Moreover, the sampling speeds are increased by interpolation in the transmit direction and reduced by decimation in the receive direction.

- The FFT module transforms the arriving symbols from time to carrier domain. The inverse FFT does the opposite transformation. Additional functions are phase rotation and gain scaling.
- The mapper puts bits on carriers. The demapper/monitor is the "bit slicer": it decodes incoming symbols, and measures the amplitude and phase errors plus the noise on the carriers.

### Real-Time Intelligence of the DASP

In Fig. 5 the scheduler in the center controls the real-time behavior of the DASP. It is a RISC with a minimum number of commands. The behavior of each slave module can be determined via control lines and registers under control of the scheduler. The scheduler can also inspect the slave modules via dedicated registers or semaphores.

The scheduler further controls a programmable timer that counts samples, symbols, and DMT frames as defined in the ADSL standard. The scheduler reads this timer, and based on the downloaded schedules (i.e., its own micro-program) it commands all slave modules in the PMD (and TC) layer precisely when needed.

The external microcontroller will be used whenever the scheduler needs it. The dialog between scheduler and microcontroller is done via interrupts, with semaphores and short messages. When a slave module needs the next micro-program, the scheduler will warn the microcontroller, which loads it in a free RAM page of the slave. Then the microcontroller signals the completion of the download to the scheduler. As a result the scheduler will swap the program RAM page of the slave, which moves on to execute its next micro-program.

Figure 6 shows the clear separation between the top-level behavior of the microcontroller software, the firmware needed to download the micro-code, the individual micro-code segments in the hardware modules, and the schedules in the scheduling unit as well as the hardware interaction between the microcontroller, the scheduler, and the slave modules.

All this may look complicated, but in fact all actual transmit scheduler micro-programs needed to control the complete behavior of the ADSL modem for the 10 s of the initialization phase contain less than 256 RISC commands.

### The DASP Achievements

The DASP design achieved a modular structure, in which a number of real-time DSP functions were realized in silicon by the IC designers, avoiding DSP firmware. The modularity allowed the DASP design to start while the detailed content of some modules was still unspecified; moreover, the micro-programs could also be written and modified later.

- At the time the DASP specification was completed, only the low-level interaction between software and ASIC was specified; even the top-level design of the microcontroller software was started later.
- The modularity allowed several individual IC designers to work in parallel. The whole circuit design of the DASP was completed in less than nine months.

In general, the efficiency of the DASP is high in spite of a relatively slow clock:

- The DASP runs at a slow master clock of only 35 MHz, which reduces the general power consumption, while the MIPS are achieved by parallel processing.

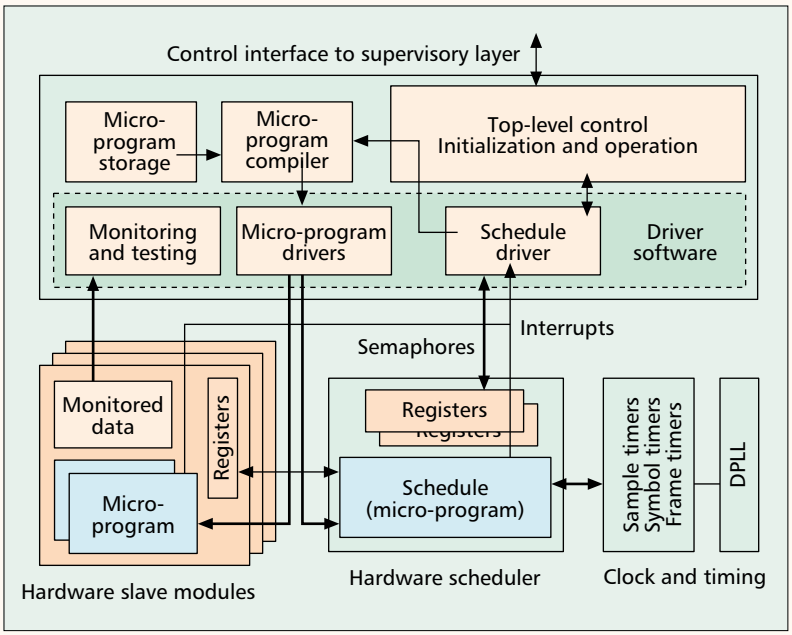


**Figure 6.** *Interaction of software modules in microprocessor and DASP.*

- All arithmetic units in the modules of the DASP have a load close to 100 percent, which results in very high efficiency.
- The equivalent MIPS over the silicon area ratio is higher than that of a DSP-based solution (whether using DSP cores or off-the-shelf DSP processors).

### The Evolution of ASICs

In successive generations the density of ASICs increased. The two large digital ASICS in 0.7 µm complementary metal oxide semiconductor (CMOS) of the first generation, for the PMD and TC layers, were merged in the second generation. In the third generation the SACHEM performed all digital transceiver functions in 450 kgates, with a size of 70 $mm^2$, 4.8 million transistors, 800 mW in 0.35 µm CMOS, and still only 35 MHz as master clock [8]. Also, the analog component has been optimized and shrunk [9]. Today the components at each side of the line are differentiated. At the central office (CO) multiple SACHEMs have been integrated in a single chip with power consumption per digital transceiver below 100 mW.

### Tracking the Evolution of the Standard

ADSL went from a conceptual definition in the early 1990s to widescale deployment in less than 10 years.[5] Very few products have grown at such a rapid pace ever.[6] The ADSL standard also evolved over these years. The microcontroller firmware and the micro-code of the SACHEM could be extended for the ADSL-lite variant defined in 1998, which required a new mode of operation called *fast retraining*. Also, the handshake procedure as standardized in 1999 in the International Telecommunication Union (ITU) was added to the firmware. Today the firmware can handle multiple variants automatically. Even the ADSL over ISDN variant could be supported with the same chipset (i.e., SACHEM + analog ASIC).

[5] *Mid-2001, more than 25 million ADSL lines had been sold worldwide.*

[6] *Most successful electronic consumption products or services such as the television, the Internet, and mobile phones took much longer!*

### Dedicated Chip Concepts also for VDSL

Also, for the Alcatel VDSL bit-pump the DASP architecture has been adopted. In a first realization DMT was used in combination with time-division duplexing. Today a standard-compliant FDD-DMT variant of VDSL again uses a similar architecture.

## Conclusions

This article describes an unconventional ADSL transceiver concept. The technical factors contributing to the success of this ADSL implementation were:

- Very early in the design phase, the easier frequency duplexing variant was chosen. This variant has been defended with success in standardization and the market.
- A DSP-based hardware emulator was built to validate design choices and optimize the algorithms and the analog front-end.
- Very quickly the design of dedicated ASICs was started: in 1992 and 1993 for the analog and digital ASICs, respectively. By the end of 1994, even before the first version of the ADSL standard was frozen, the ASICs were available on a functional board with the minimal software.
- The digital PMD ASIC contained DSP functions in hardware as dedicated RISC machines, with more optimal size and power consumption than a chip based on programmable DSP cores.
- The unique combination of high-level firmware on a standard microcontroller and downloadable micro-programs on the digital ASIC resulted in high efficiency. A single microcontroller could even serve many lines in parallel.
- In spite of the more hardware-oriented architecture, the micro-programmability offered enough flexibility, for example, for ADSL over ISDN and all other improvements in the standard.

### Acknowledgments

The authors thank the many colleagues with whom they enjoyed working on the feasibility studies, building the ASICs, hardware, and software, designing the algorithms, shaping the standards, and performing the tests and characterization of the product they made successful together.

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## BIOGRAPHIES

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PAUL SPRUYT is manager of the DSL modem team of Alcatel in Antwerp. He completed his M.Sc. degree in electronics at the University of Gent, Belgium, in 1985. He joined the Alcatel Research Center in 1989, where he first worked on equipment for ATM switching and transmission systems. Since 1992 he has been active in the R&D of ADSL and VDSL. He was also involved in high speed transmission over power lines and coaxial cables. Besides patents and articles on DSL, he also contributed to the standardization of ADSL and VDSL in ANSI T1E1.4 from 1995 to 1997. In 2000 he was awarded the Blondel Medal in France for his contribution to the development of ADSL and VDSL technology.