ANALOG DEVICES

CMOS 200 MHz
Quadrature Digital Upconverter

AD9856

FEATURES
**Universal Low Cost Modulator Solution for
  Communications Applications**
DC to 80 MHz Output Bandwidth
Integrated 12-Bit D/A Converter
Programmable Sample Rate Interpolation Filter
Programmable Reference Clock Multiplier
Internal SIN(X)/X Compensation Filter
>52 dB SFDR @ 40 MHz A_{OUT}
>48 dB SFDR @ 70 MHz A_{OUT}
>80 dB Narrowband SFDR @ 70 MHz A_{OUT}
+3 V Single Supply Operation
Space-Saving Surface-Mount Packaging
Bidirectional Control Bus Interface
Supports Burst and Continuous T_X Modes
Single Tone Mode for Frequency Synthesis Applications
Four Programmable, Pin-Selectable Modulator Profiles
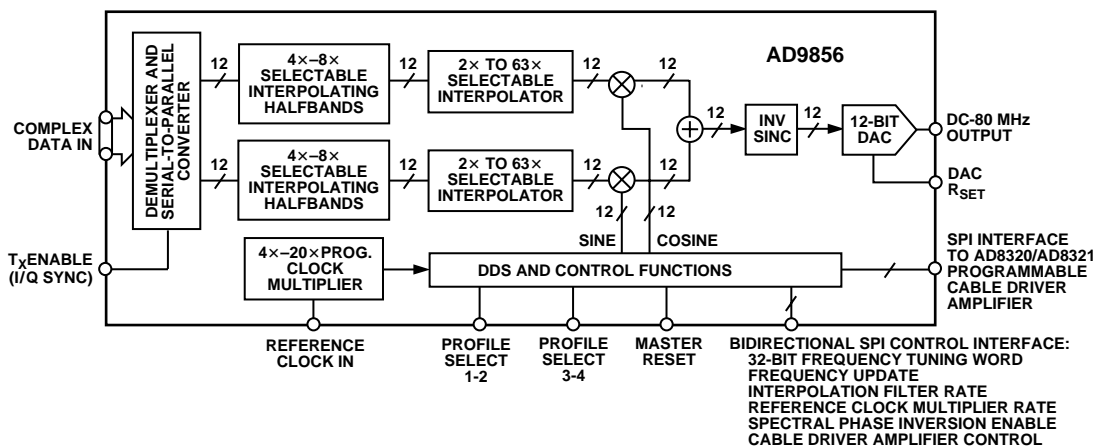**Direct Interface to AD8320/AD8321 PGA Cable Driver**

APPLICATIONS
HFC Data, Telephony and Video Modems
Wireless and Satellite Communications
Cellular Basestations

GENERAL DESCRIPTION
The AD9856 integrates a high speed direct-digital synthesizer (DDS), a high performance, high speed 12-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters and other DSP functions onto a single chip, to form a complete quadrature digital upconverter device. The AD9856 is intended to function as a universal I/Q modulator and agile upconverter for communications applications, where cost, size, power dissipation and dynamic performance are critical attributes.

The AD9856 is available in a space-saving surface mount package and specified to operate over the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

REV. A

AD9856–SPECIFICATIONS

Parameter	Temp	Test Level	Min	AD9856 Typ	Max	Units
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	5		200[1]	MHz
REFCLK Multiplier Enabled at 4×	Full	VI	5		50	MHz
REFCLK Multiplier Enabled at 20×	Full	VI	5		10	MHz
Duty Cycle	+25°C	V		50		%
Input Capacitance	+25°C	V		3		pF
Input Impedance	+25°C	V		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				12		Bits
Full-Scale Output Current			5	10	20	mA
Gain Error	+25°C	I	–10		+10	%FS
Output Offset	+25°C	I			10	µA
Differential Nonlinearity	+25°C	V		0.5		LSB
Integral Nonlinearity	+25°C	V		1		LSB
Output Capacitance	+25°C	V		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
REFCLK Multiplier Enabled at 20×	+25°C	V		–85		dBc/Hz
REFCLK Multiplier at 4×	+25°C	V		–100		dBc/Hz
REFCLK Multiplier Disabled	+25°C	V		–110		dBc/Hz
Voltage Compliance Range	+25°C	I	–0.5		1.5	V
Wideband SFDR:						
1 MHz Analog Out	+25°C	IV		70		dBc
20 MHz Analog Out	+25°C	IV		65		dBc
42 MHz Analog Out	+25°C	IV		60		dBc
65 MHz Analog Out	+25°C	IV		55		dBc
80 MHz Analog Out	+25°C	IV		50		dBc
Narrowband SFDR: (±100 kHz Window)						
70 MHz Analog Out	+25°C	IV		80		dBc
MODULATOR CHARACTERISTICS						
Adjacent Channel Power (CH Power = –6.98 dBm)	+25°C	IV	50			dBm
Error Vector Magnitude	+25°C	IV		1	2	%
I/Q Offset	+25°C	IV	50	55		dB
Inband Spurious Emissions	+25°C	IV	45	50		dBc
Pass Band Amplitude Ripple (DC to 80 MHz)	+25°C	V		±0.3		dB
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			10	MHz
Minimum Clock Pulsewidth High (t_{PWH})	Full	IV	30			ns
Minimum Clock Pulsewidth Low (t_{PWL})	Full	IV	30			ns
Maximum Clock Rise/Fall Time	Full	IV			1	ms
Minimum Data Setup Time (t_{DS})	Full	IV	25			ns
Minimum Data Hold Time (t_{DH})	Full	IV	0			ns
Maximum Data Valid Time (t_{DV})	Full	IV	30			ns
Wake-Up Time[2]	Full	IV			1	ms
Minimum RESET Pulsewidth High (t_{RH})	Full	IV	5			REFCLK Cycles
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	I	+2.6			V
Logic "0" Voltage	+25°C	I			+0.4	V
Logic "1" Current	+25°C	I			12	µA
Logic "0" Current	+25°C	I			12	µA
Input Capacitance	+25°C	V		3		pF

REV. A

Parameter	Temp	Test Level	AD9856			Units
			Min	Typ	Max	
CMOS LOGIC OUTPUTS (1 mA LOAD)						
Logic "1" Voltage	+25°C	I	2.7			mA
Logic "0" Voltage	+25°C	I			0.4	mA
POWER SUPPLY						
+V_S Current						
Full Operating Conditions[2]	+25°C	I			530	mA
Burst Operation (25%)	+25°C	I			450	mA
Single Tone Mode	+25°C	I			495	mA
160 MHz Clock	+25°C	I			445	mA
120 MHz Clock	+25°C	I			345	mA
Power-Down Mode	+25°C	I			2	mA

NOTES
[1]For 200 MHz operation in Modulation Mode at +85°C operating temperature, V_S must be +3 V min.
[2]Assuming 1.3 kΩ and 0.01 μF loop filter components.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature . . . .+165°C
Storage Temperature . . . . –65°C to +150°C
V_S . . . . +4 V
Operating Temperature . . . . –40°C to +85°C
Digital Inputs . . . . –0.7 V to +V_S
Lead Temperature (Soldering 10 sec) . . . .+300°C
Digital Output Current . . . . 5 mA
$θ_{JA}$ Thermal Impedance . . . . 38°C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS
Test Level

I – 100% Production Tested.

III – Sample Tested Only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9856AST	–40°C to +85°C	Thin Quad Flatpack	ST-48
AD9856/PCB	+25°C	Evaluation Board	

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9856 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
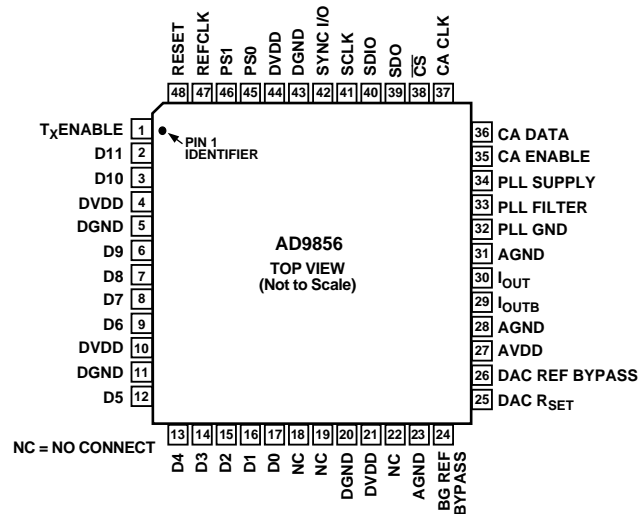
WARNING!

ESD SENSITIVE DEVICE

AD9856

PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	T_XENABLE	Input Pulse that Synchronizes the Data Stream
2	D11	Input Data (Most Significant Bit)
3	D10	Input Data
4, 10, 21, 44	DVDD	Digital Supply Voltage
5, 11, 20, 43	DGND	Digital Ground
6–9	D9–D6	Input Data
12–16	D5–D1	Input Data
17	D0	Input Data (Least Significant Bit)
18, 19, 22	NC	No Internal Connection
23, 28, 31	AGND	Analog Ground
24	BG REF BYPASS	No External Connection*
25	DAC R$_{SET}$	R$_{SET}$ Resistor Connection
26	DAC REF BYPASS	No External Connection*
27	AVDD	Analog Supply Voltage

Pin #	Pin Name	Pin Function
29	I$_{OUTB}$	Complementary Analog Current Output of the DAC
30	I$_{OUT}$	True Analog Current Output of DAC
32	PLL GND	PLL Ground
33	PLL FILTER	PLL Loop Filter Connection
34	PLL SUPPLY	PLL Voltage Supply
35	CA ENABLE	Cable Driver Amp Enable
36	CA DATA	Cable Driver Amp Data
37	CA CLK	Cable Driver Amp Clock
38	$\overline{CS}$	Chip Select
39	SDO	Serial Data Output
40	SDIO	Serial Port I/O
41	SCLK	Serial Port Clock
42	SYNC I/O	Performs I/O Synchronization
45	PS0	Profile Select 0
46	PS1	Profile Select 1
47	REFCLK	Reference Clock Input
48	RESET	Master Reset

*In most cases optimal performance is achieved with no external connection. For extremely noisy environments BG REF BYPASS can be bypassed with up to a 0.1 µF capacitor to AGND (Pin 23). DAC REF BYPASS can be bypassed with up to a 0.1 µF capacitor to AVDD (Pin 27).

PIN CONFIGURATION

REV. A

FUNCTIONAL BLOCK AND MODE DESCRIPTION

Operating Modes	1. Complex quadrature modulator mode. 2. Single tone output mode.
Input Data Format	Programmable: 12-bit, 6-bit, or 3-bit input formats. Data input to the AD9856 is 12-bit, twos complement. Complex I/Q symbol component data is required to be at least 2× oversampled, depending upon configuration.
Input Sample Rate	Up to 50 Msamples/s @ 200 MHz SYSCLK rate.
Input Reference Clock Frequency	For DC-80 MHz A_{OUT} operation (200 MHz SYSCLK rate): w/REFCLK Multiplier enabled: 10 MHz–50 MHz, programmable via control bus w/REFCLK Multiplier disabled: 200 MHz. Note: For optimum data synchronization, the AD9856 Reference Clock, and the input data clock, should be derived from the same clock source.
Internal Reference Clock Multiplier	Programmable in integer steps over the range of 4×–20×. Can be disabled (effective REFCLK Multiplier = 1) via control bus. Output of REFCLK Multiplier = SYSCLK rate, which is the internal clock rate applied to the DDS and DAC function.
Profile Select	Four pin-selectable, preprogrammed formats. Available for modulation and single tone operating modes.
Interpolating Range	Fixed 4×, selectable 2× and selectable 2×–63× range.
Half-Band Filters	Interpolating filters that provide upsampling and reduce the effects of the CIC passband roll-off characteristics.
T_XENABLE Function–Burst Mode	When Burst Mode is enabled via the control bus, the rising edge of the applied T_XENABLE pulse should be coincident with, and frame, the input data packet. This establishes data sampling synchronization.
T_XENABLE Function–Continuous Mode	When continuous mode is enabled via the control bus, the T_XENABLE pin becomes an I/Q control line. A Logic "1" on T_XENABLE indicates I data is being presented to the AD9856. A Logic "0" on T_XENABLE indicates Q data is being presented to the AD9856. Each rising edge of T_XENABLE resynchronizes the AD9856 input sampling capability.
Inverse SINC Filter	Precompensates for SIN(X)/X roll-off of DAC; user bypassable.
I/Q Channel Invert	$[I \times Cos(\omega t) + Q \times Sin(\omega t)]$ or $[I \times Cos(\omega t) - Q \times Sin(\omega t)]$ (default), configurable via control bus, per profile.
Full Sleep Mode	Power dissipation reduced to less than 6 mW when Full Sleep Mode active, programmable via control bus.

AD9856

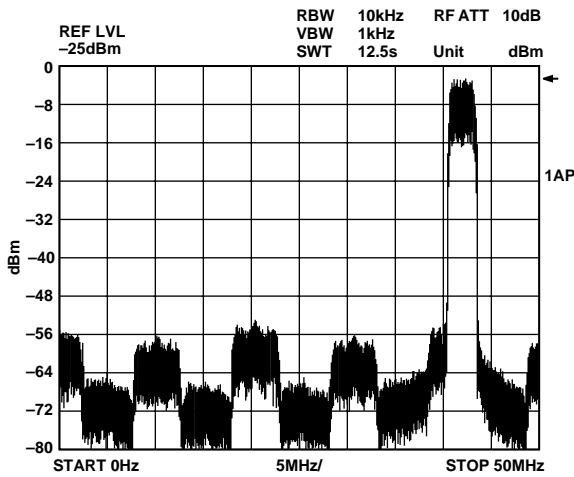## Typical Modulated Output Spectral Plots

Figure 1. QPSK at 42 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC = 3, HB3 On, 2× Data
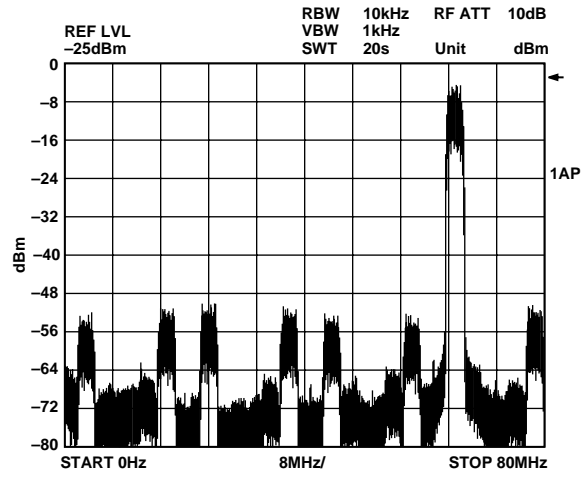

Figure 2. 64-QAM at 28 MHz and 6 MS/s; 36 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 3× Data

Figure 3. 16-QAM at 65 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC = 9, HB3 Off, 2× Data
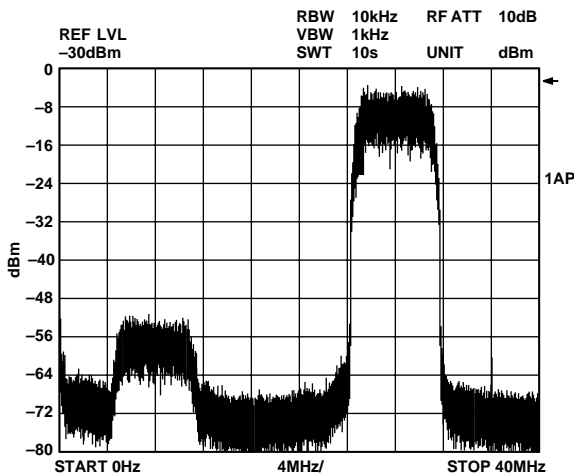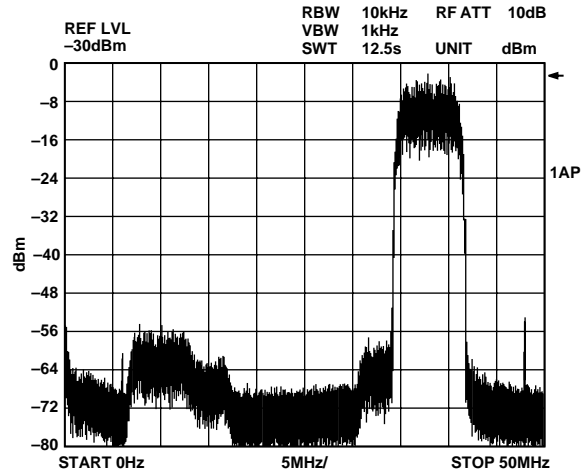

Figure 4. 256-QAM at 38 MHz and 6 MS/s; 48 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 4× Data

REV. A

Typical Single Tone Output Spectral Plots
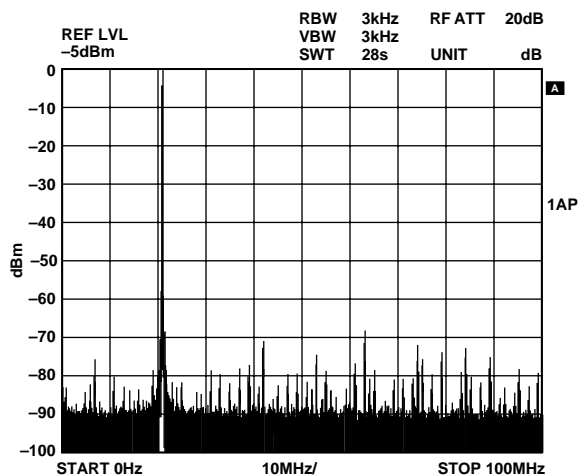
Figure 5. 21 MHz CW Output
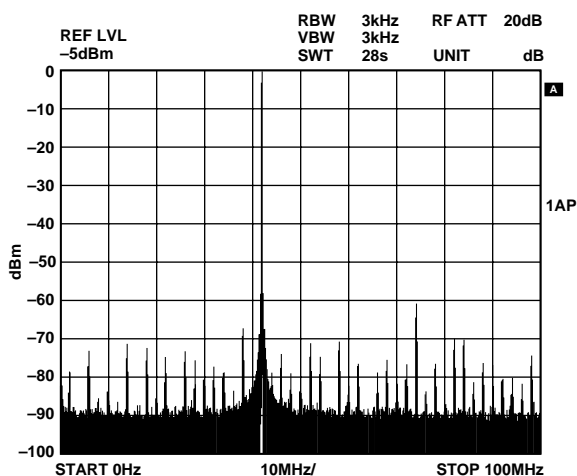
Figure 7. 42 MHz CW Output
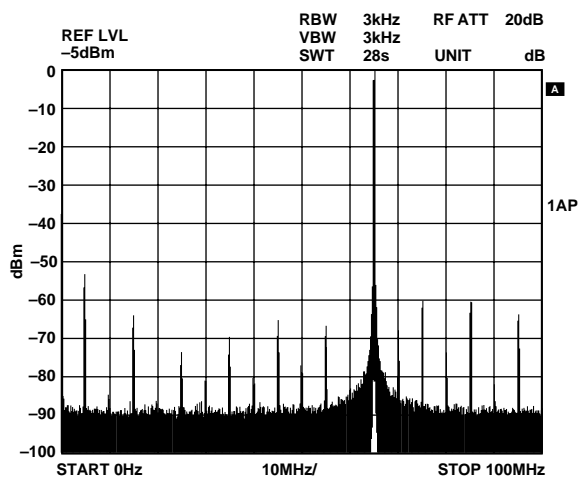
Figure 6. 65 MHz CW Output
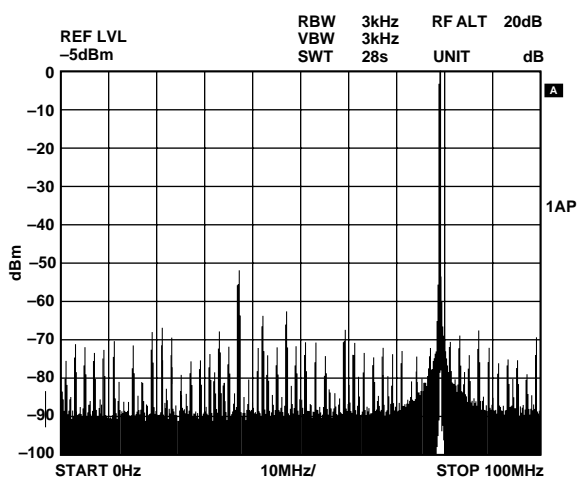
Figure 8. 79 MHz CW Output

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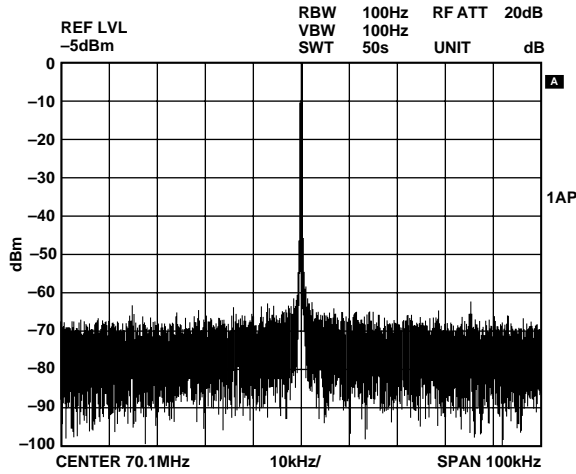## Typical Narrowband SFDR Spectral Plots

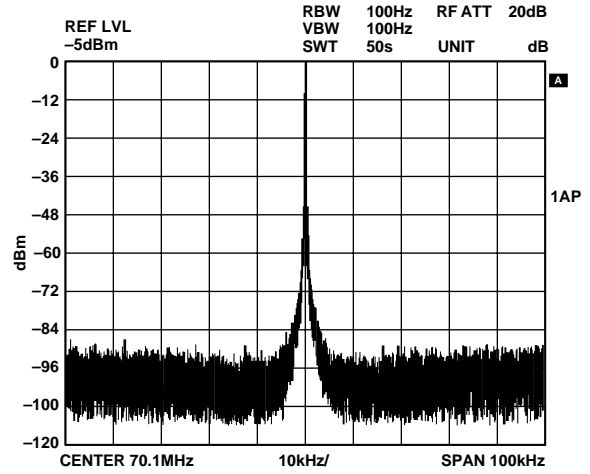Figure 9. 70.1 MHz Narrowband SFDR, 10 MHz External Clock with REFCLK Multiplier = 20×

Figure 11. 70.1 MHz Narrowband SFDR, 200 MHz External Clock with REFCLK Multiplier Disabled
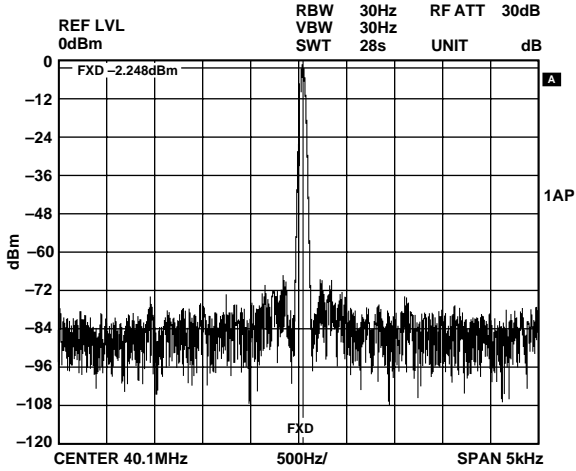
Typical Phase Noise Spectral Plots

Figure 10. 40.1 MHz Output, 10 MHz External Clock with REFCLK Multiplier = 20×
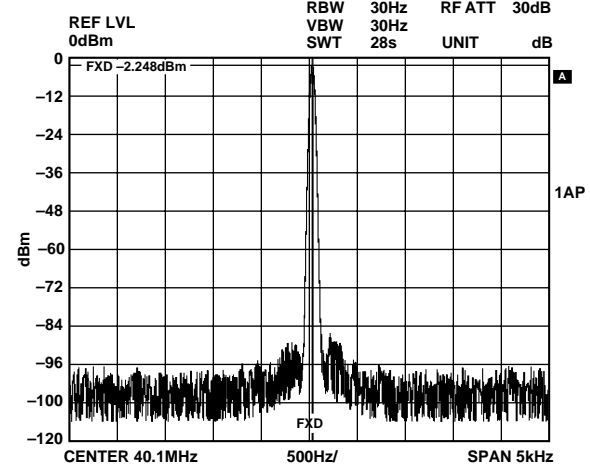

Figure 12. 40.1 MHz Output, 200 MHz External Clock with REFCLK Multiplier Disabled
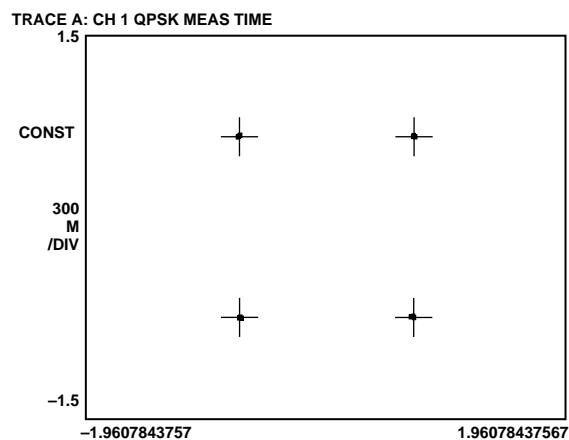
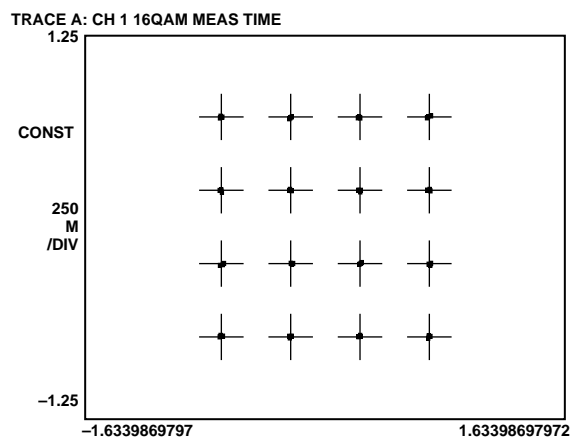# Typical Plots of Output Constellations

TRACE A: CH 1 QPSK MEAS TIME

Figure 13. QPSK, 65 MHz, 2.56 MS/s

TRACE A: CH 1 16QAM MEAS TIME

Figure 15. 16-QAM, 65 MHz, 2.56 MS/s

TRACE A: CH 1 64QAM MEAS TIME
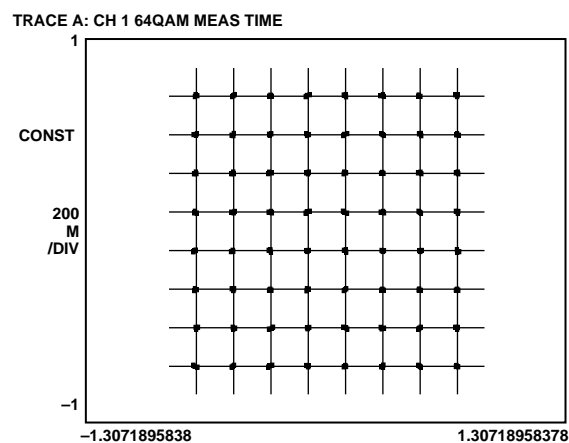
Figure 14. 64-QAM, 42 MHz, 6 MS/s

TRACE A: CH 1 256QAM MEAS TIME
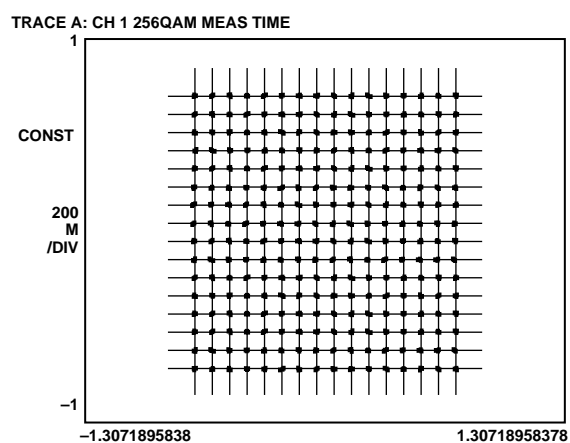
Figure 16. 256-QAM, 42 MHz, 6 MS/s

TRACE A: CH 1 MSK1 MEAS TIME

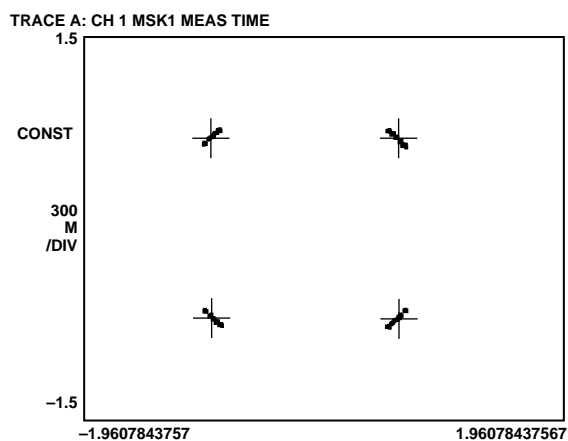*Figure 17. GMSK Modulation, 13 MS/s*

Power Consumption

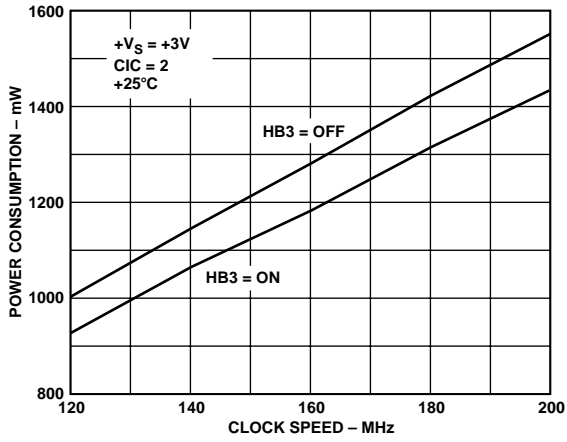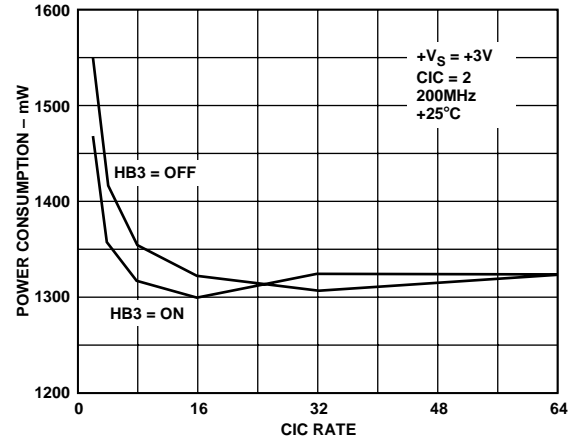Figure 18. Power Consumption vs. Clock Speed; $+V_S = +3\ V$, CIC = 2, +25°C

Figure 19. Power Consumption vs. CIC Rate; $+V_S = +3\ V$, 200 MHz, +25°C
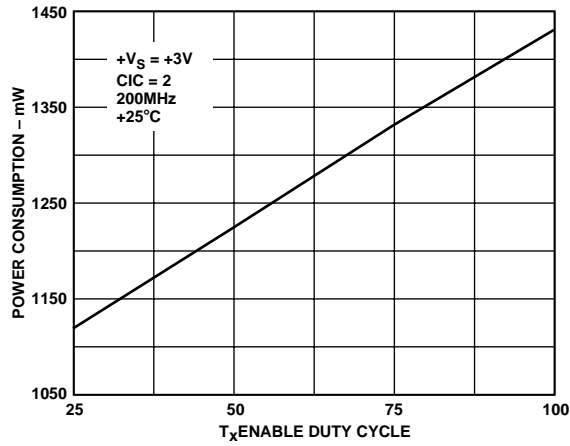

Figure 20. Power Consumption vs. Burst Duty Cycle; $+V_S = +3\ V$, CIC = 2, 200 MHz, +25°C

Table I. Serial Control Bus Register Layout

Register Address (hex)	AD9856 Register Layout								Default (hex)	Profile
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
00	SDO Active	LSB First	REFCLK Mult.<4>	REFCLK Mult.<3>	REFCLK Mult.<2>	REFCLK Mult.<1>	REFCLK Mult.<0>	Reserved	15	N/A
01	CIC Gain	Continuous Mode	Full Sleep Mode	Single Tone Mode	Bypass Inverse Sinc Filter	Bypass REFCLK Mult.	Input Format Select <1>	Input Format Select <0>	06	N/A
02	Frequency Tuning Word <7:0>								04	1
03	Frequency Tuning Word <15:8>								00	1
04	Frequency Tuning Word <23:16>								00	1
05	Frequency Tuning Word <31:24>								00	1
06	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	FC	1
07	AD8320/AD8321 Gain Control Bits <7:0>								00	1
08	Frequency Tuning Word <7:0>								00	2
09	Frequency Tuning Word <15:8>								00	2
0A	Frequency Tuning Word <23:16>								00	2
0B	Frequency Tuning Word <31:24>								80	2
0C	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	1E	2
0D	AD8320/AD8321 Gain Control Bits <7:0>								00	2
0E	Frequency Tuning Word <7:0>								Unset	3
0F	Frequency Tuning Word <15:8>								Unset	3
10	Frequency Tuning Word <23:16>								Unset	3
11	Frequency Tuning Word <31:24>								Unset	3
12	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	Unset	3
13	AD8320/AD8321 Gain Control Bits <7:0>								00	3
14	Frequency Tuning Word <7:0>								Unset	4
15	Frequency Tuning Word <15:8>								Unset	4
16	Frequency Tuning Word <23:16>								Unset	4
17	Frequency Tuning Word <31:24>								Unset	4
18	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	Unset	4
19	AD8320/AD8321 Gain Control Bits <7:0>								00	4

AD9856

REGISTER BIT DEFINITIONS
Control Bits—Register Address 00h and 01h

SDO Active—Register Address 00h, Bit 7. Active high indicates serial port uses dedicated in/out lines. Default low configures serial port as single line I/O.

LSB First—Register Address 00h, Bit 6. Active high indicates serial port access is LSB to MSB format. Default low indicates MSB to LSB format.

REFCLK Multiplier—Register Address 00h, Bits 5, 4, 3, 2, 1 form the reference clock multiplier. Valid entries range from 4–20 (decimal). Straight binary to decimal conversion is implemented. For example, to multiply the reference clock by 19 decimal, Program Register Address 00h, Bits 5–1, as 13h. Default value is 0A (hex).

RESERVED BIT—Register Address 00h, Bit 0. This bit is reserved. Always set this bit to Logic 1 when writing to this register.

CIC GAIN—Register Address 01h, Bit 7. The CIC GAIN bit multiplies the CIC filter output by 2. See the Cascaded Integrated Comb Filter section of this data sheet for more details. Default value is 0 (inactive).

CONTINUOUS MODE—Register Address 01h, Bit 6 is the continuous mode configuration bit. Active high, configures the AD9856 to accept continuous mode timing on the T_XENABLE input. A low configures the device for burst mode timing. Default value is 0 (burst mode).

FULL SLEEP MODE—Register Address 01h, Bit 5. Active high full sleep mode bit. When activated, the AD9856 enters a full shutdown mode, consuming less than 2 mA, after completing a shutdown sequence. Default value is 0 (awake).

SINGLE TONE MODE—Register Address 01h, Bit 4. Active high configures the AD9856 for single tone applications. The AD9856 will supply a single frequency output as determined by the frequency tuning word (FTW) selected by the active profile. In this mode, the 12 input data pins are ignored but should be tied high or low. Default value is 0 (inactive).

BYPASS INVERSE SINC FILTER—Register Address 01h, Bit 3. Active high, configures the AD9856 to bypass the SIN(X)/X compensation filter. Defaults value is 0 (Inverse SINC Filter Enabled).

BYPASS REFCLK Multiplier—Register Address 01h, Bit 2. Active high, configures the AD9856 to bypass the REFCLK Multiplier function. When active, effectively causes the REFCLK Multiplier factor to be 1. Defaults value is 1 (REFCLK Multiplier bypassed).

INPUT FORMAT SELECT—Register Address 01h, Bits 1 and 0, form the Input Format Mode bits.
   10b = 12-bit mode
   01b = 6-bit mode
   00b = 3-bit mode
   Default value is 10b (12-bit mode).

Profile 1 Registers—Active when PROFILE Inputs Are 00b
FREQUENCY TUNING WORD (FTW)—The frequency tuning word for Profile 1 is formed via a concatenation of register addresses 05h, 04h, 03h and 02h. Bit 7 of register address 05h is the most significant bit of the Profile 1 frequency tuning word. Bit 0 of register address 02h is the least significant bit of the Profile 1 frequency tuning word. The output frequency equation is given as: $f_{OUT} = (FTW \times SYSCLK)/2^{32}$.

INTERPOLATION RATE—Register Address 06h, Bits 7 through 2 form the Profile 1 CIC filter interpolation rate value. Allowed values range from 2 to 63 (decimal).

SPECTRAL INVERSION—Register Address 06h, Bit 1. Active high, Profile 1 Spectral Inversion bit. When active, inverted modulation is performed $[I \times Cos(\omega t) + Q \times Sin(\omega t)]$. Default is inactive, logic zero, noninverted modulation $[I \times Cos(\omega t) - Q \times Sin(\omega t)]$.

BYPASS HALF-BAND FILTER 3—Register Address 06h, Bit 0. Active high, causes the AD9856 to bypass the third half-band filter stage that precedes the CIC interpolation filter. Bypassing the third half-band filter negates the 2× upsample inherent with this filter and reduces the overall interpolation rate of the half-band filter chain from 8× to 4×. Default value is 0 (half-band 3 enabled).

AD8320/AD8321 GAIN CONTROL—Register Address 07h, Bits 7 through 0 form the Profile 1 AD8320/AD8321 gain bits. The AD9856 dedicates three output pins, which directly interface to the AD8320/AD8321 cable driver amp. This allows direct control of the cable driver via the AD9856. See the Programming/Writing the AD8320/AD8321 Cable Driver Gain Control section of this data sheet for more details. Bit 7 is the MSB, Bit 0 is the LSB. Default value is 00h.

Profile 2 Registers—Active when PROFILE Inputs Are 01b
Profile 2 Register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 3 Registers—Active when PROFILE Inputs Are 10b
Profile 3 Register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 4 Registers—Active when PROFILE Inputs Are 11b
Profile 4 Register functionality is identical to Profile 1, with the exception of the register addresses.

THEORY OF OPERATION

To gain a general understanding of the functionality of the AD9856 it is helpful to refer to Figure 21, which displays a block diagram of the device architecture. The following is a general description of the device functionality. Later sections will detail each of the data path building blocks.

Modulation Mode Operation

The AD9856 accepts 12-bit data words, which are strobed into the Data Assembler via an internal clock. The input, T$_X$ENABLE, serves as the "valve" which allows data to be accepted or ignored by the Data Assembler. The user has the option to feed the 12-bit data words to the AD9856 as single 12-bit words, dual 6-bit words, or quad 3-bit words. This provides the user with the flexibility to use fewer interface pins, if so desired. Furthermore, the incoming data is assumed to be complex, in that alternating 12-bit words are regarded as the inphase (I) and quadrature (Q) components of a symbol.

The rate at which the 12-bit words are presented to the AD9856 will be referred to as the Input Sample Rate (f$_{IN}$). It should be pointed out that f$_{IN}$ is not the same as the baseband data rate provided by the user. As a matter of fact, it is required that the user's baseband data be upsampled by at least a factor of two (2) before being applied to the AD9856 in order to minimize the frequency-dependent attenuation associated with the CIC filter stage (detailed in a later section).

The Data Assembler splits the incoming data word pairs into separate I/Q data streams. The rate at which the I/Q data word pairs appear at the output of the Data Assembler will be referred to as the I/Q Sample Rate (f$_{IQ}$). Since two 12-bit input data words are used to construct the individual I and Q data paths, it should be apparent that the input sample rate is twice the I/Q sample rate (i.e., f$_{IN}$ = 2 × f$_{IQ}$).

Once through the Data Assembler, the I/Q data streams are fed through two half-band filters (half-band filters #1 and #2). The combination of these two filters results in a factor of four (4) increase of the sample rate. Thus, at the output of half-band filter #2, the sample rate is 4 × f$_{IQ}$. In addition to the sample rate increase, the half-band filters provide the low-pass filtering characteristic necessary to suppress the spectral images produced by the upsampling process. Further upsampling is available via an optional third half-band filter (half-band filter #3). When selected, this provides an overall upsampling factor of eight (8). Thus, if half-band filter #3 is selected, then the sample rate at its output is 8 × f$_{IQ}$.

After passing through the half-band filter stages, the I/Q data streams are fed to a Cascaded Integrator-Comb (CIC) filter. This filter is configured as an interpolating filter, which allows further upsampling rates of any integer value between 2 and 63, inclusive. The CIC filter, like the half-bands, has a built-in low-pass characteristic. Again, this provides for suppression of the spectral images produced by the upsampling process.

The digital quadrature modulator stage following the CIC filters is used to frequency shift the baseband spectrum of the incoming data stream up to the desired carrier frequency (this process is known as *upconversion*). The carrier frequency is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS uses its internal reference clock (SYSCLK) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that is the modulated carrier. It should be noted at this point that the incoming data has been converted from an input sample rate of f$_{IN}$ to an output sample rate of SYSCLK (see the block diagram).

The sampled carrier is ultimately destined to serve as the input data to the digital-to-analog converter (DAC) integrated on the AD9856. The DAC output spectrum is distorted due to the intrinsic zero-order hold effect associated with DAC-generated signals. This distortion is deterministic, however, and follows the familiar SIN(X)/X (or SINC) envelope. Since the SINC distortion is predictable, it is also correctable. Hence, the presence of the optional Inverse SINC filter preceding the DAC. This is a FIR filter, which has a transfer function conforming to the inverse of the SINC response. Thus, when selected, it modifies the incoming data stream so that the SINC distortion, which would otherwise appear in the DAC output spectrum is virtually eliminated.

As mentioned earlier, the output data is sampled at the rate of SYSCLK. Since the AD9856 is designed to operate at SYSCLK frequencies up to 200 MHz, there is the potential difficulty of trying to provide a stable input clock (REFCLK). Although stable, high frequency oscillators are available commercially they tend to be cost prohibitive. To alleviate this problem, the AD9856 has a built-in programmable clock multiplier circuit. This allows the user to use a relatively low frequency (thus, less expensive) oscillator to generate the REFCLK signal. The low frequency REFCLK signal can then be multiplied in frequency by an integer factor of between 4 and 20, inclusive, to become the SYSCLK signal.
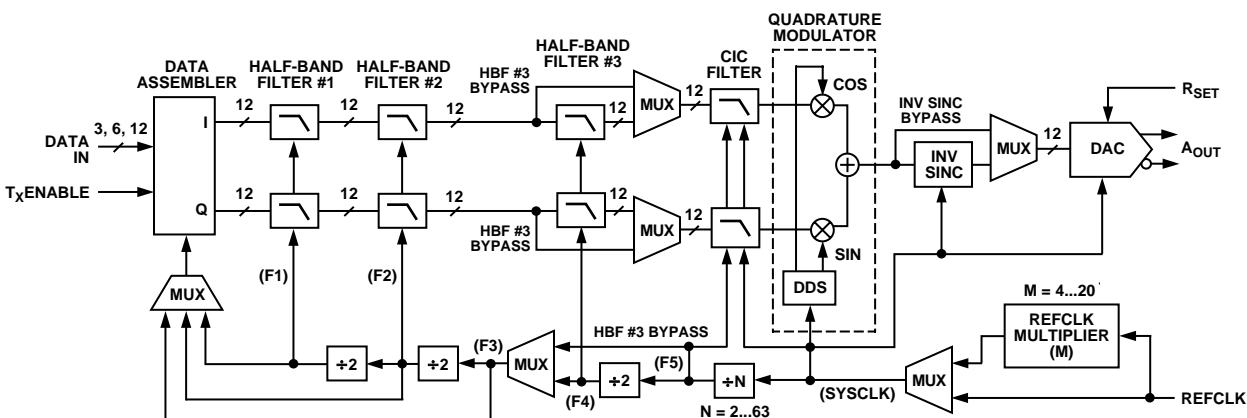

Figure 21. AD9856 Block Diagram

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Single Tone Output Operation

The AD9856 can be configured for frequency synthesis applications by writing the single tone bit true. In single tone mode, the AD9856 disengages the modulator and preceding datapath logic to output a spectrally pure single frequency sine wave. The AD9856 provides for a 32-bit frequency tuning word, which results in a tuning resolution of 0.046 Hz at a SYSCLK rate of 200 MHz.

A good rule of thumb when using the AD9856 as a frequency synthesizer is to limit the fundamental output frequency to 40% of SYSCLK. This avoids generating aliases too close to the desired fundamental output frequency, thus minimizing the cost of filtering the aliases.

All applicable programming features of the AD9856 apply when configured in single tone mode. These features include:

1. Frequency hopping via the PROFILE inputs and associated tuning word, which allows Frequency Shift Keying (FSK) modulation.
2. Ability to bypass the REFCLK Multiplier, which results in lower phase noise and reduced output jitter.
3. Ability to bypass the SIN(X)/X compensation filter.
4. Full power-down mode.

INPUT WORD RATE (f_W) vs. REFCLK RELATIONSHIP

There is a fundamental relationship between the input word rate (f_W) and the frequency of the clock that serves as the timing source for the AD9856 (REFCLK). f_W is defined as the rate at which K-bit data words (K = 3, 6 or 12) are presented to the AD9856. There are, however, a number of factors that affect this relationship. They are:

- The interpolation rate of the CIC filter stage.
- Whether or not Half-Band Filter #3 is bypassed.
- The value of REFCLK Multiplier (if selected).
- Input Word Length.

This relationship can be summed up with the following equation:

$$REFCLK = (2\ HNf_W)/MI$$

Where H, N, I and M are integers and are determined as follows:

$$
\begin{array}{llll}
H & = & | \ 1: & \text{Half-Band Filter \#3 Bypassed} \\
  &   & | \ 2: & \text{Half-Band Filter \#3 Enabled} \\
M & = & | \ 1: & \text{REFCLK Multiplier Bypassed} \\
  &   & | \ 4 \le M \le 20: & \text{REFCLK Multiplier Enabled} \\
I & = & | \ 1: & \text{Full Word Input Format} \\
  &   & | \ 2: & \text{Half Word Input Format} \\
  &   & | \ 4: & \text{Quarter Word Input Format} \\
N & = & \text{CIC interpolation rate } (2 \le N \le 63) &
\end{array}
$$

It should be obvious from these conditions that REFCLK and f_W have an integer ratio relationship. It is of utmost importance that the user chooses a value of REFCLK, which will ensure that this integer ratio relationship is maintained.

I/Q DATA SYNCHRONIZATION

As mentioned above, the AD9856 accepts I/Q data pairs, twos complement numbering system, in three different word length modes. The full word mode accepts 12-bit parallel I and Q data. The half word mode accepts dual 6-bit I and Q data inputs to

form a 12-bit word. The quarter word mode accepts multiple 3-bit I and Q data inputs to form a 12-bit word. For all word length modes, the AD9856 assembles the data for signal processing into time aligned, parallel 12-bit I/Q pairs. In addition to the word length flexibility, the AD9856 operates in two "input timing" modes, burst or continuous, programmable via the serial port.

For burst mode input timing, no external data clock needs to be provided as the data is oversampled at the D<11:0> pins using the system clock (SYSCLK). The T_XENABLE pin is required to frame the data burst as the rising edge of T_XENABLE is used to synchronize the AD9856 to the input data rate. The AD9856 registers the input data at the approximate center of the data valid time. It should be obvious that for larger CIC interpolation rates, more SYSCLK cycles are available to oversample the input data, maximizing clock jitter tolerances.

For continuous mode input timing, the T_XENABLE pin can be thought of as a data input clock running at 1/2 the input sample rate (f_W/2). In addition to synchronization, for continuous mode timing, the T_XENABLE input indicates to the AD9856 whether an I or Q input is being presented to the D<11:0> pins. It is intended that data is presented in alternating fashion such that I data is followed by Q data. Stated another way, the T_XENABLE pin should maintain approximately a 50/50 duty cycle. As in burst mode, the rising edge of T_XENABLE synchronizes the AD9856 to the input data rate and the data is registered at the approximate center of the data valid time. The continuous operating mode can only be used in conjunction with the full word input format.

Burst Mode Input Timing

Figures 22–26 describe the input timing relationship between T_XENABLE and the 12-bit input data word for all three input format modes when the AD9856 is configured for burst input timing. Also shown in these diagrams is the time-aligned, 12-bit parallel I/Q data as assembled by the AD9856.

Figure 22 describes the classic burst mode timing, for full word input mode, in which T_XENABLE frames the input data stream. Note that sequential input of alternating I/Q data, starting with I data, is required.

The input sample rate for full word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/4N$$

where N is the CIC interpolation rate.

The input sample rate for full word mode, when the third half-band filter is not engaged is given by:

$$f_{IN} = SYSCLK/2N$$

where N is the CIC interpolation rate

Figure 23 describes an alternate timing method for T_XENABLE when the AD9856 is configured in full word, burst mode operation. The benefit of this timing is that the AD9856 will resynchronize the input sampling logic when the rising edge of T_XENABLE is detected. The low time on T_XENABLE is limited to one input sample period and must be low during the Q data period. The maximum high time on T_XENABLE is unlimited. It should be clear that unlimited high time on T_XENABLE results in the timing diagram of Figure 22. See Figure 26 for the ramifications of violating the T_XENABLE low time constraint when operating in burst mode.

Figure 24 describes the input timing for half word mode, burst input timing operation.

In half word mode, data is input on the D<11:6> inputs. The D<5:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:6>,I<5:0>,Q<11:6>,Q<5:0>. Data is twos complement, the sign bit is D<11> in notation I<11:0>,Q<11:0>.

The input sample rate for half word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/2N$$

where N is the CIC interpolation rate.

The input sample rate for half word mode, when the third half-band filter is not engaged is given by:

$$f_{IN} = SYSCLK/N$$

where N is the CIC interpolation rate.

Figure 25 describes the input timing for quarter word, burst input timing operation.

In quarter word mode, data is input on the D<11:9> inputs. The D<8:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:9>, I<8:6>, I<5:3>, I<2:0>, Q<11:9>, Q<8:6>, Q<5:3>, Q<2:0>. Data is twos complement, the sign bit is D<11> in notation I<11:0>, Q<11:0>.

The input sample rate for quarter word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/N$$

where N is the CIC interpolation rate.

Please note that Half-Band Filter #3 must be engaged when operating in quarter word mode.
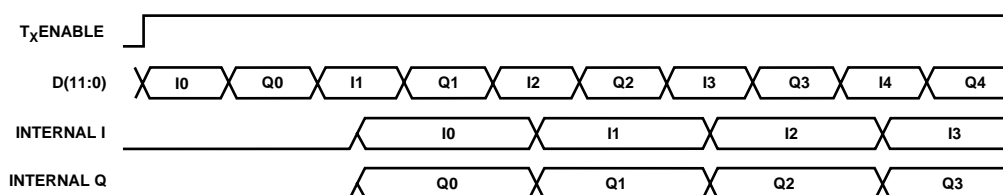

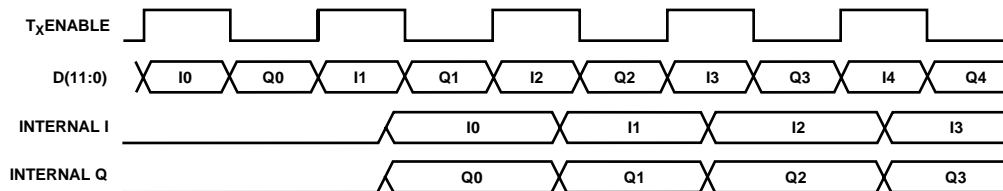Figure 22. 12-Bit Input Mode, Classic Burst Timing

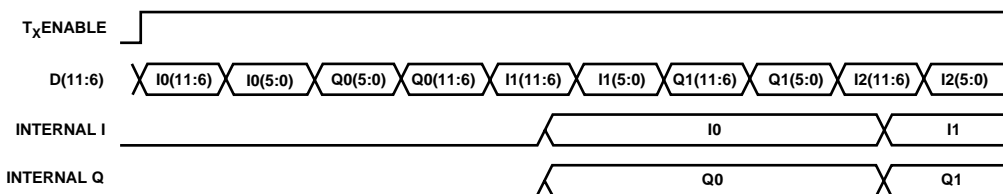Figure 23. 12-Bit Input Mode, Alternate T_XENABLE Timing

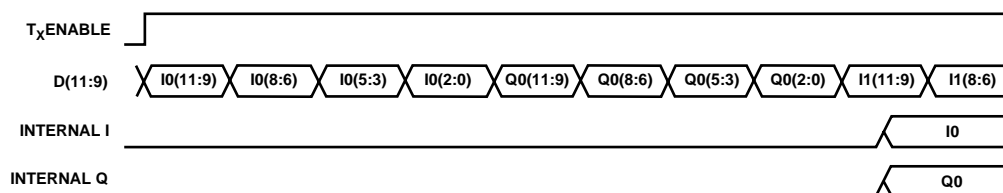Figure 24. 6-Bit Input Mode, Burst Mode Timing

Figure 25. 3-Bit Input Mode, Burst Mode Timing

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Figure 26 describes the end of burst timing and internal data assembly. It's important to note that in burst mode operation, if the $T_XENABLE$ input is low for more than one input sample period, numerical zeros are internally generated and passed to the data path logic for signal processing. This is not valid for continuous mode operation, as will be discussed later.

To ensure proper operation, the minimum time between falling and rising edges of $T_XENABLE$ is one input sample period.

Continuous Mode Input Timing
The AD9856 is configured for continuous mode input timing by writing the Continuous Mode bit true (Logic 1). The Continuous Mode bit is in register address 01h, Bit 6. The AD9856 must be configured for full word input format when operating in continuous mode input timing. The input data rate equations

described above, for full word mode, apply for continuous mode. Figure 22, which is the alternate burst mode timing diagram, is also the continuous mode input timing. Figures 27 and 28 describe what the internal data assembler will present to the signal processing logic when the $T_XENABLE$ input is held static for greater than one input sample period. Please note that the timing diagram of Figures 27 and 28 detail INCORRECT timing relationships between $T_XENABLE$ and data. They are only presented to indicate that the AD9856 will resynchronize properly after detecting a rising edge of $T_XENABLE$. It should also be noted that the significant difference between burst and continuous mode operation is that in addition to synchronizing the data, $T_XENABLE$ is used to indicate whether an I or Q input is being sampled.
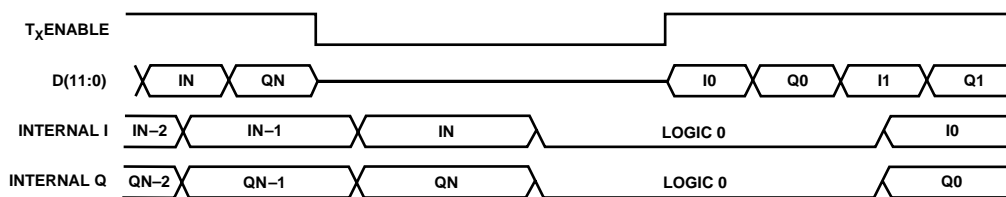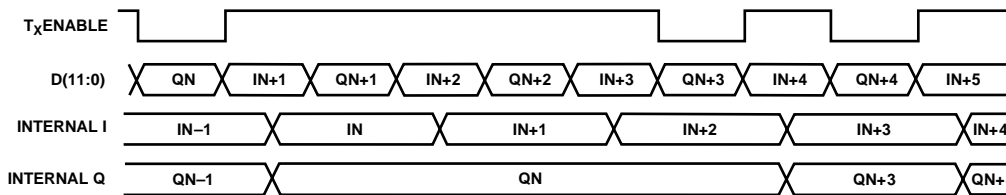
Figure 26. Burst Mode Input Timing—End of Burst

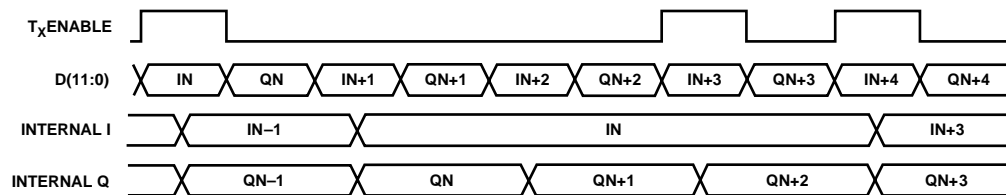*Figure 27. Continuous Mode Input Timing—$T_XENABLE$ Static High*

Figure 28. Continuous Mode Input Timing—$T_XENABLE$ Static Low

HALF-BAND FILTERS (HBFs)

Before presenting a detailed description of the HBFs, recall that the input data stream is representative of complex data; i.e., two input samples are required to produce one I/Q data pair. The I/Q sample rate is one-half the input data rate. The I/Q sample rate (the rate at which I or Q samples are presented to the input of the first half-band filter) will be referred to as f_{IQ}. Since the AD9856 is a quadrature modulator, f_{IQ} represents the baseband of the internal I/Q sample pairs. It should be emphasized here that f_{IQ} is not the same as the baseband of the user's symbol rate data, which must be upsampled before presentation to the AD9856 (as will be explained later). The I/Q sample rate (f_{IQ}) puts a limit on the minimum bandwidth necessary to transmit the f_{IQ} spectrum. This is the familiar Nyquist limit and is equal to one-half f_{IQ}, which hereafter will be referred to as f_{NYQ}.

HBF 1 is a 47-tap filter that provides a factor-of-two increase in sampling rate. HBF 2 is a 15-tap filter offering an additional factor-of-two increase in sampling rate. Together, HBF 1 and 2 provide a factor-of-four increase in the sampling rate ($4 \times f_{IQ}$ or $8 \times f_{NYQ}$). Their combined insertion loss is a mere 0.01 dB, so virtually no loss of signal level occurs through the first two HBFs. HBF 3 is an 11-tap filter and, if selected, increases the sampling rate by an additional factor of two. Thus, the output sample rate of HBF 3 is $8 \times f_{IQ}$ or $16 \times f_{NYQ}$. HBF 3 exhibits 0.03 dB of signal level loss. As such, the loss in signal level through all three HBFs is only 0.04 dB and may be ignored for all practical purposes.

In relation to phase response, all three HBFs are linear phase filters. As such, virtually no phase distortion is introduced within the passband of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

In addition to knowledge of the insertion loss and phase response of the HBFs, some knowledge of the frequency response of the HBFs is useful as well. The combined frequency response of HBF 1 and 2 is shown in Figure 29.

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9856. A look at the passband detail of the HBF 1 and 2 response indicates that in order to maintain an amplitude error of no more than 1 dB, we are restricted to signals having a bandwidth of no more than about 90% of f_{NYQ}. Thus, in order to keep the bandwidth of the data in the flat portion of the filter passband, the user must oversample the baseband data by at least a factor of two prior to presenting it to the AD9856. Note that without oversampling, the Nyquist bandwidth of the baseband data corresponds to the f_{NYQ}. As such, the upper end of the data bandwidth will suffer 6 dB or more of attenuation due to the frequency response of HBF 1 and 2. Furthermore, if the baseband data applied to the AD9856 has been pulse shaped there is an additional concern. Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that $0 \leq \alpha \leq 1$. A value of 0

causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and $\alpha = 1$, the Nyquist bandwidth of the data will correspond with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the frequency response of HBF 1 and 2.
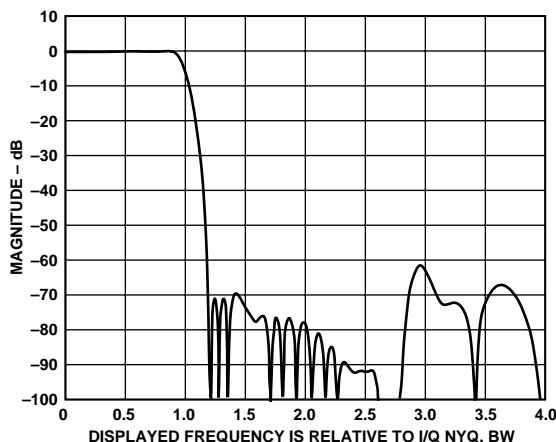
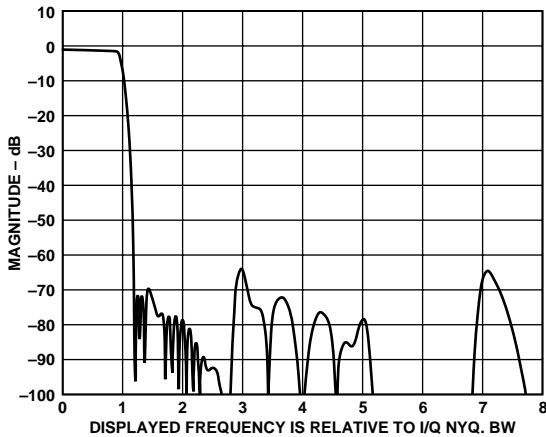*a. Half-Band 1 and 2 Frequency Response*
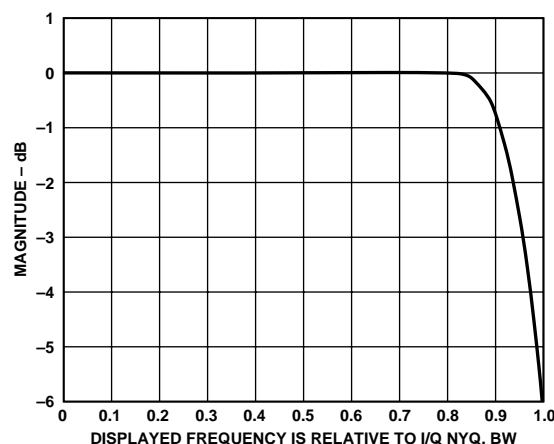
b. Passband Detail

Figure 29. Combined Frequency Response of HBF 1 and 2

To reiterate, the user must *oversample* their baseband data by at least a *factor of two* (2). In addition, there is a further restriction on pulse shaping. That is, the maximum value of α that can be implemented is 0.8. This is because the data bandwidth becomes: $1/2(1 + \alpha) \, f_{NYQ} = 0.9 \, f_{NYQ}$, which puts the data bandwidth at the extreme edge of the flat portion of the filter response. If a particular application requires an α value between 0.8 and 1, then the user must *oversample* the baseband data by at least a *factor of four* (4).

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In applications requiring both a low data rate and a high output sample rate, a third HBF is available (HBF 3). Selection of HBF 3 offers an upsampling ratio of eight (8) instead of four (4). The combined frequency response of HBF 1, 2 and 3 is shown in Figure 30. Comparing the passband detail of HBF 1 and 2 with the passband detail of HBF 1, 2 and 3, it becomes evident that HBF 3 has virtually no impact on frequency response from 0 to 1 (where 1 corresponds to f_{NYQ}).

a. Half-Band 1, 2 and 3 Frequency Response
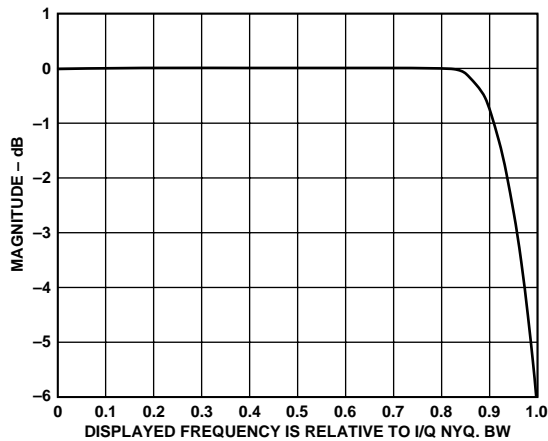
b. Passband Detail

Figure 30. Combined Frequency Response of HBF 1, 2 and 3

CASCADED INTEGRATOR-COMB (CIC) FILTER

A CIC filter is unlike a typical FIR filter in that it offers the flexibility to handle differing input and output sample rates (only in integer ratios, however). In the purest sense, a CIC filter can provide either an increase or a decrease in sample rate at the output relative to the input, depending on the architecture. If the integration stage precedes the comb stage, the CIC filter provides sample rate reduction (*decimation*). When the comb stage precedes the integrator stage the CIC filter provides an increase in sample rate (*interpolation*). In the AD9856, the CIC filter is configured as an interpolator. In fact, it is a programmable interpolator and provides a sample rate increase, R, such that $2 \le R \le 63$.

In addition to the ability to provide a change in sample rate between input and output, a CIC filter also has an intrinsic low-pass frequency response characteristic. The frequency response of a CIC filter is dependent on three factors:

1. The rate change ratio, R.
2. The order of the filter, N.
3. The number of unit delays per stage, M.

It can be shown that the system function, H(z), of a CIC filter is given by:

$$H(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}} \right)^N = \left(\sum_{k=0}^{RM-1} z^{-k} \right)^N$$

The form on the far right has the advantage of providing a result for z = 1 (corresponding to zero frequency or dc). The alternate form yields an indeterminate form (0/0) for z = 1, but is otherwise identical. The only variable parameter for the AD9856's CIC filter is R. M and N are fixed at 1 and 4, respectively. Thus, the CIC system function for the AD9856 simplifies to:

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^4 = \left(\sum_{k=0}^{R-1} z^{-k} \right)^4$$

The transfer function is given by:

$$H(f) = \left(\frac{1 - e^{-j(2\pi fR)}}{1 - e^{-j(2\pi f)}} \right)^4 = \left(\sum_{k=0}^{R-1} e^{-j(2\pi fk)} \right)^4$$

The frequency response in this form is such that f is scaled to the output sample rate of the CIC filter. That is, f = 1 corresponds to the frequency of the output sample rate of the CIC filter. H(f/R) will yield the frequency response with respect to the input sample of the CIC filter. Figure 31 reveals the CIC frequency response and passband detail for R = 2 and R = 63 and with HBF 3 bypassed. Figure 32 is similar but with HBF 3 selected. Note the flatter passband response when HBF 3 is employed.

As with the case of the HBFs, consideration must be given to the frequency dependent attenuation that the CIC filter introduces over the frequency range of the data to be transmitted. Note that the CIC frequency response plots have f_{NYQ} as their reference frequency; i.e., unity (1) on the frequency scale corresponds to f_{NYQ}. If the incoming data that is applied to the AD9856 is oversampled by a factor of 2 (as required), then the Nyquist bandwidth of the applied data is one-half f_{NYQ} on the CIC frequency response plots. A look at the 0.5 point on the passband detail plots reveals a worst case attenuation of about 0.25 dB (HBF 3 bypassed, R = 63). This, of course, assumes pulse shaped data with $\alpha = 0$ (minimum bandwidth scenario). When a value of $\alpha = 1$ is used, the bandwidth of the data corresponds to f_{NYQ} (the point, 1.0 on the CIC frequency scale). Thus, the worst case attenuation for $\alpha = 1$ is about 0.9 dB.
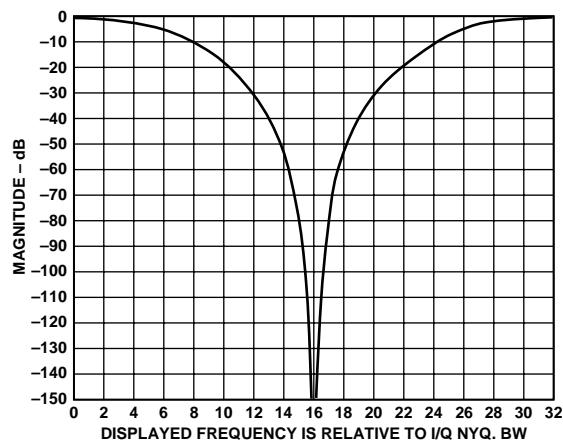
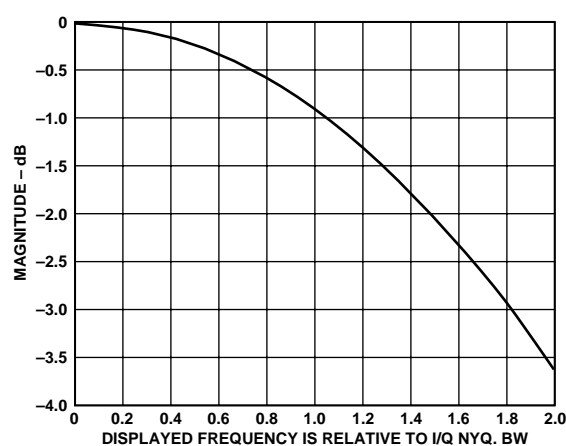a. CIC Frequency Response (R = 2, HBF 3 Bypass)
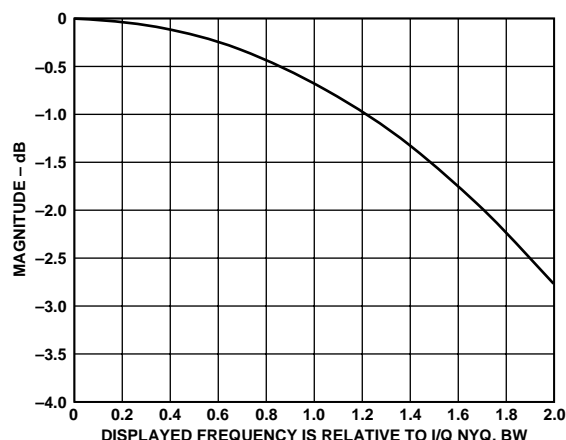
c. Passband Detail (R = 2, HBF 3 Bypass)
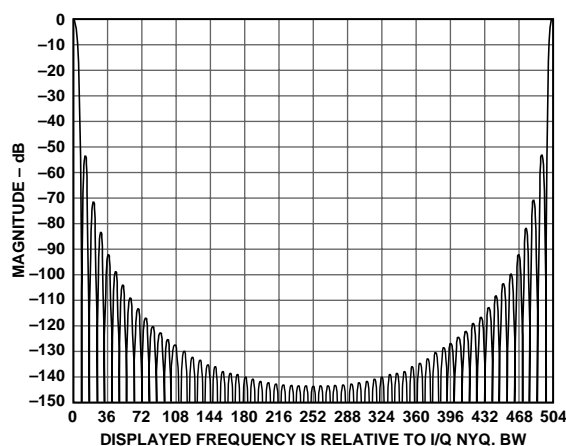
b. CIC Frequency Response (R = 63, HBF 3 Bypass)

d. Passband Detail (R = 63, HBF 3 Bypass)

Figure 31. CIC Filter Frequency Response (HB 3 Bypassed and R = 2, 63)

The degree of the impact of the attenuation introduced by the CIC filter over the Nyquist bandwidth of the data is application specific. The user must decide how much attenuation is acceptable. If less attenuation is desired, then additional oversampling of the baseband data must be employed. Alternatively, the user can precompensate the baseband data before presenting it to the AD9856. That is, if the data is precompensated through a filter that has a frequency response characteristic, which is the inverse of the CIC filter response, then the overall system response can be nearly perfectly flattened over the bandwidth of the data.

Another issue to consider with the CIC filters is insertion loss. Unfortunately, CIC insertion loss is not fixed but is a function of R, M and N. Since M and N are fixed for the AD9856, the CIC insertion loss is a function of R, only.

Interpolation rates that are an integer power-of-2 result in no insertion loss. However, all noninteger power-of-2 interpolation rates result in a specific amount of insertion loss.

To help overcome the insertion loss problem, the AD9856 provides the user a means to boost the gain through the CIC

stage by a factor of 2 (via the CIC Gain bit—see the AD9856 control register description). The reason for this feature is to allow the user to take advantage of the full dynamic range of the DAC, thus maximizing the signal-to-noise ratio (SNR) at the output of the DAC stage. Obviously, it is desirable to operate the DAC over its full-scale range in order to minimize the inherent quantization effects associated with a DAC. Any significant loss through the CIC stage will be reflected at the DAC output as a reduction in SNR. The degradation in SNR can be overcome by boosting the CIC output level. Table II (The CIC Interpolation Filter Insertion Loss Table) tabulates insertion loss as a function of R. The values are provided in linear and decibel form, both with and without the factor-of-two gain employed.

A word of caution: When the CIC Gain bit is active, the user must ensure that the data supplied to the AD9856 is scaled down to yield an overall gain of unity (1) through the CIC filter stage. Gains in excess of unity are likely to cause overflow errors in the data path, thereby compromising the validity of the analog output signal.

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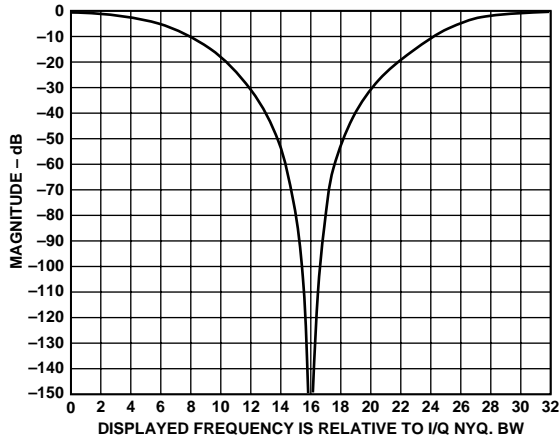
a. CIC Frequency Response (R = 2, HBF 3 Selected)
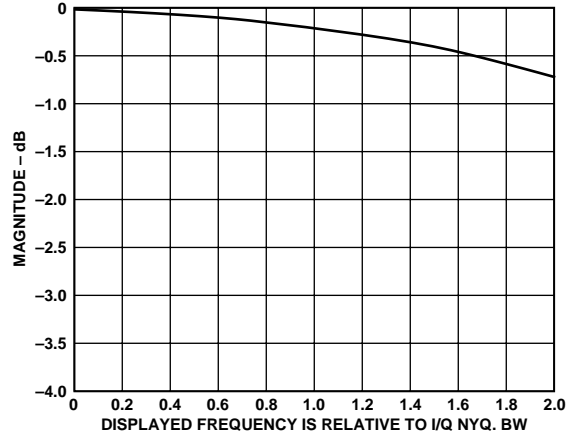
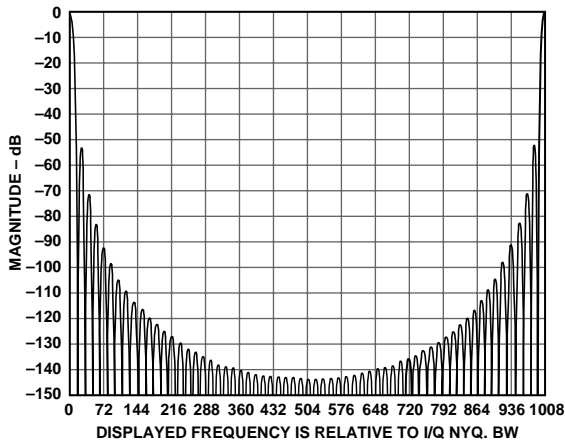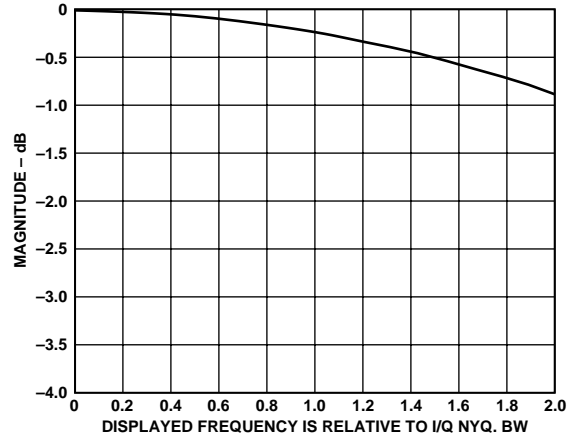

c. Passband Detail (R = 2, HBF 3 Selected)

b. CIC Frequency Response (R = 63, HBF 3 Active)

d. Passband Detail (R = 63, HBF 3 Active)

Figure 32. CIC Filter Frequency Response (HB 3 Selected and R = 2, 63)

DIGITAL QUADRATURE MODULATOR
Following the CIC filter stage the I and Q data (which have been processed independently up to this point) are mixed in the modulator stage to produce a digital modulated carrier. The carrier frequency is selected by programming the direct digital synthesizer (see the DDS section) with the appropriate 32-bit tuning word via the AD9856 control registers. The DDS simultaneously generates a digital (sampled) sine and cosine wave at the programmed carrier frequency. The digital sine and cosine data is multiplied by the Q and I data, respectively, to create the quadrature components of the original data upconverted to the carrier frequency. The quadrature components are digitally summed and passed on to the subsequent stages.

The key point is that the modulation is done digitally, which eliminates the phase and gain imbalance and crosstalk issues typically associated with analog modulators. Note that the modulated "signal" is actually a number stream sampled at the rate of SYSCLK, which is the same rate at which the DAC is clocked (see Figure 21, the AD9856 block diagram).

It should be pointed out that the architecture of the quadrature modulator results in a 3 dB loss of signal level. To visualize this, assume that both the I data and Q data are fixed at the maximum possible digital value, x. Then the output of the modulator, y, is:

$$y = x \times \cos(\omega) + x \times \sin(\omega) = x \times [\cos(\omega) + \sin(\omega)]$$

From this equation it can be shown that y assumes a maximum value of $x\sqrt{2}$ (a gain of 3 dB). However, if the same number of bits were used to represent the y values, as is used to represent the x values, an overflow would occur. To prevent this possibility, an effective "divide-by-two" is implemented on the y values, which reduces the maximum value of y by a factor of two. Since division by two results in a 6 dB loss, the modulator yields an overall loss of 3 dB (3 dB – 6 dB = –3 dB, or 3 dB of loss).

REV. A

Table II. CIC Interpolation Filter Insertion Loss Table

Interpolation Rate	Default Gain		2× Gain	
	(Linear)	(dB)	(Linear)	(dB)
2	1.0000	0.000	2.0000	6.021
3	0.8438	−1.476	1.6875	4.545
4	1.0000	0.000	2.0000	6.021
5	0.9766	−0.206	1.9531	5.815
6	0.8438	−1.476	1.6875	4.545
7	0.6699	−3.480	1.3398	2.541
8	1.0000	0.000	2.0000	6.021
9	0.7119	−2.951	1.4238	3.069
10	0.9766	−0.206	1.9531	5.815
11	0.6499	−3.743	1.2998	2.278
12	0.8438	−1.476	1.6875	4.545
13	0.5364	−5.411	1.0728	0.610
14	0.6699	−3.480	1.3398	2.541
15	0.8240	−1.682	1.6479	4.339
16	1.0000	0.000	2.0000	6.021
17	0.5997	−4.441	1.1995	1.580
18	0.7119	−2.951	1.4238	3.069
19	0.8373	−1.543	1.6746	4.478
20	0.9766	−0.206	1.9531	5.815
21	0.5652	−4.955	1.1305	1.065
22	0.6499	−3.743	1.2998	2.278
23	0.7426	−2.585	1.4852	3.436
24	0.8438	−1.476	1.6875	4.545
25	0.9537	−0.412	1.9073	5.609
26	0.5364	−5.411	1.0728	0.610
27	0.6007	−4.427	1.2014	1.593
28	0.6699	−3.480	1.3398	2.541
29	0.7443	−2.565	1.4886	3.455
30	0.8240	−1.682	1.6479	4.339
31	0.9091	−0.827	1.8183	5.193
32	1.0000	0.000	2.0000	6.021
33	0.5484	−5.219	1.0967	0.802
34	0.5997	−4.441	1.1995	1.580
35	0.6542	−3.686	1.3084	2.335
36	0.7119	−2.951	1.4238	3.069
37	0.7729	−2.237	1.5458	3.783
38	0.8373	−1.543	1.6746	4.478
39	0.9051	−0.866	1.8103	5.155
40	0.9766	−0.206	1.9531	5.815
41	0.5258	−5.583	1.0517	0.437
42	0.5652	−4.955	1.1305	1.065
43	0.6066	−4.342	1.2132	1.679
44	0.6499	−3.743	1.2998	2.278
45	0.6952	−3.157	1.3905	2.863
46	0.7426	−2.585	1.4852	3.436
47	0.7921	−2.024	1.5842	3.996
48	0.8438	−1.476	1.6875	4.545
49	0.8976	−0.938	1.7952	5.082
50	0.9537	−0.412	1.9073	5.609
51	0.5060	−5.917	1.0120	0.104
52	0.5364	−5.411	1.0728	0.610
53	0.5679	−4.914	1.1358	1.106
54	0.6007	−4.427	1.2014	1.593
55	0.6347	−3.949	1.2693	2.072
56	0.6699	−3.480	1.3398	2.541
57	0.7065	−3.018	1.4129	3.002
58	0.7443	−2.565	1.4886	3.455
59	0.7835	−2.120	1.5669	3.901
60	0.8240	−1.682	1.6479	4.339
61	0.8659	−1.251	1.7317	4.770
62	0.9091	−0.827	1.8183	5.193
63	0.9539	−0.410	1.9077	5.610

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INVERSE SINC FILTER (ISF)

The AD9856 is almost entirely a digital device. The input "signal" is made up of a time series of digital data words. These data words propagate through the device as numbers. Ultimately, this number stream must be converted to an analog signal. To this end, the AD9856 incorporates an integrated DAC. The output waveform of the DAC is the familiar "staircase" pattern typical of a signal that is sampled and quantized. The staircase pattern is a result of the finite time that the DAC holds a quantized level until the next sampling instant. This is known as a zero-order hold function. The spectrum of the zero-order hold function is the familiar SIN(X)/X, or SINC, envelope.

The series of digital data words presented at the input of the DAC represent an impulse stream. It is the spectrum of this impulse stream, which is the desired output signal. Due to the zero-order hold effect of the DAC, however, the output spectrum is the product of the zero-order hold spectrum (the SINC envelope) and the Fourier transform of the impulse stream. Thus, there is an intrinsic distortion in the output spectrum, which follows the SINC response.

The SINC response is deterministic and totally predictable. Thus, it is possible to pre-distort the input data stream in a manner, which compensates for the SINC envelope distortion. This can be accomplished by means of an ISF. The ISF incorporated on the AD9856 is a 17-tap, linear phase FIR filter. Its frequency response characteristic is the inverse of the SINC envelope. Data sent through the ISF is altered in such a way as to correct for the SINC envelope distortion.

It should be noted, however, that the ISF is sampled at the same rate as the DAC. Thus, the effective range of the SINC envelope compensation only extends to the Nyquist frequency (1/2 of the DAC sample rate).

Figure 33 is a plot that shows the effectiveness of the ISF in correcting for the SINC distortion. The plot includes a graph of the SINC envelope, the ISF response and the SYSTEM response (which is the product of the SINC and ISF responses). It should be mentioned at this point that the ISF exhibits an insertion loss of 3.1 dB. Thus, signal levels at the output of the AD9856 with the ISF bypassed are 3.1 dB higher than with the ISF engaged. However, for modulated output signals, which have a relatively wide bandwidth, the benefits of the SINC
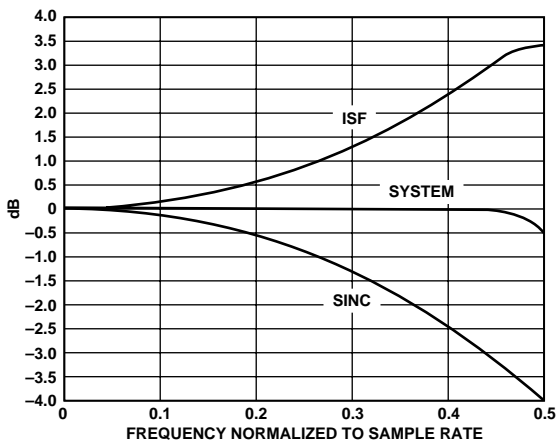

Figure 33. Inverse SINC Filter Response

compensation usually outweigh the 3 dB loss in output level. The decision of whether or not to use the ISF is an application specific system design issue.

DIRECT DIGITAL SYNTHESIZER FUNCTION

The direct digital synthesizer (DDS) block generates the sine/cosine carrier reference signals that are digitally modulated by the I/Q data paths. The DDS function is frequency tuned via the serial control port with a 32-bit tuning word. This allows the AD9856's output carrier frequency to be very precisely tuned while still providing output frequency agility.

The equation relating output frequency of the AD9856 digital modulator to the frequency tuning word (FTWORD) and the reference clock (REFCLK) is given as:

$$A_{OUT} = (FTWORD \times REFCLK)/2^{32}$$

Where: A_{OUT} and $REFCLK$ frequencies are in Hz and $FTWORD$ is a decimal number from 0 to 4,294,967,296 (2^{31})

Example: Find the FTWORD for A_{OUT} = 41 MHz and REFCLK = 122.88 MHz

If A_{OUT} = 41 MHz and REFCLK = 122.88 MHz, then:

$$FTWORD = 556AAAAB \ hex$$

Loading 556*AAAAB*h into control bus registers 02h–05h (for Profile 1) programs the AD9856 for A_{OUT} = 41 MHz, given a REFCLK frequency of 122.88 MHz.

D/A CONVERTER

A 12-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (please see the AD9851 Complete-DDS data sheet for a detailed explanation of aliased images). The wideband 12-bit DAC in the AD9856 maintains spurious-free dynamic range (SFDR) performance of –60 dBc up to A_{OUT} = 42 MHz and –55 dBc up to A_{OUT} = 65 MHz.

The conversion process will produce aliased components of the fundamental signal at n × SYSCLK ± F$_{CARRIER}$ (n = 1, 2, 3). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid modulation impairments. A relatively inexpensive 7th order elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

The AD9856 provides true and complement current outputs on pins 30 and 29 respectively. The full-scale output current is set by the R$_{SET}$ resistor at Pin 25. The value of R$_{SET}$ for a particular I$_{OUT}$ is determined using the following equation:

$$R_{SET} = 39.936/I_{OUT}$$

For example, if a full-scale output current of 20 mA is desired, then R$_{SET}$ = (39.936/0.02), or approximately 2 kΩ. Every doubling of the R$_{SET}$ value will halve the output current. Maximum output current is specified as 20 mA.

The full-scale output current range of the AD9856 is 5 mA–20 mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching, that is, the two outputs should be terminated equally for best SFDR performance.

The output load should be located as close as possible to the AD9856 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads (such as an LC filter). Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance, that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9856 will see for signals within the filter passband. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9856.

The output compliance voltage of the AD9856 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V, otherwise, signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The use of a transformer with a grounded center-tap for common-mode rejection results in signals at the AD9856 DAC output pins that are symmetrical about ground.

As previously mentioned, by differentially combining the two signals the user can provide some degree of common mode signal rejection. A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or "clock feedthrough" that is equally present on both input signals. The AD9856 true and complement outputs can be differentially combined using a broadband 1:1 transformer with a grounded, center-tapped primary to perform differential combining of the two DAC outputs.

REFERENCE CLOCK MULTIPLIER

Due to the fact that the AD9856 is a DDS-based modulator, a relatively high frequency system clock is required. For DDS applications, the carrier is typically limited to about 40% of SYSCLK. For a 65 MHz carrier, the system clock required is above 160 MHz. To avoid the cost associated with these high frequency references, and the noise coupling issues associated with operating a high frequency clock on a PC board, the AD9856 provides an on-chip programmable clock multiplier (REFCLK Multiplier). The available clock multiplier range is from 4× to 20×, in integer steps. With the REFCLK Multiplier enabled, the input reference clock required for the AD9856 can be kept in the 10 MHz to 50 MHz range for 200 MHz system operation, which results in cost and system implementation savings. The REFCLK Multiplier function maintains clock integrity as evidenced by the AD9856's system phase noise characteristics of –105 dBc/Hz (A_{OUT} = 40 MHz, REFCLK Multiplier = 6, Offset = 1 kHz) and virtually no clock-related spurii in the output spectrum. External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 μF) provide the compensation zero for the REFCLK Multiplier PLL loop. The overall loop performance has been optimized for these component values.

THROUGHPUT AND LATENCY

Data latency through the AD9856 is easiest to describe in terms of SYSCLK clock cycles. Latency is a function of the AD9856 configuration; primarily affected by the CIC interpolation rate and whether the third half-band filter is engaged.

When the third half-band filter is engaged the AD9856 latency is given by:

$$126 \, N + 37 \; SYSCLK \, clock \, cycles$$

where N is the CIC interpolation rate.

If the AD9856 is configured to bypass the third half-band filter, the latency is given by:

$$63 \, N + 37 \; SYSCLK \, clock \, cycles.$$

These equations should be considered estimates as observed latency may be data dependent. The latency was calculated using the linear delay model for the FIR filters.

In single tone mode, frequency hopping is accomplished via changing the PROFILE input pins. The time required to switch from one frequency to another is less than 50 SYSCLK cycles with the Inverse SINC Filter engaged. With the Inverse SINC Filter bypassed, the latency drops to less than 35 SYSCLK cycles.

CONTROL INTERFACE

The AD9856 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9856. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9856's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9856. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9856, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9856 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer (1–4), and the starting register address for the first byte of the data transfer.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9856. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9856 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one communication cycle in a multibyte transfer is the preferred method. However, single byte communication cycles are useful to reduce CPU overhead when register access requires one byte only. Examples of this may be to write the AD9856 SLEEP bit, or an AD8320/AD8321 gain control byte.

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At the completion of any communication cycle, the AD9856 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9856 is registered on the rising edge of SCLK. All data is driven out of the AD9856 on the falling edge of SCLK.

Figures 34–37 are useful in understanding the general operation of the AD9856 Serial Port.

INSTRUCTION BYTE

The instruction byte contains the following information as shown below (see Table III):

Table III. Instruction Byte Information

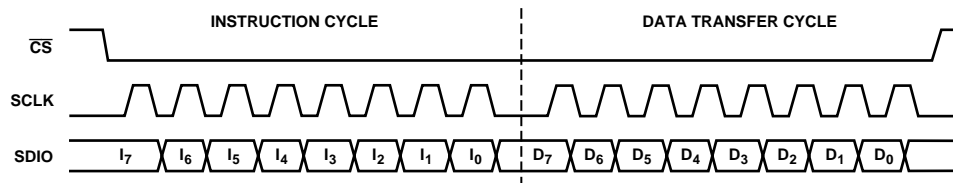| MSB	D6	D5	D4	D3	D2	D1	LSB
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

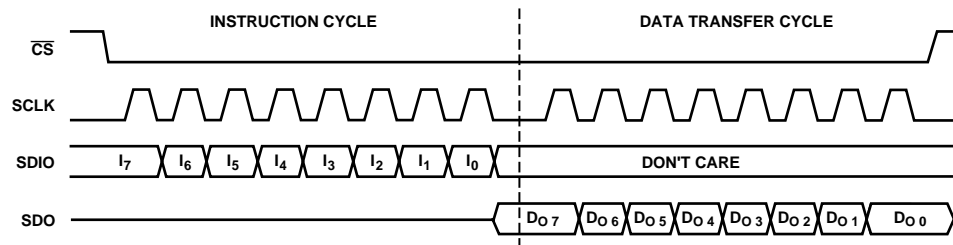Figure 34. Serial Port Writing Timing—Clock Stall Low

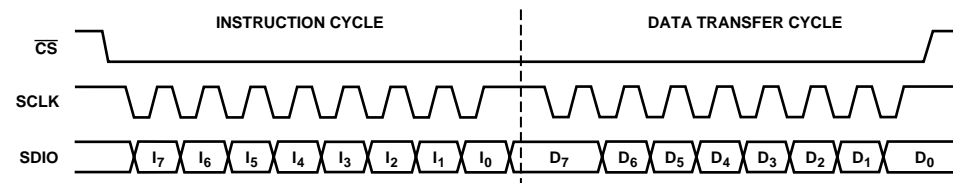Figure 35. Three-Wire Serial Port Read Timing—Clock Stall Low

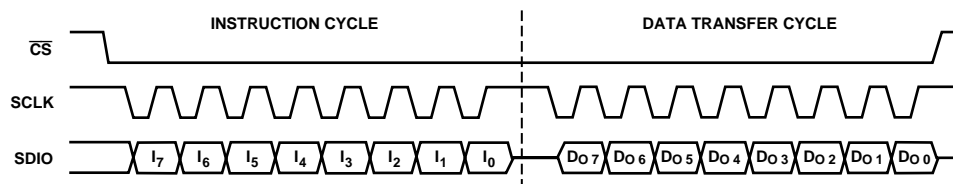Figure 36. Serial Port Write Timing—Clock Stall High

Figure 37. Two-Wire Serial Port Read Timing—Clock Stall High

R/$\overline{W}$–Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

N1, N0—Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle of the communications cycle. The bit decodes are shown in Table IV.

Table IV. N1, N2 Decode Bits

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9856.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9856 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

$\overline{CS}$—Chip Select. Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO—Serial Data I/O. Data is always written into the AD9856 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 0h. The default is logic zero, which configures the SDIO pin as bidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9856 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

SYNC I/O—Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the SYNC I/O pin causes the current communication cycle to abort. After SYNC I/O returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

CA CLK—Output clock pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the CLK input of the AD8320/AD8321.

CA DATA—Output data pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the SDATA input of the AD8320/AD8321.

CA ENABLE—Output Enable pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the DATAEN input of the AD8320/AD8321.

MSB/LSB TRANSFERS

The AD9856 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the REG0<6> bit. The default value of REG0<6> is low (MSB first). When REG0<6> is set active high, the AD9856 serial port is in LSB first format. The instruction byte must be written in the format indicated by REG0<6>. That is, if the AD9856 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

NOTES ON SERIAL PORT OPERATION

The AD9856 serial port configuration bits reside in Bits 6 and 7 of register address 0h. It is important to note that the configuration changes *immediately* upon writing to this register. For multibyte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

The AD9856 serial port controller address can roll from 19h to 0h for multibyte I/O operations if the MSB first mode is active. The serial port controller address can roll from 0h to 19h for multibyte I/O operations if the LSB first mode is active.

The system must maintain synchronization with the AD9856 or the internal control logic will not be able to recognize further instructions. For example, if the system sends an instruction byte for a 2-byte write, then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9856, but the next eight rising SCLK edges are interpreted as the next instruction byte, *not* the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9856, the SYNC I/O pin provides a means to re-establish synchronization without re-initializing the entire chip. The SYNC I/O pin enables the user to reset the AD9856 state machine to accept the next eight SCLK rising edges to be coincident with the instruction phase of a new communication cycle. By applying and removing a "high" signal to the SYNC I/O pin, the AD9856 is set to once again begin performing the communication cycle in synchronization with the system. Any information that had been written to the AD9856 registers during a valid communication cycle prior to loss of synchronization will remain intact.
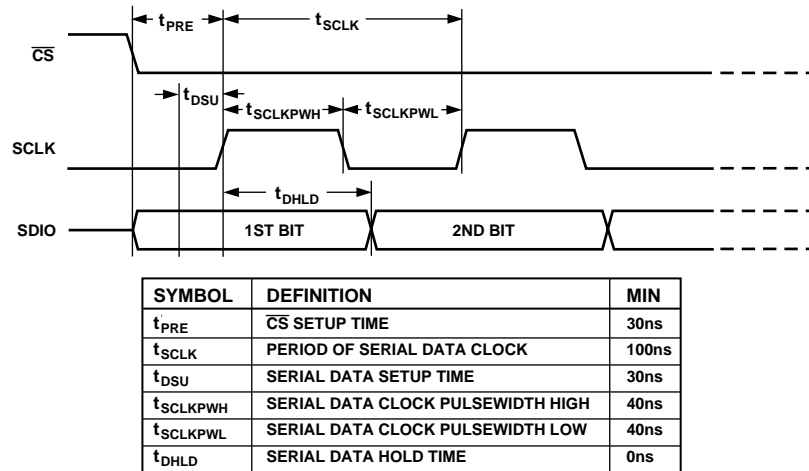
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SYMBOL	DEFINITION	MIN
t_{PRE}	$\overline{CS}$ SETUP TIME	30ns
t_{SCLK}	PERIOD OF SERIAL DATA CLOCK	100ns
t_{DSU}	SERIAL DATA SETUP TIME	30ns
$t_{SCLKPWH}$	SERIAL DATA CLOCK PULSEWIDTH HIGH	40ns
$t_{SCLKPWL}$	SERIAL DATA CLOCK PULSEWIDTH LOW	40ns
t_{DHLD}	SERIAL DATA HOLD TIME	0ns

Figure 38. Timing Diagram for Data Write to AD9856

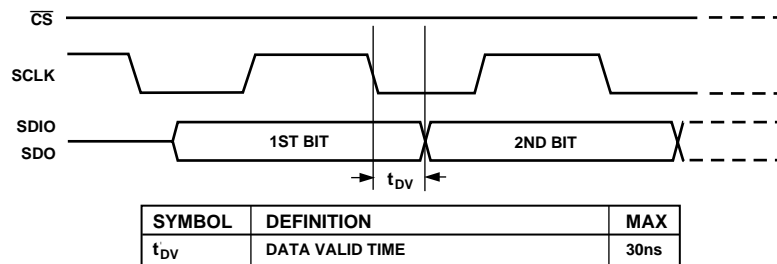| SYMBOL	DEFINITION	MAX
t_{DV}	DATA VALID TIME	30ns

Figure 39. Timing Diagram for Read from AD9856

PROGRAMMING/WRITING THE AD8320/AD8321 CABLE DRIVER AMPLIFIER GAIN CONTROL

Programming the Gain Control register of the AD8320/AD8321 programmable cable driver amplifier can be accomplished via the AD9856 serial port. Four 8-bit registers (one per profile) within the AD9856 store the gain value to be written to the AD8320/AD8321. The AD8320/AD8321 is written via three dedicated AD9856 output pins that are directly connected to the AD8320/AD8321's serial input port. The transfer of data from the AD9856 to the AD8320/AD8321 requires 136 SYSCLK clock cycles and occurs upon detection of three conditions. Each is described below:

1. Power-up Reset—Upon initial power up, the AD9856 clears (Logic 0) the contents of control registers 07h, 0Dh, 13h, and 19h, which defines the lowest gain setting of the AD8320/AD8321. Thus, the AD9856 writes all 0s out of the AD8320/AD8321 serial interface.

2. Change in profile selection bits (PS1, PS0)—The AD9856 samples the PS1, PS0 input pins and writes to the AD8320/AD8321 gain control register when a change in profile is determined. The data written to the AD8320/AD8321 comes from the AD9856 gain control register associated with the current profile.

3. Serial Port Write of AD9856 Registers that Contain AD8320/AD8321 Data—The AD9856 will write to the AD8320/AD8321 with data from the gain control register associated with the current profile whenever ANY AD9856 gain control register is updated. The user does not have to write the AD9856 in any particular order or be concerned with time between writes. If the AD9856 is currently writing to the AD8320/AD8321 while one of the four AD9856 gain control registers is being addressed, the AD9856 will immediately terminate the AD8320/AD8321 write sequence (without updating the AD8320/AD8321) and begin a new AD8320/AD8321 write sequence.
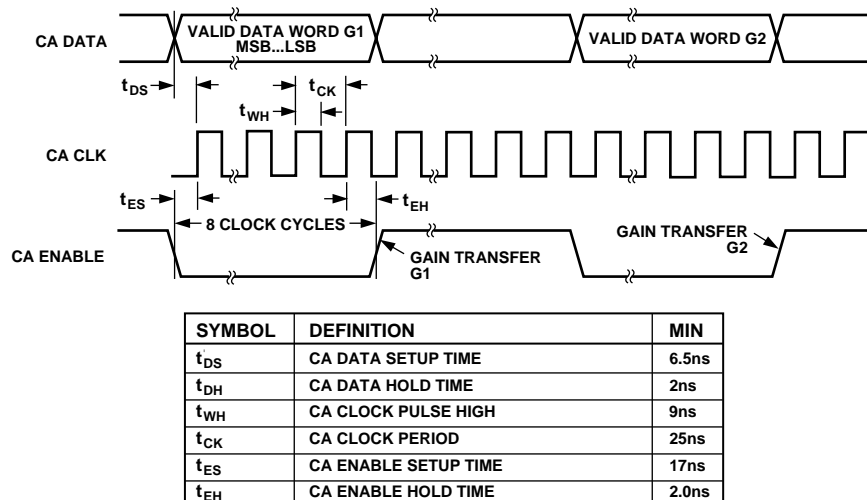
SYMBOL	DEFINITION	MIN
t_{DS}	CA DATA SETUP TIME	6.5ns
t_{DH}	CA DATA HOLD TIME	2ns
t_{WH}	CA CLOCK PULSE HIGH	9ns
t_{CK}	CA CLOCK PERIOD	25ns
t_{ES}	CA ENABLE SETUP TIME	17ns
t_{EH}	CA ENABLE HOLD TIME	2.0ns

Figure 40. Programmable Cable Driver Amplifier Output Control Interface Timing

UNDERSTANDING AND USING PIN SELECTABLE MODULATOR PROFILES

The AD9856 Quadrature Digital Upconverter is capable of storing four preconfigured modulation modes called "profiles" that define the following:

- Output Frequency—2 Bits
- Interpolation Rate—6 Bits
- Spectral Inversion Status—1 Bit
- Bypass 3rd Half-Band Filter—1 Bit
- Gain Control of AD8320/AD8321—8 Bits

Output Frequency: This attribute consists of four 8-bit words loaded into four register addresses to form a 32-bit frequency tuning word (FTW) for each profile. The lowest register address corresponds to the least significant 8-bit word. Ascending addresses correspond to increasingly significant 8-bit words. The output frequency equation is given as: $f_{OUT} = (FTW \times SYSCLK)/2^{32}$.

Interpolation Rate: Consists of a 6-bit word representing the allowed interpolation values from 2 to 63. Interpolation is the mechanism used to "up-sample" or multiply the input data rate such that it exactly matches that of the DDS sample rate (SYSCLK). This implies that the system clock must be an exact multiple of the symbol rate. This 6-bit word represents the 6 MSBs of the eight bits allocated for that address. The remaining two bits contain the spectral inversion status bit and half-band bypass bit.

Spectral Inversion: Single bit that when at Logic 0 the default or "noninverted" output from the adder is sent to the following stages. A Logic 1 will cause the inverted output to be sent to the following stages. The noninverted output is described as I × Cos(ωt) – Q × Sin(ωt). The inverted output is described as I × Cos(ωt) + Q × Sin(ωt). This bit is located adjacent to the LSB at the same address as the interpolation rate (see above).

Bypass Third Half-Band Filter: A single bit located in the LSB position of the same address as the interpolation rate. When this bit is Logic 0, the third half-band filter is engaged

and its inherent 2× interpolation rate is applied. When this bit is Logic 1, the third half-band filter is bypassed and the 2× interpolation rate is negated. This allows users to input higher data rates—rates that may be too high for the minimum interpolation rate if all three half-band filters with their inherent 2× interpolation rate are engaged. The overall effect is to reduce minimum interpolation rate from 8× to 4×.

AD8320/AD8321 Gain Control: An 8-bit word that controls the gain of an AD8320/AD8321 Programmable Gain Amplifier connected to the AD9856 with the 3-bit SPI interface bus. Gain range is from –10 dB (00 hex) to +26 dB (FFhex). The gain is linear in V/V/LSB and follows the equation: $A_V = 0.316 + 0.077 \times Code$. Where "Code" is the decimal equivalent of the 8-bit gain word.

Profile Selection: After profiles have been loaded into the appropriate registers, the user may select which profile to use with two input pins: PS0 and PS1, Pins 45 and 46. Profiles are selected according to the table below.

Table V. Profile Select Matrix

PS1	PS0	PROFILE
0	0	1
0	1	2
1	0	3
1	1	4

Except while in single tone mode, it is recommended that users suspend the T_XENABLE function by bringing that pin to Logic 0 prior to changing from one profile to another and then reasserting T_XENABLE afterwards. This assures that any dis-continuities resulting from register data transfer are not transmitted up or downstream. Furthermore, changing interpolation rates during a burst may create an unrecoverable digital overflow condition that would interrupt transmission of the current burst until a RESET and reloading procedure would be completed.

AD9856

POWER DISSIPATION CONSIDERATIONS

The majority of the AD9856 power dissipation comes from digital switching currents. As such, power dissipation is highly dependent upon chip configuration.

Obviously, the major contributor to switching current is the maximum clock rate at which the device is operated, but other factors can play a significant role. Factors such as the CIC interpolation rate, and whether the third half-band filter and inverse SINC filters are active, can affect the power dissipation of the device.

It is important for the user to consider all of these factors when optimizing performance for power dissipation. For example, there are two ways to achieve a 6 MS/s transmission rate with the AD9856. The first method uses an f_{MAX} of 192 MHz; the other method uses an f_{MAX} of 144 MHz, which reduces power dissipation by nearly 25%.

For the first method, the input data must be externally 4× up-sampled. The AD9856 must be configured for a CIC interpolation rate of three while bypassing the 3rd half-band filter. This results in an I/Q input sample rate of 24 MHz which is further upsampled by a factor of 8 to 192 MHz.

The second method requires an f_{MAX} of 144 MHz with externally 2× upsampled input data. The AD9856 is configured for a CIC interpolation rate of 3 while bypassing the 3rd half-band filter. The input I/Q sample rate is 12 MHz, which is further upsampled by a factor of 12 MHz to 144 MHz.

For burst applications with relatively long nonbursting periods, the sleep bit is useful for saving power. When in sleep mode, power is reduced to below 6 mW. Consideration must be given to wake-up time, which will generally be in the 400 μs to 750 μs range. For those applications that cannot use the sleep bit due to this wake-up time, there is an alternate method of reducing power dissipation when not transmitting. By writing the "Bypass REFCLK Multiplier" bit active, the power is reduced by nearly the REFCLK Multiplier factor. For example, if the external reference clock is 16 MHz and REFCLK Multiplier is set to 10×, all clocks will divide down by a factor of 10 when the REFCLK Multiplier is bypassed. This effectively scales down the power dissipation by nearly a factor of 10. In this case, both the REFCLK Multiplier function and the DAC, which use relatively little power, remain fully powered. The REFCLK Multiplier circuit is locked to the 16 MHz external reference clock but its output is driving a very small load, hence very little power dissipation. When the REFCLK Multiplier is reactivated, the acquisition time is small. In this power-reduction technique, the larger the REFCLK Multiplier factor, the larger the power savings.

The AD9856 is specified for operation at +3.0 V ± 5% and the thermal impedance of the AD9856 in the 48-LQFP plastic package is 38°C/W. At 200 MHz operation, power dissipation is 1.5 W. This permits operation over the industrial temperature range without exceeding the maximum junction temperature of 150°C. To realize this quoted thermal impedance, all power and ground pins must be soldered down to a multilayer PCB with power and ground copper planes directly available at the package pins.

Under worst case conditions, that is, with power supplies at +2.85 V and ambient temperatures of +85°C, device operation at 200 MHz is guaranteed for single tone mode only. For modulation mode at 200 MHz, +85°C operation, the minimum power supply voltage is +3.0 V.

AD9856 EVALUATION BOARD

An evaluation board is available for the AD9856 quadrature digital upconverter that facilitates bench and system analysis of the device. The AD9856/PCB contains the AD9856 device and Windows software that allows control of the device via the printer port of a PC. The DAC output is provided on a jack for spectral analysis.

The AD9856/PCB circuit board has provisions for a single-ended low-pass filter to be implemented by the user on the output of the DAC. The parts list for 45 MHz and 70 MHz low-pass filters can be obtained by consulting the factory.

There is also a provision for the user to implement the AD8320/AD8321 programmable cable driver amplifier on the AD9856/PCB evaluation board. The AD8320/AD8321 gain is programmed through the AD9856 via the menu driven control software.
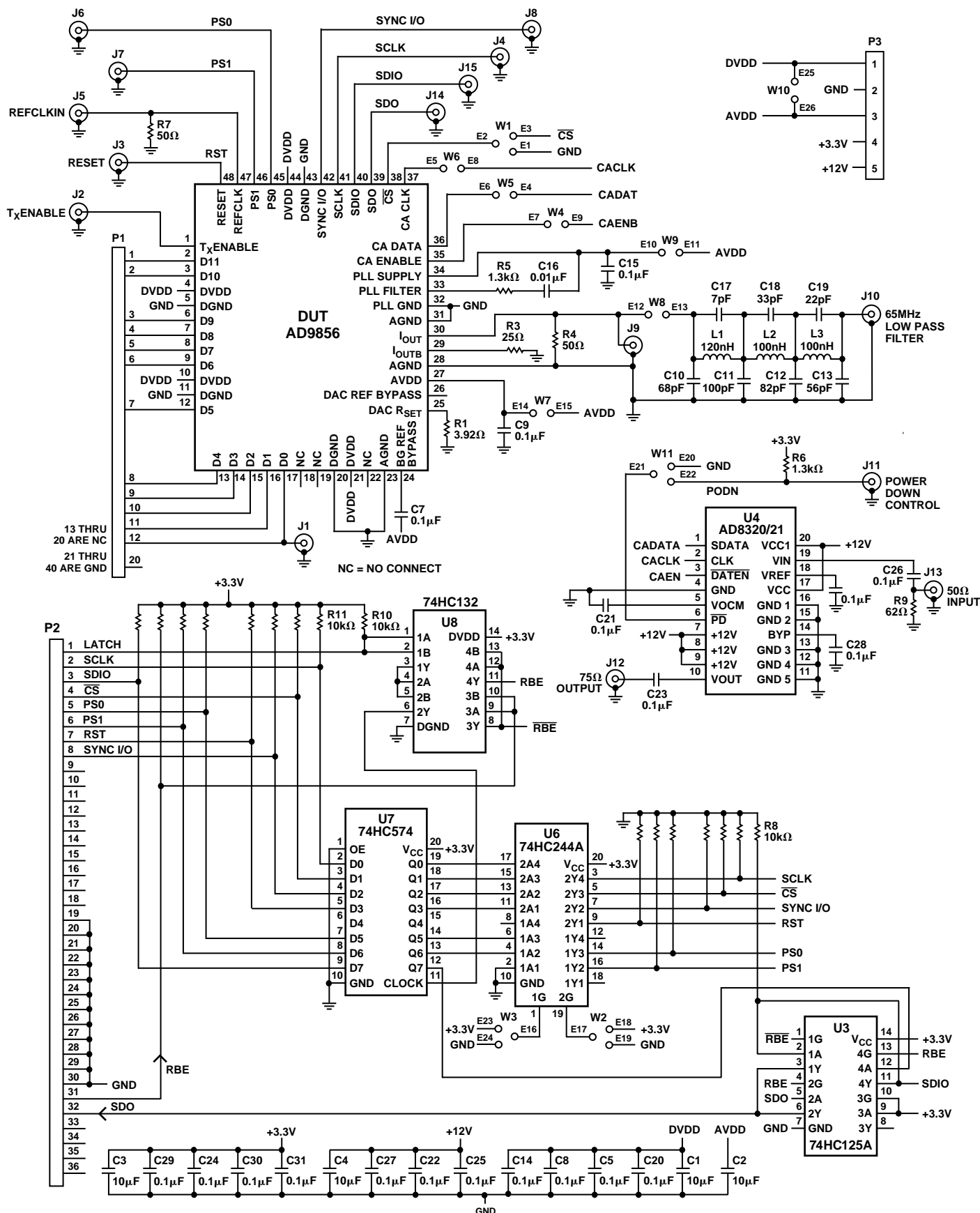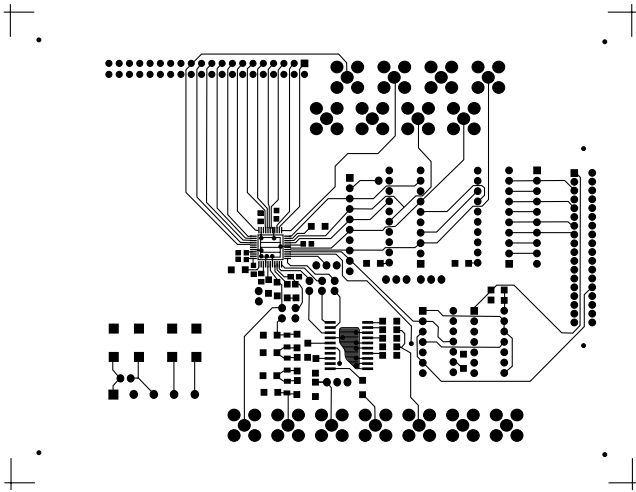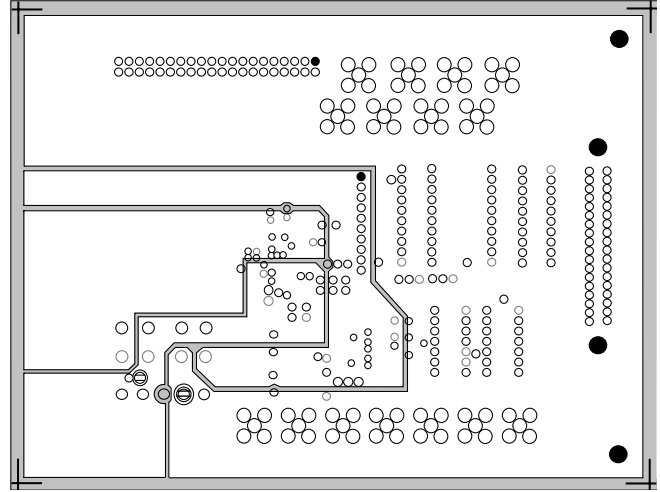
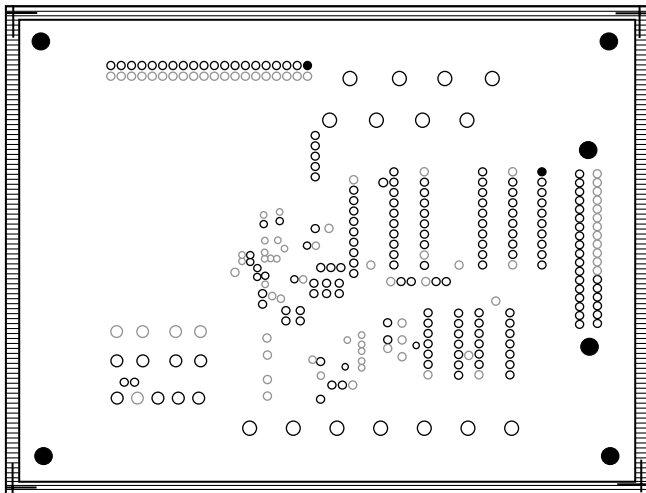*Figure 41. AD9856/PCB Evaluation Board Electrical Schematic*
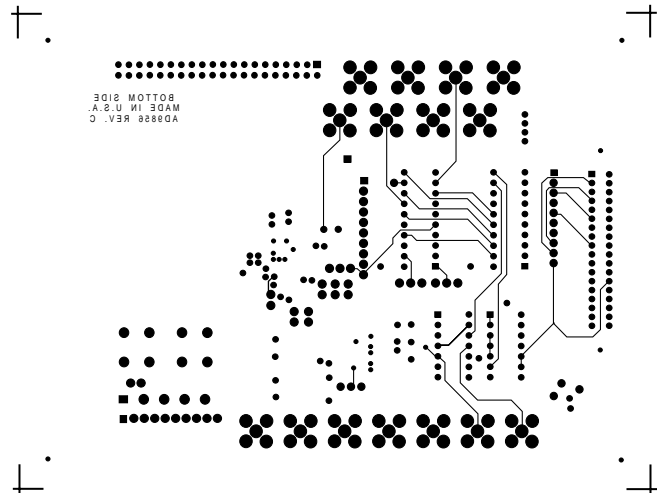
AD9856

a. Layer 1 (Top)—Signal Routing and Ground Plane

c. Layer 3—DUT +V, +5 V and +12 V Power Plane

b. Layer 2—Ground Plane

d. Layer 4 (Bottom)—Signal Routing

Figure 42. PCB Layout Patterns for Four-Layer AD9856-PCB Evaluation Board
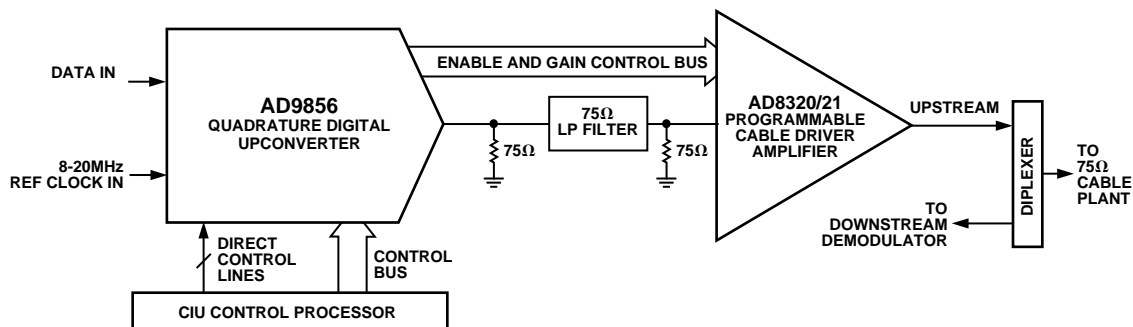
REV. A

Figure 43. Basic Implementation of AD9856 Digital Modulator and AD8320/AD8321 Programmable Cable Driver
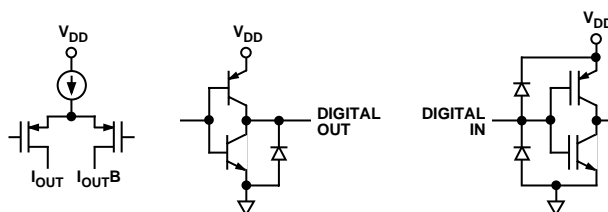Amplifier in 5 MHz–65 MHz HFC Return-Path Application

Figure 44. Equivalent I/O Circuits

AD9856

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

48-Lead Quad Flatpack IC Package (LQFP)
(ST-48)

0.063 (1.60) MAX

0.057 (1.45)
0.053 (1.35)

0.030 (0.75)
0.018 (0.45)

SEATING
PLANE

0.006 (0.15)
0.002 (0.05)

0° MIN

0° – 7°

0.007 (0.18)
0.004 (0.09)

0.354 (9.00) BSC

0.276 (7.0) BSC

48
1

37
36

TOP VIEW
(PINS DOWN)

12
13

25
24

0.276
(7.0)
BSC

0.354
(9.00)
BSC

0.019 (0.5)
BSC

0.011 (0.27)
0.006 (0.17)

REV. A