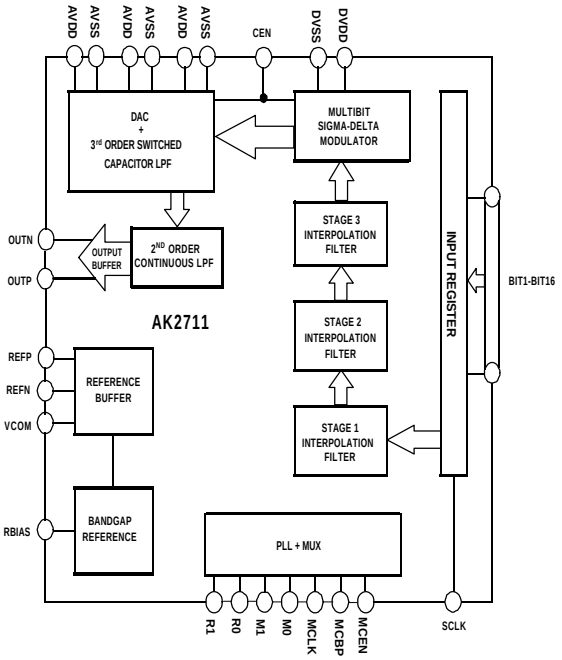
AK2711

High Speed DAC w/16-Bit Resolution at 1.2 MSPS

Features

- Monolithic 16-Bit Oversampled DAC
- 16 x Oversampling, 20 MSPS Clock
- Internal low jitter PLL allows clock input speeds of 2, 4, 8 and 16 x sample clock.
- 1.25 MHz Input Word Rate
- AC Specifications
  - 500 kHz Signal Passband
  - Signal-to-Noise: 86 dB
  - Signal-to-(Noise plus Distortion): 82.5 dB
  - Dynamic range: 86 dB
  - Out-of-band (up to 10 Mhz): 70 dB
- Digital Filter
  - Passband Ripple: 0.05dB
  - Stopband Attentuation: 70dB
- Low Power Dissipation 200 mW
- Power Supply
  - Analog Supply + 5 V
  - Digital Supply + 3 V/ + 5 V
- 4 V Vpp differential glitch free output
- Edge triggered input latch for parallel data input
- 44 pin LQFP package

Block Diagram



Description

The AK2711 is a 16-bit, high speed oversampled digital-to-analog converter optimized for waveform reconstruction applications requiring high dynamic range. Glitches that are characteristic of Nyquist rate DACs are avoided by use of an over-sampled, multi-bit sigma-delta architecture. The AK2711 is manufactured on an advanced submicron analog process. High dynamic range is achieved by the use of proprietary multi bit delta sigma techniques.

The AK2711 is a switched capacitor DAC, with a nominal full scale differential output of 4 V with a common-mode output level of 2.5V.

The on-chip interpolation filter suppresses original inband images eliminating the need for complex external analog smoothing filters. Additional out-of-band filtering is provided after the sigma-delta DAC The on-chip reference and reference buffer amplifier are configured for maximum accuracy and flexibility.

Phase-Lock-Loop clock multiplier provides the necessary synchronized 16fs clock to support the over-sampled DAC. An external synchronous clock can also be used.

The AK2711 operates on a single +5 V analog supply and +5 V/ +3 V digital supply, typically consuming 200mW. The AK2711 is available in a 44-lead LQFP package and is specified to operate from -40 to 85C.

PERFORMANCE SPECIFICATION

DC SPECIFICATION

AVDD = 5.0V, DVDD = 3V, AGND = DGND = 0V, f_{MCLK} = 20 MSPS, T_{MAX}=85C, T_{MIN}=-40C

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Resolution		16			Bits
Accuracy					
Integral Nonlinearity (INL)			±2		LSB
Differential Nonlinearity (DNL)			±0.8		LSB
Monotonicity	Bits Guaranteed[1]	16			Bits
Offset Error	Note 1		0.3	TBD	% FSR
Gain Error	Note 1	TBD	-3.5	TBD	% FSR
Temperature Drift					
Offset Error			1.1		ppm/C
Gain Error			50		ppm/C
Power Supply Rejection					
AVDD,DVDD,SVDD	50 mV supply ripple(500kHz)		0.1		% FSR
Analog Output					
Output Full Scale	V_{REF} = 2.5V		4		V_{p-p} Diff
Output Common Mode Voltage			2.43		V
Output Load Resistance		2			k ohms
Output Load Capacitance				20	pF
Internal Voltage Reference					
Output Voltage		TBD	2.43	TBD	V
Power Supplies					
AVDD & SVDD		4.75	5	5.25	V
DVDD		2.7	3	5.25	V
Supply Currents					
I(AVDD + SVDD)	100kHz Input, -2.2dBFS[1]		35	TBD	mA
I(DVDD)	100kHz Input, -2.2dBFS[1]		9	TBD	mA
Power Consumption					
Power	100kHz Input, -2.2dBFS[1]		202		mW

PERFORMANCE SPECIFICATION[continued]

AC SPECIFICATION

AVDD = +5V, DVDD= +3V, f_{MCLK} = 20 MSPS, T_{MAX}=85C, T_{MIN}=-40C

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
DYNAMIC PERFORMANCE					
Input Test Frequency: 100 KHz					
Signal to Noise (SNR)	Input Amplitude: -0.5dBFS[1]	TDB	86		dB
	Input Amplitude: -6 dBFS		80		dB
SNR + Distortion (SINAD)	Input Amplitude: -0.5 dBFS[1]	TBD	82.5		dB
	Input Amplitude: -6 dBFS		79		dB
Total Harmonic Distortion (THD)	Input Amplitude: -0.5 dBFS[1]		85	TDB	dB
	Input Amplitude: -6 dBFS		88		dB
Spurious Free Dynamic Range (SFDR)	Input Amplitude: -0.5 dBFS[1]	TBD	86		dB
	Input Amplitude: -6 dBFS		89		dB
Input Test Frequency: 500 KHz					
Signal to Noise (SNR)	Input Amplitude: -0.5dBFS		86		dB
	Input Amplitude: -6 dBFS		80		dB
Spurious Free Dynamic Range (SFDR)	Input Amplitude: -0.5 dBFS		86		dB
	Input Amplitude: -6 dBFS		89		dB
INTERMODULATION DISTORTION					
f_{IN1} = 475 kHz, f_{IN2} = 525 kHz			TBD		dBFS
DYNAMIC CHARACTERISTICS					
Settling Time	To 0.003% FS		TBD		us
Output Propagation Delay			TBD		Clocks
Output Noise Voltage			71		uV rms

DIGITAL FILTER CHARACTERISTICS

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
DAC Filter					
Passband Ripple	0 to 0.4 fs			±0.05	dB
Stopband Attenuation	> 0.596 fs	-70			dB

PERFORMANCE SPECIFICATION[continued]

DIGITAL SPECIFICATION

AVDD = +5V, DVDD = +5V, T_{MAX}=85C, T_{MIN}=-40C

Parameter		Conditions/Comments	Min.	Typ	Max	Units
VIH	High Level Input Voltage	Clock Pin	2			V
VIL	Low Level Input Voltage	Clock Pin			0.8	V
VIH	High Level Input Voltage	All other pins	0.7*DVDD			V
VIL	Low Level Input Voltage	All other pins			0.3*DVDD	
$R_{PULLDOWN}$	Pull Down Resistance	MCEN, MCBP, R1, R0, M1, M0, TST, DITHEN, DEMEN, SCAN	10		50	K Ohms
I_{IL}	Input Leakage Current	All pins except internal pull-down pins			±10	uA

Notes

1. 100% production tested at 25C and sample tested at the specified temperatures.

Absolute Maximum Ratings

AGND, SGND,RGND and DGND = 0V. All voltages are with respect to ground.

Parameter		Min.	Max.	Units
Power Supplies				
VA	Analog Power Supply	-0.3	6.0	V
VD	Digital Power Supply	-0.3	VA	V
GND	Difference between AGND, SGND, AGND2 and DGND		0.3	V
IIN	Input Current—All pins except supply pins		±10	mA
VIND	Digital Input Voltage	-0.3	VD + 0.3	V
Temperature				
Ta	Ambient Operating Temperature (Power Applied)	-40	80	°C
Tstg	Storage Temperature	-65	150	°C

Recommended Operation Conditions

AGND, SGND, AGND2, and DGND = 0V. All voltages are with respect to ground.

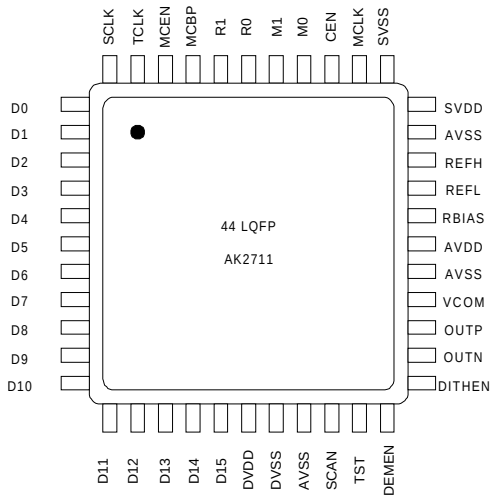
Parameter		Min.	Typ.	Max.	Units
Power Supplies[1]					
VA	Analog Power Supply (AVDD & SVDD)	4.75	5.0	5.25	V
VD	Digital Power Supply (DVDD)	2.7	3.3	VA	V

Digital Switching Characteristics

AVDD = +5V, DVDD=5V, CL=20pF, T_{MAX}=85C, T_{MIN}=-40C

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
tMCLK	Master Clock Period		50			ns
tSCLK	Sample Clock Period		800			ns
tMCLKH	Master Clock Pulse Width High		20			ns
tMCLKL	Master Clock Pulse Width Low		20			ns
tSCLKH	Sample Clock Pulse Width High		396			ns
tSCLKL	Sample Clock Pulse Width Low		396			ns
tS	Input Setup Time to SCLK		5			ns
tH	Input Hold Time after SCLK		5			ns

PIN LAYOUT



PIN DESCIPTION

No.	Pin Name	I/O	Pin Function and Description
1-16	D0-D15	I	**Data Input.** (MSB = Pin 16 LSB = Pin1)
17	DVDD		**3V Digital Supply.** DVDD = 3/5V
18	DVSS		**3V Digital Ground.** DVSS = 0V
19	AVSS		**Analog Ground.** AVSS=0V
20	SCAN	I	**Test Mode Pin**
21	TST	I	**Test Mode Pin**
22	DEMEN	I	**Test Mode Pin**
23	DITHEN	I	**Dither Enable (Active low)**
24	OUTN	O	**Differential Analog Output**
25	OUTP	O	**Differential Analog Output**
26	VCOM	O	**Internal Common mode voltage**
27	AVSS		**Analog Ground.** AVSS=0V
28	AVDD		**Analog Supply.** AVDD = 5V
29	RBIAS	I	**Resistor Connected to Ground (4.99K ohms)**
30	REFL	O	**1V output derived from internal bandgap voltage**
31	REFH	O	**4V output derived from internal bandgap voltage**
32	AVSS		**Analog Ground.** AVSS=0V
33	SVDD		**5 V Analog Supply** SVDD = 5V
34	SVSS		**Analog Ground.** SVSS = 0V
35	MCLK	I	**Master Clock**
36	CEN	I	**Chip Enable** (Active High)
37	M0	I	**PLL Mode Pins. M1,M0** 00 - MCLK = SCLK; 01 - MCLK = 2SCLK, 10- MCLK = 4SCLK; 11 - MCLK = 16SCLK.
38	M1	I	
39	R0	I	**Connected to 0V**
40	R1	I	**Connected to 5V**
41	MCBP	I	**PLL Bypass**
42	MCEN	I	**Enables PLL Clock Output**
43	TCLK	O	**PLL Clock Output**
44	SCLK	I	**Sample Clock** (Data is latched on the positive edge of the clock)

THEORY OF OPERATION

The AK2711 is a 16 bit, 2.5MSPS Digital to Analog converter intended for xDSL and high speed instrumentation, medical imaging and high resolution, high speed signal generation. A novel delta-sigma modulator operating at 20Mhz employing multibit quantization and dynamic element matching techniques achieves 86dB signal to noise performance, with a 86dB of spurious free dynamic range and a low power dissipation of 200mW.

The on-chip interpolation filter and continuos time filter provides excellent stop-band rejection to suppress any stray signal greater than 0.745MHz, substantially easing the requirements of any anti-imaging filter for the analog output path.

The AK2711 features an internal digital PLL to provide flexibility in the clock input. The PLL MODE pin allow for different clocking options. A digital supply of 5.25 to 2.7V can be used, though a 3V supply is recommended to minimize digital noise on the board. The CEN pin is provided to reset the internal filters, in case of an overflow condition and correct initialization during power up.An on-chip reference and reference buffer is included on the AK2711. The 2.5V reference provides for a 4V pk-pk differential output full scale.

Digital Inputs

A parallel data interface uses the sample clock (SCLK) to clock in the input data. The positive edge of SCLK strobes the 2's complement data into the input registers of the AK2711. The SCLK can be asynchronous to the master clock (MCLK).

Digital Interpolation Filter

The purpose of the interpolator is to oversample the input data, i.e. to increase the sample rate so that the attentuation requirements on the analog filters are relaxed. The interpolation is performed using a multistage FIR digital filters.The filtering introduces a $\pm$0.05dB of passband ripple and a stopband attentuation of -70dB.

Multibit Sigma Delta Modulator

The AK2711 employs a multi bit sigma delta using proprietary dynamic element matching techniques to provide excellent linearity.

Dither Generator

The AK2711 includes an on chip dither generator, which is intended to further reduce the quantization noise introduced by the multibit DAC. This dithering can be externally turned off using a test mode pin, DITHEN.

Analog Filtering

The AK2711 includes a 3rd order switched capacitor discrete time low pass filter followed by a 2nd order analog continuos time low pass filter. These filters eliminate the need for any additional off chip external reconstruction filtering. The continuos time filtering results in glitch free output waveforms.

Phase Lock Loop

A digital phase lock loop is integrated on chip to provide flexibility in clocking. The Mode pins allow MCLK to 1x, 2x, 4x and 16x times the SCLK frequency. The Range pins allow for a different ranges of SCLK from 625KHz to 2.5MHz. The best performance is achieved when the PLL is bypassed.

Analog Output and Reference Overview

The value of VCM defines the maximum output voltage to the AK2711. An internal reference buffer scales the VCM of 2.5V to create REFH and REFL. The scale factor for these buffers is 0.8. Thus the maximum output voltage of the D/A is defined to be +0.8 x VCM = +2V to -0.8 x VCM = -2V.

Output Drive, Buffering and Loading

The AK2711 analog output stage is able to drive a load of 1K ohms. If a single ended output is required, a differential to single ended instrument op amp circuit is required. Level scaling can also be achieved easily using this circuit.

DIFFERENTIAL TO SINGLE ENDED DRIVER

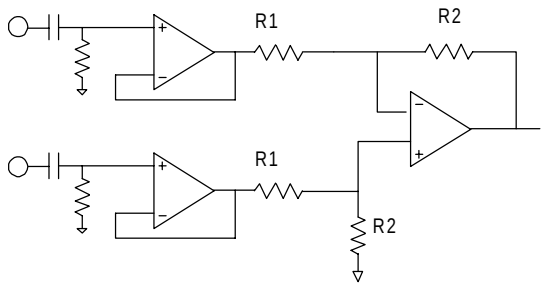


Figure 1: AC Coupled Differential Buffer with Level Shifting

REFERENCE OPERATION

The AK2711 contains an integrated bandgap reference and a internal reference buffer amplifier. This reference generates a 2.5V. The actual voltages used by the internal circuitry of the AK2711 appear on the REFH and REFL pins. For proper operation, it is necessary to add a capacitive network to decoupled the pins. All digital switching lines must be drawn away from these pins.

BIAS PIN

The pin is connected to a 4.99k ohms. This sets up the bias currents to all the analog circuitry. Minimization of capacitance to this pin is recommended in order to prevent instability of the bias pin amplifier.

CLOCK INPUT CONSIDERATION

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AK2711. The CLK input buffer is powered by a 5V analog supply and requires high and low levels of 3.5V and 1V respectively. Low jitter crystal controlled oscillators make the best clock source

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Multi layer printed circuit boards (PCBs) are recommended to provide for optimal grounding and power schemes. The use of ground and power planes results in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While AK2711 features separate analog and digital pins, it should be treated as an analog component.

Analog and Digital Supply Decoupling

The analog and digital supplies should be decoupled as close to the chip as physically possible. A combination of 0.1uF and 10uF should be connected between each pair of power supplies: AVDD and AVSS, DVDD and DVSS, and SVDD and SVSS. An external decoupling and bias network is shown in figure 2.

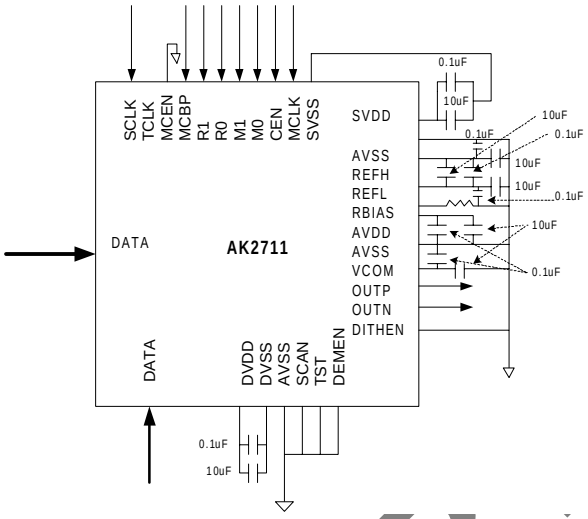
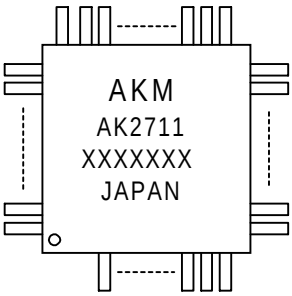


Figure2: Decoupling and Bias Connection for AK2711

MARKING SPEC

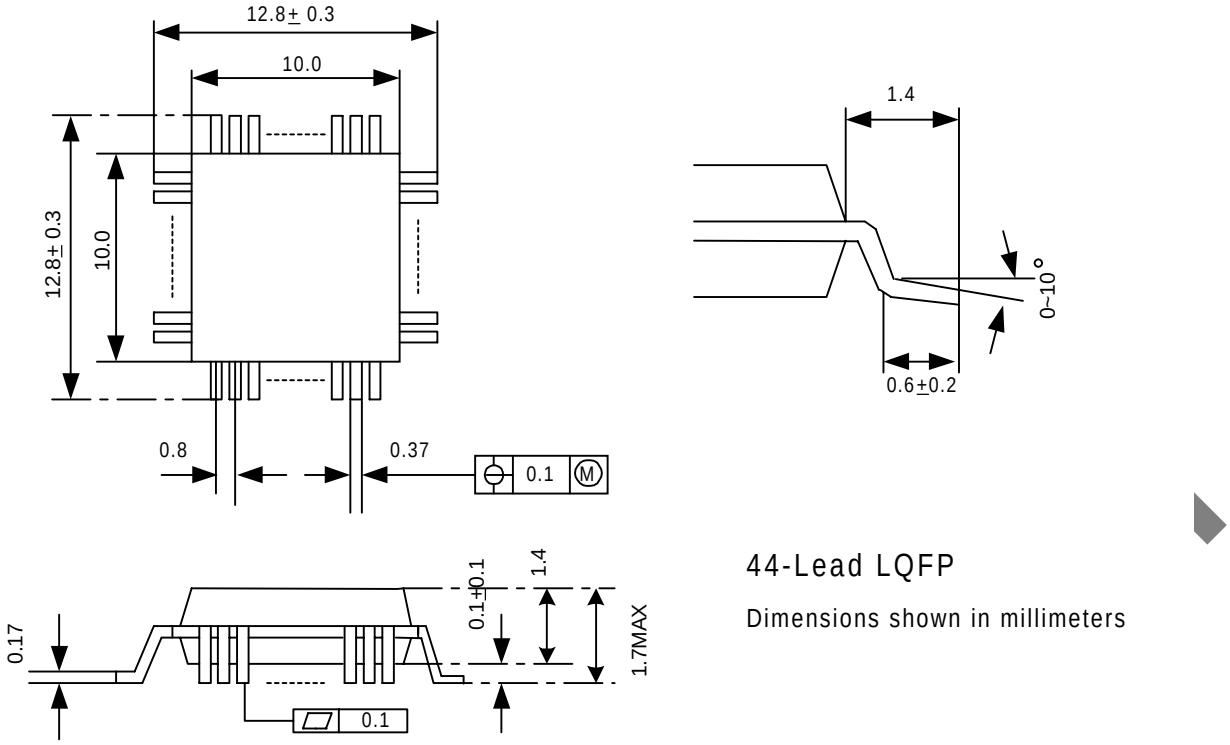
Marking Spec



XXXXXXX Date and Production Code

JAPAN Country Of Origin

OUTLINE DIMENSIONS



44-Lead LQFP

Dimensions shown in millimeters

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