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Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module

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INTRODUCTION

This application note describes how to implement an Analog-to-Digital (A/D) Converter function using a member of the PIC16C6XX series of microcontrollers. Although these microcontrollers do not have a built-in A/D Converter like other controllers from Microchip, the comparator function, internal voltage reference and timers can be used to digitize an analog signal.

Some of the standard PICmicros have a comparator module, consisting of two comparators, both of which can be connected to PORTA in a variety of configurations. The internal voltage reference divider can be used with the comparators to establish thresholds. Additionally, one of the comparator inputs can be configured to the RA2 port allowing for the use of an external voltage reference. By combining these elements, a first order modulator and first order filter can be designed, emulating the function of an analog-to-digital delta-sigma conversion.

This method of conversion is quickly implemented in firmware with very few additional external components. Consequently, the cost of hardware implementation is minimal, particularly for such a high resolution converter solution. The input range is very flexible and adjusted with external resistors. Although this method is not particularly strong in terms of DC accuracy, it is well suited for ratiometic applications.

DELTA-SIGMA THEORY

The function of the classical Delta-Sigma Analog-to-Digital Converter is modeled with two circuit segments; a modulator and a digital filter. The modulator section acquires an input signal as shown in Figure 1. The input signal is added to a signal from a Digital-to Analog (D/A) Converter in the negative feedback loop. This differentiated signal then passes through an integrator and finally to one of the two inputs of a comparator. The comparator acts like a one-bit quantitizer. The output of the comparator is sent back to the differentiator via a one-bit Digital-to-Analog Converter. Additionally, the output of the comparator passes through a digital filter. With time, the output of the digital filter provides a multi-bit conversion result.
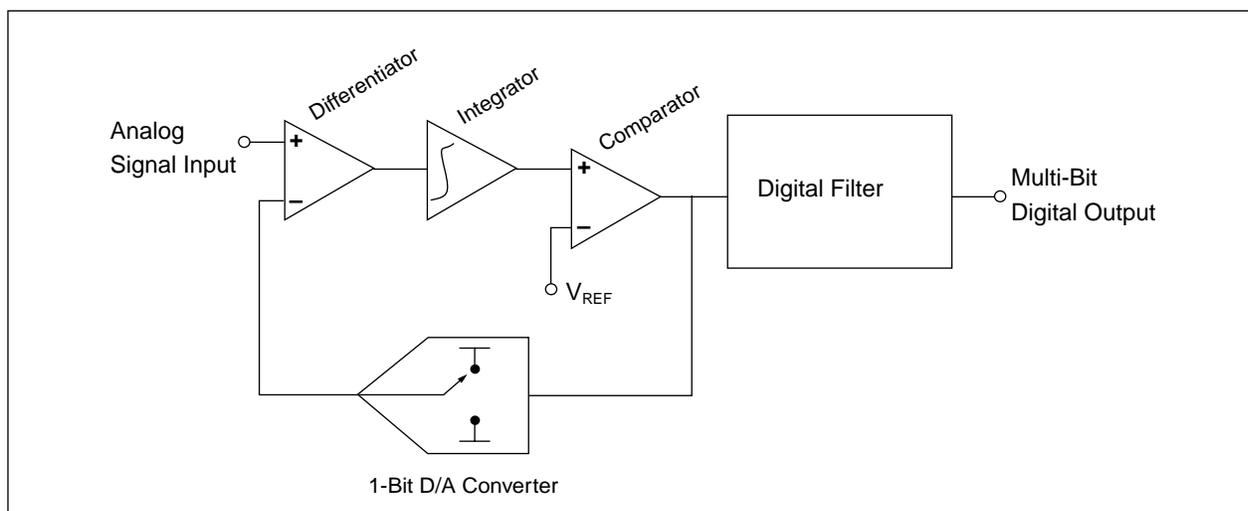

FIGURE 1: *First Order Delta-Sigma A/D Converter Block Diagram.*

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This fundamental circuit concept has been used to generate a large variety of the converters that provide high resolution, relatively inexpensively. The next logical step for this type of A/D Converter is to move it into the controller. A basic controller is not able to execute this type of function, however, a few additional peripherals make it possible. The circuit diagram for this type of implementation is shown in Figure 2.
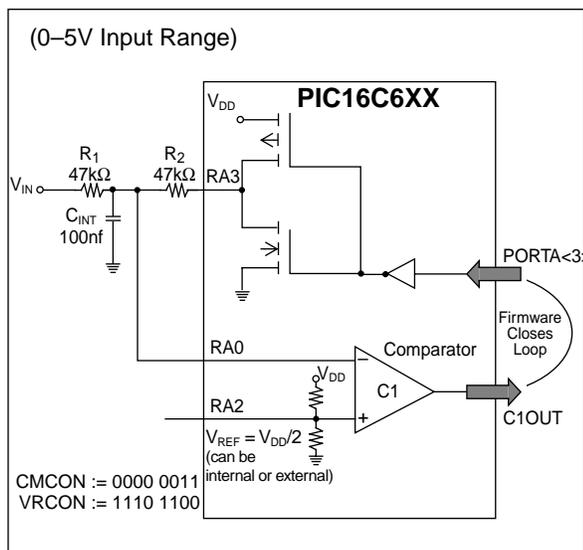

FIGURE 2: *A microcontroller can be configured as a Delta-Sigma Converter with two additional external resistors and one capacitor. In this configuration, a low pass filter is also implemented as part of the input network.*

In the circuit shown in Figure 2, the integrator function of the delta-sigma function is implemented with an external capacitor, C_{INT}. The absolute accuracy of this external capacitor is not critical, only its stability from integration to integration, which occurs in a relatively short period of time. When RA3 of the PIC16C6XX is set high, the voltage at RA0 increases in magnitude. This occurs until the output of the comparator (C1OUT) is triggered low. At this point the driver to the RA3 output is switched from high to low. Once this has occurred, the voltage at the input to the comparator (RA0) decreases. This occurs until the comparator is tripped high. At this point, RA3 is set high and the cycle repeats. While the modulator section of this circuit is cycling, two counters are used to keep track of the time and of the number of ones versus zeros that occur at the output of the comparator.

If this circuit were compared to the classical Delta-Sigma Converter, the integrator would be C_{INT}. The comparator is part of the controller, as well as its voltage reference. The one-bit D/A Converter is implemented in firmware by driving RA3 in accordance with the output of the comparator (CMCON<6>). The firmware drives the D/A Converter output at RA3. The digital filter is implemented with two counters.

IMPLEMENTATION WITH THE CONTROLLER

With the circuit in Figure 2, it is possible to conceptualize the delta-sigma function. The controller implementation of this circuit is summarized in the flow chart in Figure 3.
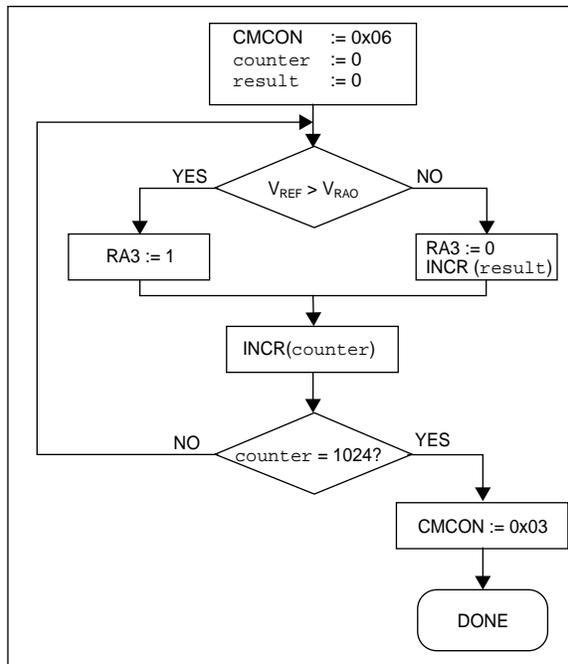

FIGURE 3: *A Delta-Sigma A/D Conversion Flow Chart implemented with circuit shown in Figure 2. Care should be taken to make the time required for every cycle taken through the flow chart to be a constant. This code is implemented until a conversion is complete.*

Normally the output of the comparator is directly connected to RA3 which keeps the voltage at RA0 equal to the reference voltage of the comparator in preparation for the next conversion.

When function "DeltaSigA2D" (Appendix A) is called to perform a conversion, the result and counter variables are cleared. Then the comparator is set to disconnect the output from RA3. This puts RA3 under active program control.

The comparator is checked at the beginning of each loop. If the voltage on the capacitor is less than the input voltage, RA3 is set high, which will put charge into the capacitor raising the voltage. If the voltage on the capacitor is greater than the input voltage, RA3 is set low, taking charge out of the capacitor lowering the capacitor voltage and the result register is incremented.

This continues as long as necessary to get the required resolution. For ten bits of resolution, 2^{10} (1024) laps through the loop are required. Each lap through the loop takes 17 instruction cycles. Padding is used to keep all paths through the code equal. A conversion cycle takes 17.5mS when using a 4 MHz clock.

When finished, the comparator output is fed directly to RA3, and the conversion is returned in result_l and result_h.

The sample code provided calls the DeltaSigA2D function and prints the result in an infinite loop. The output is transmitted at 9600 baud via RB7. The answers can be displayed on a dumb terminal program such as Hyperterm included with Windows '95.

FIGURE 4: *Conversion time versus bits of resolution assuming a 20μs integration time.*

Each integration result is taken at a regular time interval. If it is assumed that the time interval of a conversion is 20μs, the conversion time versus bits can easily be calculated. This relationship is shown graphically in Figure 4. For instance, a 10-bit conversion would require 2^{10} or 1024 samples. If the microcontroller conversion loop is 20μs, one complete conversion would take 20.48ms.

Room temperature test data for the circuit shown in Figure 2 is graphed in Figure 5. In Figure 5, the voltage input is plotted versus the output code on the left axis and the output error on the right axis. This data was taken with the 1024 laps through the flow chart in Figure 3. The expected resolution of this configuration is 10-bits. The maximum code error for this test was ±2 counts or 2-bits of uncertainty. Consequently, the effective number of bits of this A/D Converter is 8-bits. The core portion of the code that was used to perform this conversion is listed at the end of the application note.
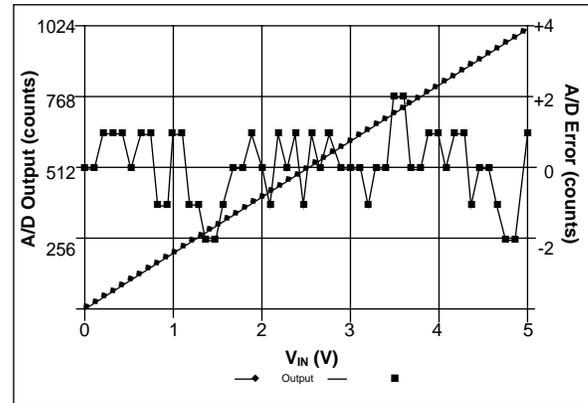

FIGURE 5: *Room temperature test data for the circuit shown in Figure 2. The input voltage range is 0.003 to 4.99V. The maximum error found in the test was ±2 counts. In this 10-bit system that is equivalent to ±9.8mV. This test was performed using one sample. Results may vary from part to part. V_{DD} = 5V, calibration performed at 0.5V and 4.99V.*

The A/D error was calculated assuming the codes for Vin = 0.5V and Vin = 4.5V are ideal. This test was performed with one microcontoller at room temperature. These result may vary from part to part.

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ERROR ANALYSIS

This high resolution, low cost Delta-Sigma Converter provides a good solution for ratiometric applications where having the absolute results is not critical. Additionally, the function of analog gain is replaced by the inherent digital filtering that this technique utilizes.

In this example, V_{DD} is 5V and the reference voltage is ~V_{DD}/2. The resistors are 47kΩ, which are chosen to minimize the leakage errors across the resistors versus the RDS_{ON} error of the output pin, RA3. The capacitor has a value of 100nF.

RDS_{ON} Error

This error comes from the drain-source resistance of the output FETs on the output pin, RA3. At room temperature, this resistance error is typically less than 100Ω. Compared to R_2, RDS_{ON} introduces about 0.2% gain error. This is easily compensated for by increasing the resistor, R_1 by approximately 100Ω. Additionally, the value of the RDS_{ON} resistance will increase with rising temperature. Assuming a temperature change from 20°C to 70°C, RDS_{ON} will change from ~100Ω to ~200Ω which adds an additional 0.2% error.

RA0 Port Leakage Current

This leakage current is specified at 1nA at room temperature and 0.5µA (max) over temperature. The leakage current from the port at RA0 causes a voltage drop across the parallel combination of R_1 and R_2. With these two resistors equaling 47kΩ, the error caused by this leakage current is ~11mV. This is also close to a 0.2% error. At room temperature this error is negligible. Leakage current does increase with temperature.

Non-Symmetrical Output Port (RA3)

When the output port is high the FET resistance is dependent on the p-channel on resistance. When the output port is low the FET resistance is dependent on the n-channel on resistance. The p-channel on resistance is usually greater than the on resistance of the n-channel FET. As a consequence, there is an additional offset contribution of 5.5mV at room and over temperature.

Voltage Reference

The internal voltage reference to the comparator is implemented with a simple voltage divider. The absolute value of this voltage is dependent on internal resistor matching and power supply voltage. Assuming the power supply is an accurate 5V, the voltage error of this reference, part to part is significant. However, once the initial error of the internal voltage reference is removed with calibration, it is ratiometric to the power supply.

This is the biggest error in the circuit, but easily reduced with an external voltage reference.

Integration Capacitor

Any leakage errors of the capacitor will contribute to the overall error of the system. If the RC time constant of the circuit is greater than the sample frequency, the non-linearity of this time response will cause a linearity error in the system.

In this case the RC time constant is equal to:

$$t_{RC} = R_1 || R_2 * C_{INT}$$

$$t_{RC} = 47kΩ || 47kΩ * 100nF$$

$$t_{RC} = 2.35ms$$

The dielectric absorbtion is not critical. This is due to the fact that the capacitor voltage is held at a relative constant level.

In this example, the maximum voltage deviation due to the non-linearity of the RC network is ~8mV. This is also below a 0.2% error. If a lower sampling frequency is used, the integrating capacitor must be increased in value.

Comparator Offset

The offset of the comparator is specified at 10mV (max). With a V_{DD} of 5V, the error caused by the comparator is ~0.2%.

Error Source	Contribution at Room Temp		Error Due to Temperature	
	Offset	Gain	Offset	Gain
RDS_{ON} or RA3 (with R1 = 47kΩ+100Ω)	negligible	negligible		0.2%
Port Leakage	negligible	N/A	11mV	N/A
FET Symmetry of RA3	5.5mV	negligible	5.5mV	N/A
Internal Voltage Reference	49mV	N/A	49mV*	N/A
Comparator Offset	10mV	N/A	10mV	N/A
Most Probable Total Error			52mV*	0.2%
* the offset error of the internal voltage reference can be reduced significantly with an external reference.				

TABLE 1: *Error contribution of all of the error sources at room and at temperature (-40 to 85°C) for R2 = 47kΩ. The "Most Probable Error Over Temperature" is calculated as the square root of the sum of the squares.*

Out of Range Inputs

In the event that the input signal goes to the maximum, minimum, or beyond the design limits, the converter will produce erroneous results. This problem can be corrected by decreasing R_2 by 10% to 20%.

Offset Adjustment

If the application requires that the effect of the system be nulled, this can be done by leaving V_{IN} open and running a conversion cycle. The results of this conversion will be equal to the offset voltage of the microprocessor system plus the external reference (if used).

OTHER INPUT RANGES

The configuration shown in Figure 2 is designed for a 0 to 5V input range. The input range for this circuit is determined by the resistor network (comprising of R_1 and R_2) and the reference voltage to the non-inverting input of the comparator. If the ratio of R_1 and R_2 is changed, the input range can be increased or decreased in accordance with the relationship between R_1 and R_2. Further adjustments can be implemented with an additional resistor added to this input structure that is biased to ground or the power supply.

Input Range of 2V to 3V

By adjusting the ratio of R_1 and R_2, the input range of this converter can be increased or decreased. The resistors that are selected for the circuit in Figure 6 reduces the input range from ±2.5V as in Figure 2 to +/-500mV. In both cases, the input range is centered around the reference voltage to the comparator, 2.5V. This type of input range is best suited for sensors with smaller output voltage ranges, such as the buffered output of a pressure sensor or load cell.

The resistors are determined by comparing the desired input range to the voltage range of RA3. Assuming that the reference voltage in this problem is 2.5V, the input range changes +/-500mV and the voltage at RA3 changes by +/-2.5V. The ratio of these two voltage ranges is 5:1. Consequently, during one integration period the difference between the current through R_2 and R_1 must always be less than zero. In this manner, the RA3 gate will be capable of driving the capacitor, C_{INT}, past the reference voltage applied to the non-inverting input of the comparator.
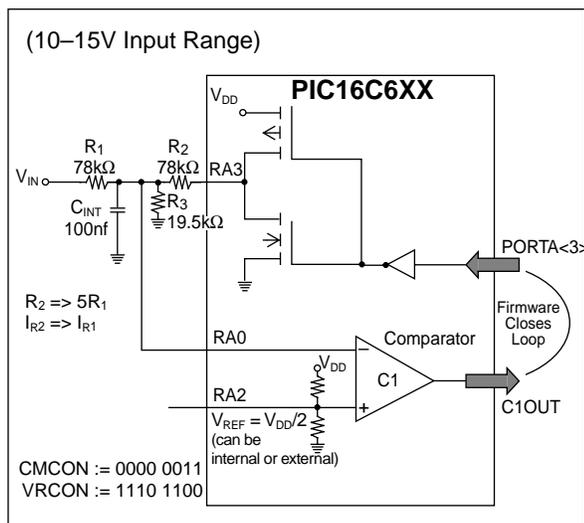

FIGURE 6: *Configuration of the microcontroller for a delta-sigma conversion with a ±500mV range centered around 2.5V.*

The design equations for this circuit are:

$$V_{IN(CM)} = V_{RA0}$$

$$V_{IN(P\ TO\ P)} = V_{RA3(P\ TO\ P)}\ (R_1/R_2)$$

where

$V_{IN(CM)}$ is equal to

$(V_{IN\ (MAX)} - V_{IN\ (MIN)})\ /2 + V_{IN\ (MIN)}$

V_{RA0} is the voltage applied to the comparator's inverting input

$V_{IN\ (P\ TO\ P)}$ is equal to $(V_{IN(MAX)} - V_{IN(MIN)})$

$V_{RA3\ (P\ TO\ P)}$ is equal to $V_{RA3(MAX)} - V_{RA3(MIN)}$

Input Range of 10V to 15V

By adding an additional resistor to the input structure of the A/D Converter, an offset adjustment can be applied to the input range. In Figure 7, R_1 and R_2 are equal and configured to allow for an input range of +/-2.5V as shown in Figure 2. The addition of R_3, which is referenced to ground, provides a level shift to the input range of 10V.

With this circuit configuration, a 5V (full-scale) current through R_1 is equal to V_{REF} / R_1. If R_3 is used to draw the same current to ground, the integrating capacitor will not be charged. In this manner, a 2.5V offset is implemented with $R_3 = R_1$. To achieve a 10V offset, R_3 must be equal to $4*R_1$ as shown in Figure 7.

FIGURE 7: *Configuration of the microcontroller for a delta-sigma conversion with a ±2.5V range centered around 12.5V.*

The design equations for this circuit are:

$$V_{IN(CM)} = V_{RA0} \ (1 + R_1/R_3)$$

$$V_{IN(P\ TO\ P)} = V_{RA3(P\ TO\ P)} \ (R_1/R_2)$$

where

$V_{IN(CM)}$ is equal to

$(V_{IN\ (MAX)} - V_{IN\ (MIN)}) \ /2 + V_{IN\ (MIN)}$

V_{RA0} is the voltage applied to the comparator's inverting input

$V_{IN\ (P\ TO\ P)}$ is equal to $(V_{IN(MAX)} - V_{IN(MIN)})$

$V_{RA3\ (P\ TO\ P)}$ is equal to $V_{RA3(MAX)} - V_{RA3(MIN)}$

Input Range of ±500mV

The circuit in Figure 8 using the scaling technique discussed in the circuit shown in Figure 5 and the offset shift technique discussed in the circuit shown in Figure 6. With this circuit, the input range is +/-500mV. This is achieved by making $R_2 = 5R_1$. Then the signal input range is level shifted by -2.5V. In the circuit in Figure 8 this is implemented with a resistor, R_3, to the positive supply. This level shift is achieved by making $R_3 = R_1$.
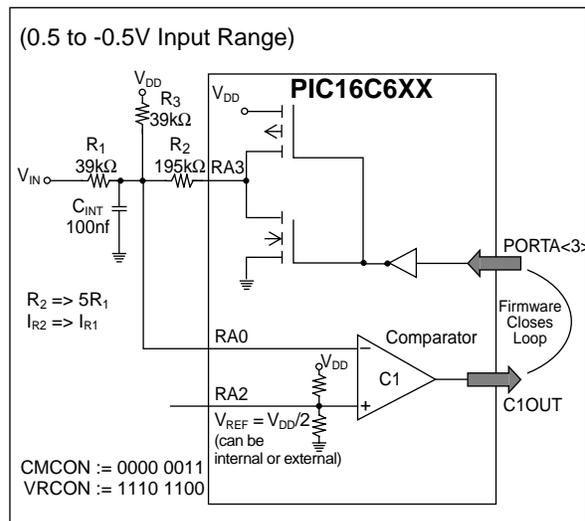

FIGURE 8: *Configuration of the microcontroller for a delta-sigma conversion with a ±500mV range centered around ground.*

The design equations for this circuit are:

$$V_{IN(CM)} = V_{RA0} \ (1 + R_1/R_3)$$

$$V_{IN(P\ TO\ P)} = V_{RA3(P\ TO\ P)} \ (R_1/R_2)$$

where

$V_{IN(CM)}$ is equal to

$(V_{IN\ (MAX)} - V_{IN\ (MIN)}) \ /2 + V_{IN\ (MIN)}$

V_{RA0} is the voltage applied to the comparator's inverting input

$V_{IN\ (P\ TO\ P)}$ is equal to $(V_{IN(MAX)} - V_{IN(MIN)})$

$V_{RA3\ (P\ TO\ P)}$ is equal to $V_{RA3(MAX)} - V_{RA3(MIN)}$

This circuit can be used to measure the current through a shunt resistor. The main error term at room temperature is comparator offset. In systems with a known "zero-current" state, the offset can be measured and removed through calculation or removed by adding or subtracting the offset to the `result` counter.

REFERENCES

Cox, Doug, "Implementing Ohmmeter/Temperature Sensor", AN512, Microchip Technology, Inc.

Richey, Rodger, "Resistance and Capacitance Meter Using a PIC16C622", AN611, Microchip Technology, Inc.

APPENDIX A: SOURCE CODE = DeltaSig.asm

```
;************************************************************************
;* Filename: DeltaSig.asm
;************************************************************************
;* Author:        Dan Butler
;* Company:       Microchip Technology Inc.
;* Revision:      1.00
;* Date:          02 December 1998
;* Assembled using MPASM V2.20
;************************************************************************
;* Include Files:
;*         p16C622.inc    V1.01
;************************************************************************
;* Provides two functions implementing the Delta Sigma A2D.
;* InitDeltaSigA2D sets up the voltage reference and comparator
;* in the "idle" state.
;* DeltaSigA2D runs the actual conversion.  Results provided in
;* result_l and result_h.
;*         See An700 figure 2 for external circuitry required.
;************************************************************************
;* What's changed
;*
;* Date    Description of change
;*
;************************************************************************
#include   <p16C622.inc>
cblock
           result_l
           result_h
           counter:2
endc
;
;
;
InitDeltaSigA2D
           bsf        STATUS,RP0
           movlw      0xEC
           movwf      VRCON
           bcf        PORTA,3         ;set comparator pin to output
           bcf        STATUS,RP0
           movlw      0x06            ;set up for 2 analog comparators with common reference
           movwf      CMCON
           return
;
;   Delta Sigma A2D
;   The code below contains a lot of nops and goto next instruction.  These
;   are necessary to ensure that each pass through the loop takes the same
;   amount of time, no matter the path through the code.
;
DeltaSigA2D
           clrf       counter
           clrf       counter+1
           clrf       result_l
           clrf       result_h
           movlw      0x03            ; set up for 2 analog comparators with common reference
           movwf      CMCON
loop
           btfsc      CMCON,C1OUT     ; Is comparator high or low?
           goto       complow         ; Go the low route
comphigh
           nop                        ; necessary to keep timing even
           bcf        PORTA,3         ; PORTA.3 = 0
           incfsz     result_l,f      ; bump counter
           goto       eat2cycles      ;
           incf       result_h,f      ;
           goto       endloop         ;
```

```
complow
        bsf     PORTA,3         ; Comparator is low
        nop                     ; necessary to keep timing even
        goto    eat2cycles      ; same here
eat2cycles
        goto    endloop         ; eat 2 more cycles
endloop
        incfsz  counter,f       ; Count this lap through the loop.
        goto    eat5cycles      ;
        incf    counter+1,f     ;
        movf    counter+1,w     ;
        andlw   0x04            ; Are we done? (We're done when bit2 of
        btfsc   STATUS,Z        ; the high order byte overflows to 1).
        goto    loop            ;
        goto    exit            ;
eat5cycles
        goto    $+1             ; more wasted time to keep the loops even
        nop                     ;
        goto    loop            ;
exit
        movlw   0x06            ; set up for 2 analog comparators with common reference
        movwf   CMCON
        return
        end
```

NOTES:

NOTES:

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable".
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