AN7721/22
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- 8-bit resolution
- Up to 250 MSPS conversion rate
- Single +5 V supply required for SPT7721/22
- On-board clock driver and reset circuit
- On-board adjustable references and common mode
- On-board single-ended to differential input buffer, with adjustable level
- On-board single-ended to differential transformer (1:1)
- Digital output buffers
- 3.3/5 V logic output

APPLICATIONS

- Evaluation of the SPT7721/22
- Engineering system prototype aid
- Major block for prototype system
- Guide to system layout
- AC dynamic analysis of the SPT7721/22 (with customer-provided data capture and FFT system)

DESCRIPTION

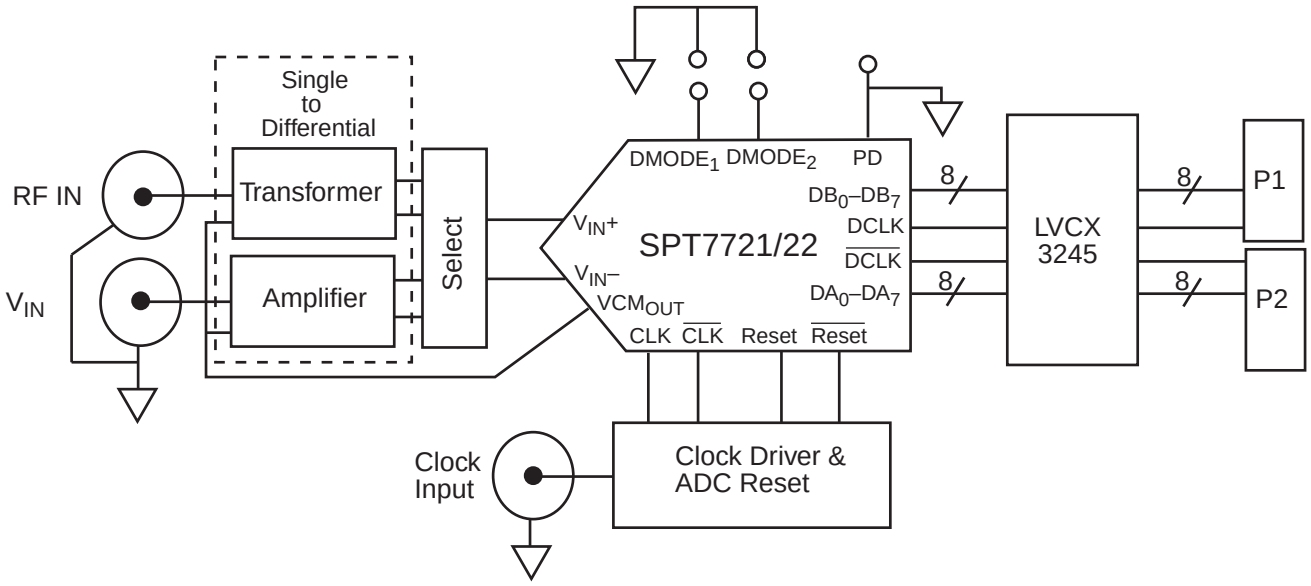
The SPT7721/22 8-bit analog-to-digital converter, with a sample rate of 250 MSPS, is a fast differential analog input device. It provides outstanding dynamic performance with very low power dissipation and operates with a +5 V supply. It is available in a 44-lead thin quad flat pack (TQFP) package.

The EB7721/22 evaluation board is intended to be used as a tool for device characterization and to demonstrate the performance of the SPT7721/22.

The differential clock inputs of the SPT7721/22 are very flexible, operating over a wide voltage range. The digital data outputs are compatible with 3.3 V or 5 V logic.

The analog input of the SPT7721/22 permits ±0.5 V (typical) differential, with +2.5 V of common-mode voltage, internally provided. The board supports straight AC transformer coupling of input signal or op-amp buffering as single-to-differential converter. These input signals are mutually exclusive.

BLOCK DIAGRAM



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The 16 digital output bits, plus the data clock, are buffered out for downstream digital processing.

There is a clock buffer which will allow sinewave input to generate the differential PECL sample clock. In addition, there is a reset circuit which demonstrates how synchronization might be performed between two SPT7721/22s.

There are four separate voltage inputs that power the various circuits on the evaluation board. They are: ±5 V analog; +3/5 V digital, which determines the output logic voltages for the SPT7721/22; and +3.3 V digital, which provides the supply for the final output stage of the EB7721/22.

The EB77721/22 description consists of seven separate sections. Each will be discussed in detail in this application note. They include the following:

Power Supplies and Grounding
Layout
Analog Inputs
Common Mode Voltage
Clock/Reset Circuits
Digital Output
Control Options and Test Points

Figure 3 shows a detailed schematic of the evaluation board. Table III is a list of materials/parts for the EB7721/22. Layouts of the board layers have been included (Figures 4, 5, 6, and 7). The board has an area for breadboarding of additional circuits as required by the user.

POWER SUPPLIES AND GROUNDING

The EB7721/22 requires analog ±5 V (designated +A5 and –A5 on the board), digital +5 or +3 V for output (designated +D3/5 on the board), and +3.3 V digital supply for output buffers (designated +D3.3 on the board).

The ±A5 supplies the single-to-differential operational amplifier, the SPT7721/22 (AV_{CC}), and the clock and reset circuits.

The +D3/5 digital supply provides power to the SPT7721/22 ODV_{DD} pins and to the $V_{CC}B$ pins of the output buffers.

The +D3.3 powers the final outputs stage of the output buffers.

Power supply connection points are labeled for operator convenience. Before connecting any power supply to the evaluation board, set the supply to the correct value and power off. Ensure all power supplies are connected and preset before full power is applied. Figure 1 shows the proper connection of the power supplies. After powerup, verify the supply voltages are within specification before proceeding (refer to Table I). Make any necessary adjustments, referencing your measuring instrument to the appropriate return node. The typical currents listed are with a 200 MHz clock and 50 MHz input.

Figure 1 – Power Supply Connections

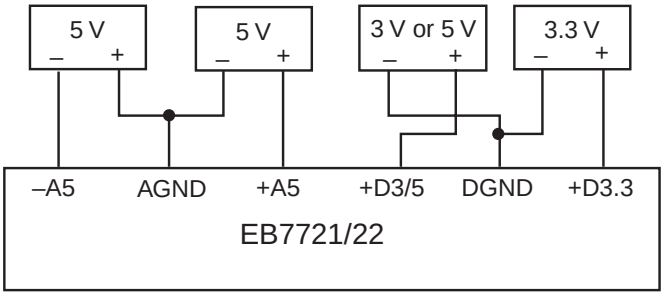


Table I – Power Supply Requirements

	Vmin	Vtyp	Vmax	Ityp
–A5	–4.9 V	–5 V	–6 V	–11 mA
+A5	+4.9 V	+5 V	+6 V	+412 mA
+D3.3	+2.7 V	+3.3 V	+3.6 V	+110 mA
+D3/5	+2.7 V	+3.3 V	+5.5 V	+42 mA

The SPT7721/22 was designed to use a common analog and digital ground plane. The EB7721 application board separates the analog at the SPT7721/22 and it is at this split that SPT recommends connecting analog and digital grounds together using a ferrite bead.

LAYOUT

This evaluation board was designed and manufactured with five layers: two signals (top and bottom layers), one ground plane layer with both analog and digital, and two power layers that accommodate all power distribution including all post-power-supply filtered power. The ordering of the layers are: Top–Signal (used for critical signals requiring controlled impedance), Second–Ground, Third–Power, Fourth–Power, and Bottom–Signal. The signal layers are designed with a controlled characteristic impedance of 50 ohms. Figures 4–7 show the actual layout for the EB7721/22.

ANALOG INPUTS

Analog input signals required for the SPT7721/22 are differential input signals presented to the V_{IN}+ and V_{IN}– pins.

The differential input signals may be applied from either one of two input circuits: the first is a single-ended to differential RF transformer; the second is through an op-amp, which takes a single-ended input and creates a differential analog input signal for the SPT7721/22.

The transformer circuit consists of a Mini-Circuit T1-6T RF transformer (1:1, with center tap), center-tapped secondary with a 1 dB pass-band from approximately 50 kHz to 300 MHz. The design is such that the differential output is loaded to a 50 ohm load, reflecting this back to the primary for impedance matching and maximum power transfer. Ensure J7 and J8 are jumpered appropriately when using the transformer input as the signal source.

The center tap of the RF transformer is driven by the V_{CM} output pin of the SPT7721/22. V_{CM} is typically 2.5 V nominal on the EB7721/22. The maximum input signal allowed at RF-IN is approximately 1 V peak-to-peak.

The A_{IN} signal source is processed by an op-amp (AD8131, U2) to create the differential input signal. The offset voltage required for the common mode is generated by the SPT7721/22.

Selection criteria of buffer op-amps are as follows:
- Dynamic range (open loop gain of >75 dB)
- Gain bandwidth >500 MHz
- THD <60 dB
- SNR >60 dB

The differential outputs of the amplifier drive respective sides of the SPT7721/22. In addition, clamping diodes (D2 and D3, SB101B) are designed in to ensure the input levels at powerup and during any other anomalistic occurrence do not exceed the limit specification for the input to this device.

SPT recommends appropriate bandpass filters on the input when performing AC characterization of this part.

COMMON-MODE VOLTAGE CIRCUIT

The SPT7721/22 has an on-chip common-mode voltage reference. It is typically 2.5 volts and is capable of driving 50 µA, typically. It is used for either one of two purposes on the EB7721/22. One use is to drive the center tap of the RF transformer at the RF-IN connection. The second use is to provide level shifting for the single-to-differential converter present at the A_{IN} connection.

CLOCK CIRCUIT

On-board clock drive is performed by a differential receiver. The receiver's reference is set by the VBB voltage available on that device. The drive signal is assumed to be a sinusoid signal; however, any modified signal with correct clock pulse width high and low would be allowed. The reference level would be approximately –1.3 V if operated with normal ECL supplies. Using elevated supplies in this application, its voltage will be 5 volts more positive, or +3.7 V. The VBB voltage is also summed with the input signal via the 50 ohm termination resistor R9. The peak-to-peak voltage of the zero-crossing sinewave input should be 1 V.

The output of the differential receiver goes to a 100E104 XOR gate. This device acts as a buffer for the clock which drives the CLK and /CLK pins of the SPT7721/22. In addition, some gates are used in conjunction with a manual switch and the 100EL30 triple D Flip-Flop to generate the RESET and /RESET signals for the SPT7721/22.

Ensure the clock source signal is capable of driving a 50 ohm load. If it is not, modify the input termination resistor (R9) to accommodate the user's drive circuit.

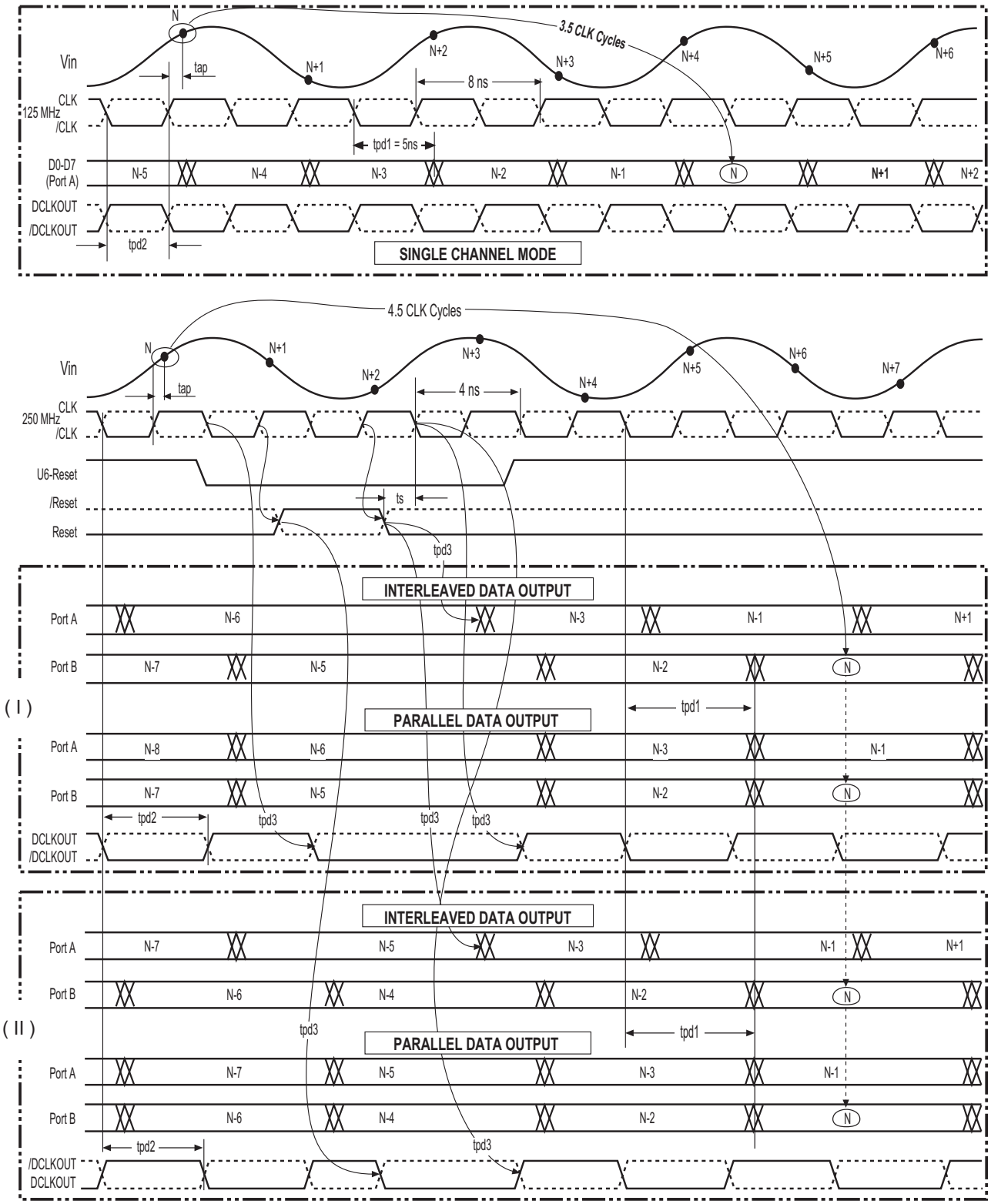
DIGITAL OUTPUT

The SPT7721/22 output can be 3.3 V logic or 5 V logic. Digital buffers/voltage translator ICs were used, which will accept either logic level and will support +3.3 V logic levels on the output. To select the SPT7721/22 output logic levels, the user will need to adjust the +3.3/5 V power supply. The input side of digital buffers U3 and U4 can operate at either voltage and is determined by the same supply.

The EB7721/22 provides the eight A-bank data outputs and the DCLK_OUT signal from the SPT7721/22 to the P2 connector. Also present on this connector are the +D3/5 supply and access to the output enable to U4. The 8,B bank data outputs and the /DCLK_OUT signals appear at the P1 connector. Also available at P1 are the +D3/5 supply and access to the output enable of U3. Refer to Figure 3 for the pin-out of the P1 and P2 connectors. If the output enable signals of either U3 or U4 will be driven from external circuits, install the appropriate jumper (J1 or J2).

Note that series damping resistors (value of 47 ohms) are in series with the outputs of the EB7721/22 digital output buffers to reduce oscillations when there would be a mismatch of impedance or long signal or cable lengths from the output of the EB7721/22 to the user's receiver circuit. These may be modified or replaced with zero ohm resistors as the user's application may require. The user will need to furnish required latch and/or data storage circuitry external to the EB7721.

Figure 2 – Timing Diagram



NOTES:

1) Refer to SPT7721 data sheet for detail on tpd1, tpd2, tpd3 and ts
2) Rising edge of Reset forces DCLKOUT to Low
3) Both PortA and PortB output, DCLKOUT and /DCLKOUT will not switch when Reset is Hi

CONTROL OPTIONS AND TEST POINTS

Table II outlines the name, use and intent of the jumpers, test points and switches.

Table II – Control Options and Test Points

NAME	DESCRIPTION	INTENDED USE
J1	JUMPER PINS	Connect the /OE signal of U3 to connector P1
J2	JUMPER PINS	Connect the /OE signal of U4 to connector P2
J4	JUMPER PINS	Controls the logic level for $DMODE_1$. Removed = Logic High; installed = Logic Low
J5	JUMPER PINS	Controls the logic level for $DMODE_2$. Removed = Logic High; installed = Logic Low
J6	JUMPER PINS	Selects the negative power supply source for U2. "A" position is –5V, "B" position is analog ground
J7	JUMPER PINS	Selects the V_{IN}– source. "A" position is A_{IN}, "B" position is RF-IN
J8	JUMPER PINS	Selects the V_{IN}+ source. "A" position is A_{IN}, "B" position is RF-IN
CLK	TESTPOINT	Measure the Clock signal presented to the SPT7721/22
/CLK	TESTPOINT	Measure the /Clock signal presented to the SPT7721/22
RST	TESTPOINT	Measure the RST signal presented to the SPT7721/22
/RST	TESTPOINT	Measure the /RST signal presented to the SPT7721/22
/RST	SWITCH	Momentary switch used to provide the Reset signals to the SPT7721/22

SETUP AND CALIBRATION

The set-up and calibration operation involves setting power supplies, connecting and powerup, installing the proper jumpers, setting up and verifying sample clock operation, and verifying functional operation of the output of the EB7721/22. The following setup assumes the RF-IN is used for test.

1. Power supplies

Ensure that the power supplies are disconnected from the EB7721/22. Set power supplies according to Table I. Turn off supplies and connect power supplies to the evaluation board. Turn on all power supplies simultaneously.

2. Jumpers

J1 – Removed
J2 – Removed
J4 – Removed
J5 – Installed
J6 – A position
J7 – B position
J8 – B position

3. Sample Clock

Set user-provided 100 MHz, 1 V_{P-P} sinewave clock, or other desired clock frequency that is within the part specification. Connect clock to the CLK, SMA connector on the evaluation board.

4. Analog Input

Set up a 1 V_{P-P}, symmetrical around ground, 25 MHz sinewave signal or other appropriate frequency. Connect this signal to RF-IN.

5. Digital Output

If user does not have a digital capture system for processing and observing data, an oscilloscope or logic analyzer may be used to observe the digital-encoded data of the analog input signal.

Figure 3 – EB7721/22 Detailed Schematic

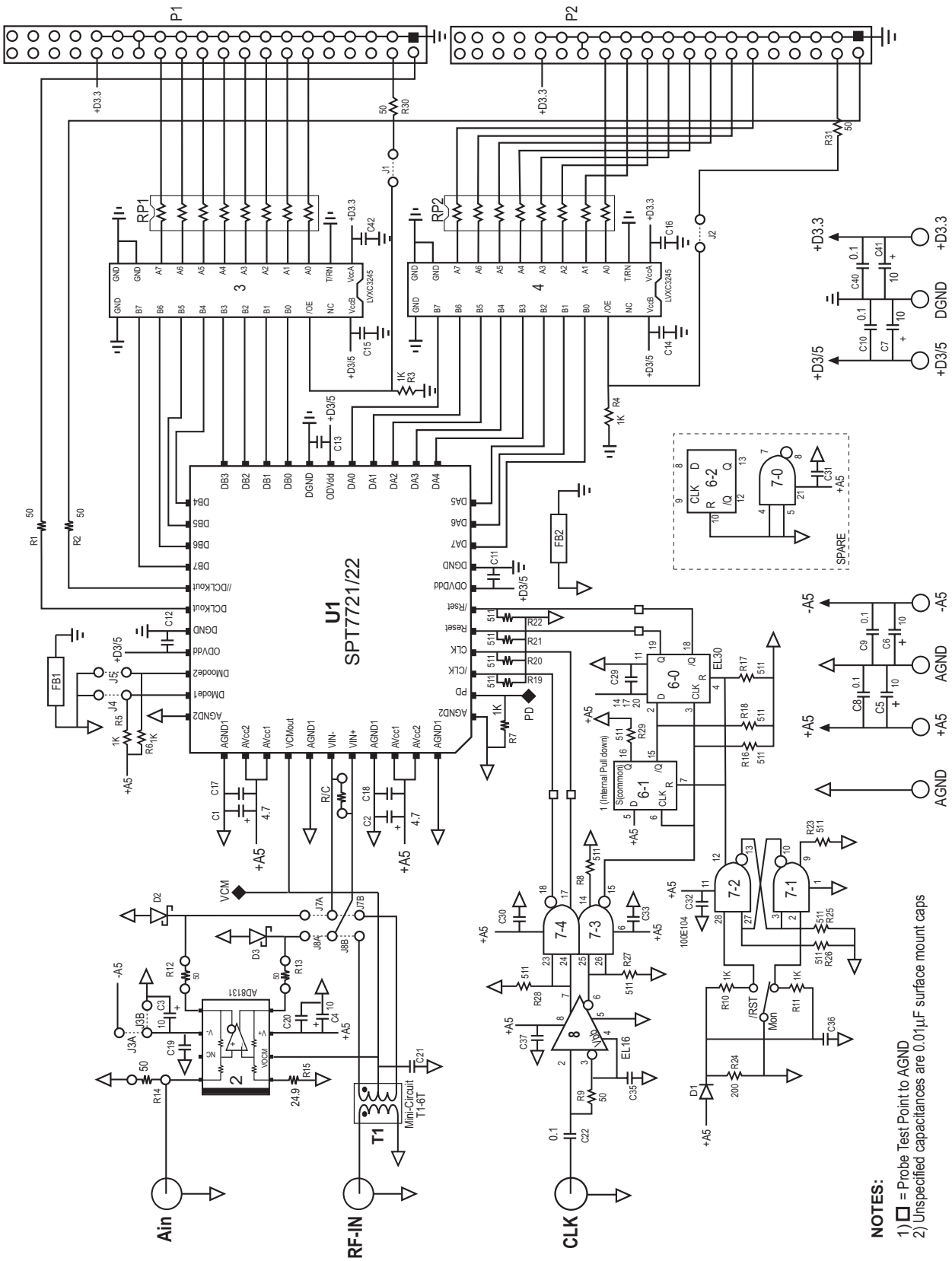


Table III – EB7721/22 Evaluation Board Bill of Materials

#	Reference	Manufacturer Part Number	Description	Qty	Suggested Manufacturer
1	C1,2	ECS-T1CY475R	4.7 µF Tantalum Chip Cap	2	Panasonic/Any
2	C3-7,41	ECS-T1CX106R	10 µF Tantalum Chip Cap	6	Panasonic/Any
3	C8-10,22,40	ECU-V1H104KBW	0.1 µF Chip Cap	5	Panasonic/Any
4	C11-21,29-33, 36-39,42	ECU-V1H103KBM	0.01 µF Chip Cap	21	Panasonic/Any
5	C25-28,34,35		DO NOT LOAD		
6	D1	1N4148DICT	Axial Diode	1	LiteOn / Any
7	D2,3	SD101B	Schottky Diode	2	LiteOn / Any
8	FB1,2	EXC-ELSA35V	Ferrite Bead	2	Panasonic
9	J1-6,12-14	PZC36SAAN	Jumper Pins (trim from 36-Pin)	1	Sullins
10	J7,8	Pin Receptacles		NA	Per Item #31
11	J9-11	901-144-8-RFX	RF Connector (SMA)	3	Amphenol
12	J15-21	108-0740-001	Banana Jack	7	Johnson
13	P1,2	PZC36DBAN	40-Pin Horiz Male Conn (trim from 72-Pin)	2	Sullins
14	R1,2,9,30,31	ERJ-8ENF49R9	50 Ohm Chip Resistor	5	Panasonic/Any
15	R3-7,10,11	ERJ-8ENF1001	1 kOhm Chip Resistor	7	Panasonic/Any
16	R8,16-23,25-29	ERJ-8ENF5110	511 Ohm Chip Resistor	14	Panasonic/Any
17	R12-14	MFR-25FBF 49R9	50 Ohm Axial Resistor (socketed)	3	Yageo / Any
18	R15	ERJ-8ENF24R9	25 Ohm Chip Resistor	1	Panasonic/Any
19	R24	ERJ-8ENF2000	200 Ohm Chip Resistor	1	Panasonic/Any
20	R/C		TO BE DETERMINED (socketed)		
21	RP1,2	761-3-R47	47 Ohm 8-Res DIP Array	2	CTS
22	S1 (“/RST”)	ET08SD1CBE[1]	Mom. Toggle Switch	1	C&K
23	TP1-6	40F6045	Solder Terminal	6	NEWARK
24	U1	SPT7721/22	8-Bit, 250 MSPS ADC	1	SPT
25	U2	AD8131 AR	Differential Driver	1	Analog Devices
26	U3,4	74LVXC3245 (M24B)	3-State Transceiver/Register	2	National
27	U5	T1-6T (KK81)	RF Transformer	1	Mini-Circuits
28	U6	MC100EL30DW	Triple D Flip-Flop	1	Motorola
29	U7	MC100E104FN	Quint AND/NAND Gate	1	Motorola
30	U8	MC10EL16D	Differential Receiver	1	Motorola
31	N/A	ED5044-ND	Pin Receptacles (for “socketed” parts)	14	DIGI-KEY
32	N/A	929955-06	Shunt for Jumper	5	DIGI-KEY (3M)
33	N/A	1902EK-ND[2]	1" Nylon Spacer	4	DIGI-KEY
34	N/A	H143-ND[2]	4-40 Pan-head Screw	4	DIGI-KEY
35	EB7721/22	Rev A	Evaluation Board	1	Short Circuits

[1] Mount with toggle to the left.
[2] Mount in four corners as bottom side legs.

Figure 4 – EB7721/22 Top Layer – Signal

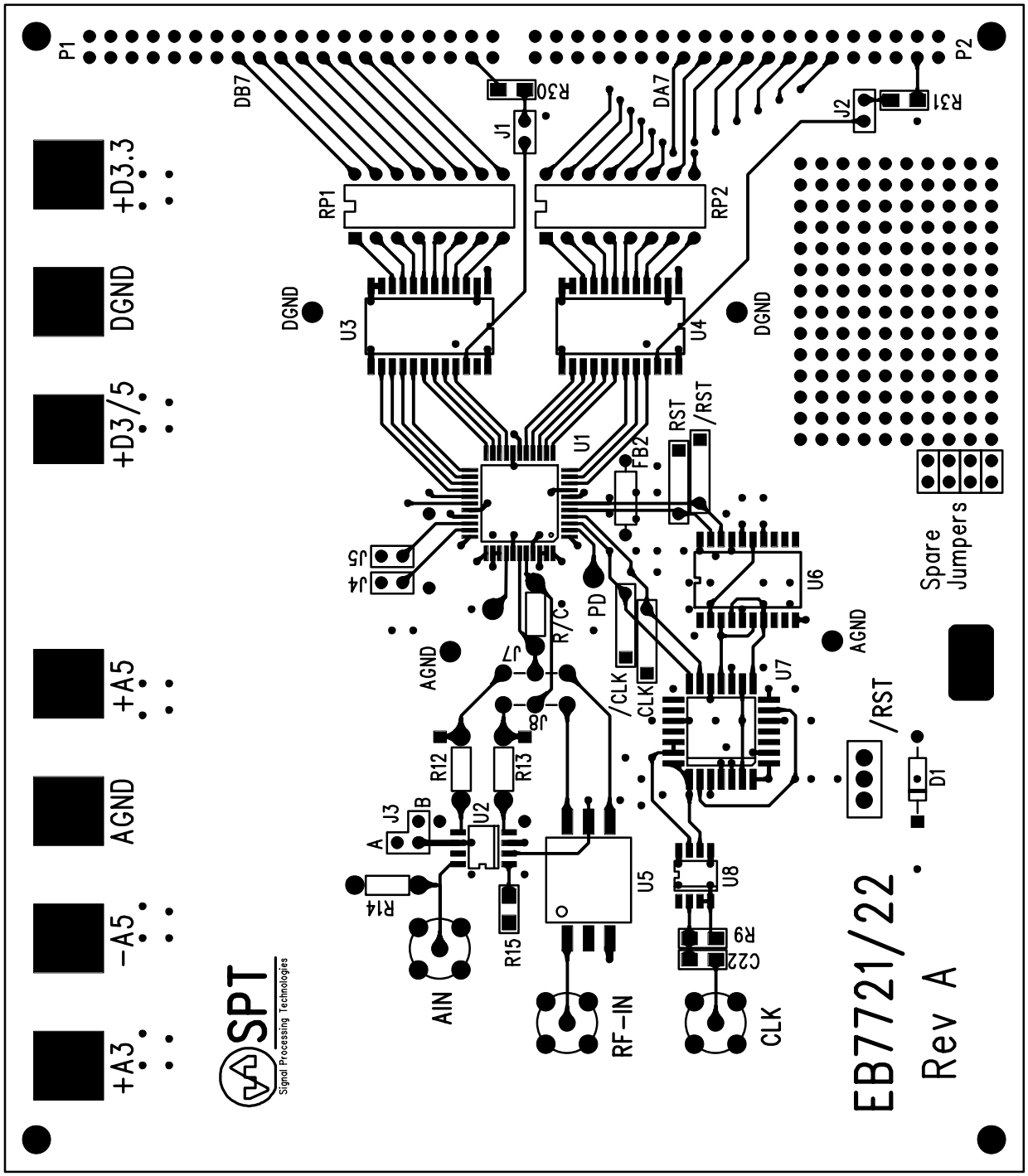


Figure 5 – EB7721/22 Second Layer – Ground

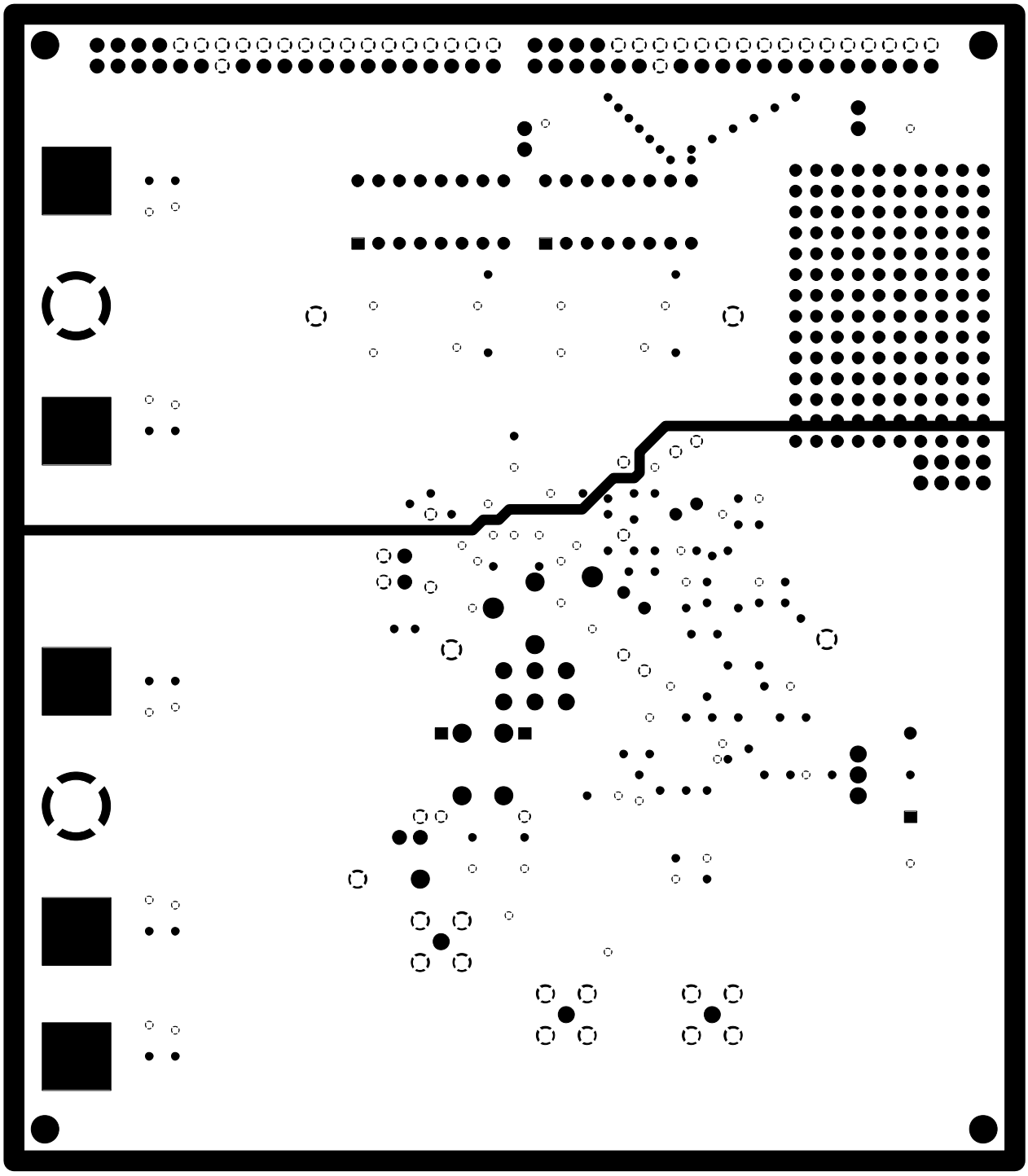


Figure 6 – Third and Fourth Layers – Power

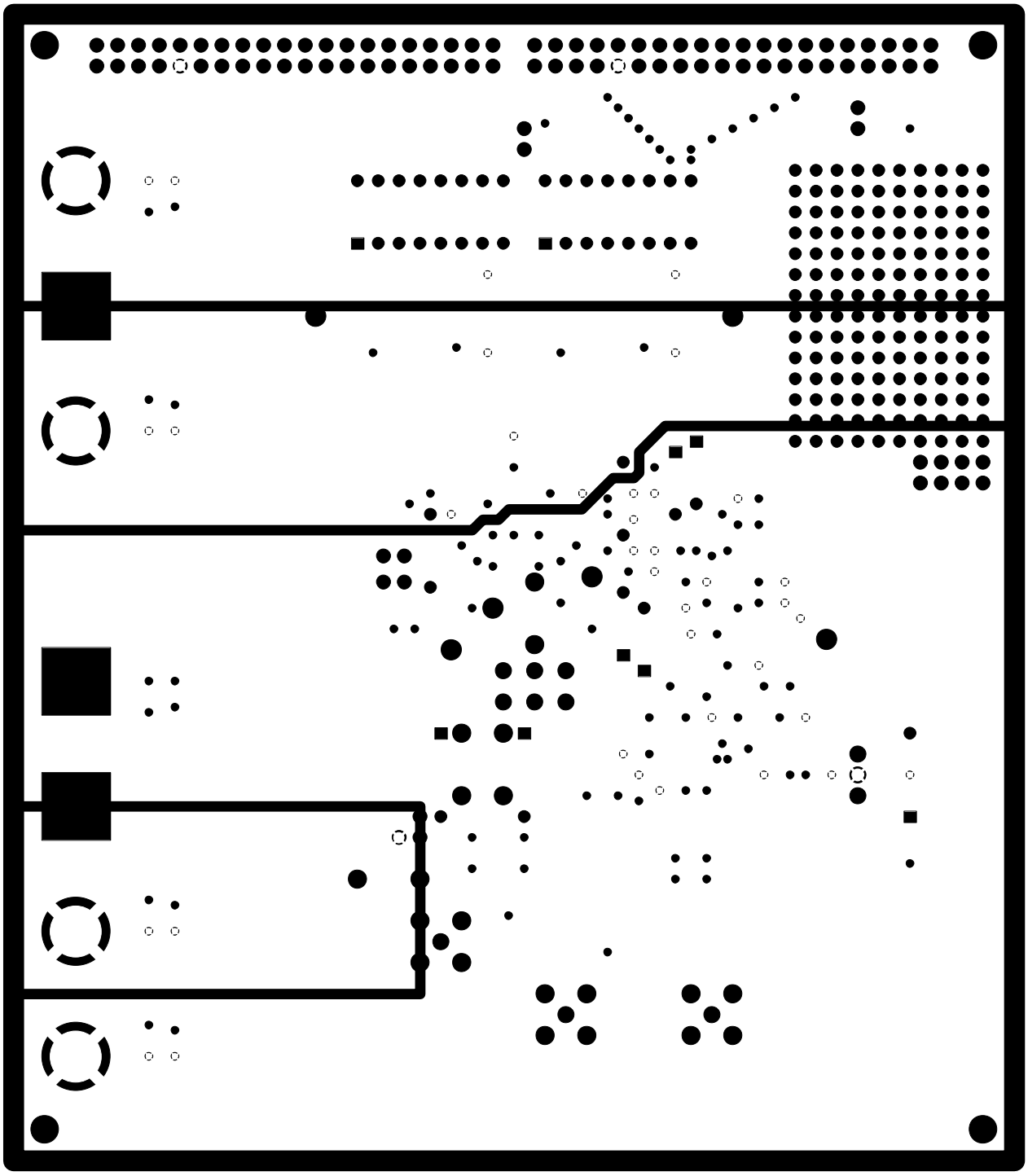


Figure 7 – Bottom Layer – Signal