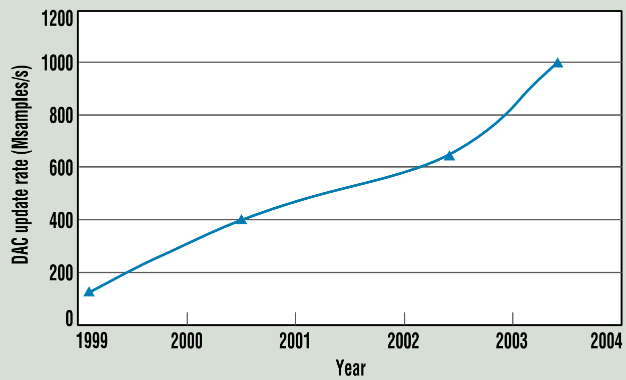
DACs Ready To Tackle New Challenges

DIGITAL-TO-ANALOG CONVERTERS (DACS) have made significant strides in the last few decades and have spurred the use of digital techniques in a multitude of applications. The performance from a single chip only seems to get better every day as processes continue to advance and novel topologies continue to emerge. Hybrids and boards are relegated to niche applications where users are looking for a total solution with specific features and interfaces from a single module or board. Meanwhile, monolithics have taken control of the majority of applications.

Today, 24-bit resolution accompanied by excellent performance from a single low-cost miniature package is standard. CMOS reigns in areas where density must accompany low power and low supply voltages. BiCMOS takes precedence where speed and resolution must be combined with superior ac and dc performance. Progress in process technologies is letting designers pack multiple high-performance, high-resolution DACs on one die. In addition, more functions and features are being integrated without compromising performance, while keeping the power budget under control and the cost attractive.



Driven by some emerging applications, integration is on the rise. To serve optical switching requirements, some suppliers are attempting to pack 128 DACs in one package. Others are integrating high-resolution devices with flash memory to store linearization curves, as well as adding the latest I^2C interface. Furthermore, high-performance DACs are being merged with powerful DSP cores on the same piece of silicon.

The future even looks brighter as self-adaptive silicon techniques are ready to tackle new challenges and bring themselves on a par with mainstream digital circuits. Both precision analog and faster digital circuits can reside side by side on a single SoC solution using the lowest-cost, highest-density standard CMOS process available from any foundry.

The delta-sigma (Δ-Σ) architecture continues to dominate high-resolution DACs that run at slow to moderate speeds. In this sector, designers combine a multibit second-order and higher architecture with a deep-submicron CMOS process to push resolution to 24 bits with high dynamic performance and low noise at 3- or 5-V single-supply voltages. As they exploit the state-of-the-art CMOS technology, these converters permit more functionality on-chip. They also allow multiple such units to be integrated on the same die for multichannel applications.

To meet the stringent dynamic requirements of 3G wideband, multicarrier cellular basestations, and broadband software radios, suppliers are readying segmented-current source DACs with 14-bit and better resolution with input data rates of 160 Msamples/s and output rates of 400 Msamples/s. Based on an interpolating architecture, they implement on-chip selectable 2x/4x/8x digital interpolation filters to provide high image rejection and low intermodulation distortion of –80 dBc up to 30 MHz. These converters, especially those from Analog Devices, also achieve adjacent-channel power ratio (ACPR) of –71 dBc at 71 MHz. In its latest incarnation, Texas Instruments (TI) has boosted the ACPR and third-order intermodulation distortion performance of its 14-bit 400-Msample/s offering to support IF frequencies above 150 MHz. Plus, it includes on-chip a low-voltage differential signaling interface (LVDS) to ASIC and FPGA.

For PC graphics, set-top boxes, and other imaging applications, the trend is toward monolithic 10- and 12-bit triple DAC chips with very good linearity specifications. For single-channel video DACs, the trend is toward 14 bits at a 20-Msample/s sampling rate, with 16-bit, 20-Msample/s versions on the drawing board. Signal Processing Technology *(www.spt.com)* has added such correction in its latest 14-bit solution to offer INL of 0.5 LSB and DNL close to 1 LSB.

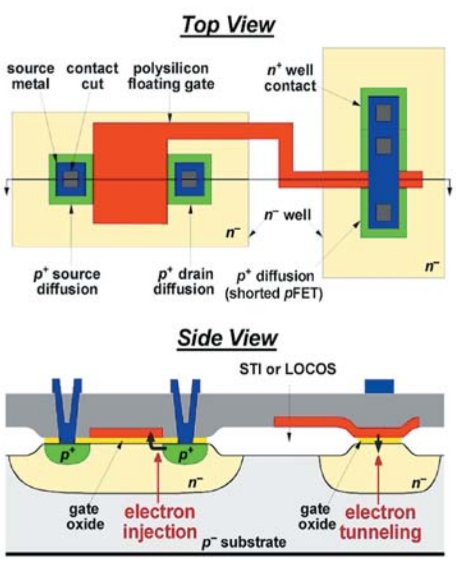
Today, 5-V DACs based on 0.35-µm CMOS are prevalent. Some 3-V high-resolution, high-performance versions have hit the market too. Now, the makers are prepping high-resolution and high-speed versions with excellent ac and dc performance to operate at 2.5 V. For instance, Signal Processing Technology *(www.spt.com)* is readying a 14-bit, 40-Msample/s unit to operate at 3 V, and a 10-bit, 70-Msample/s device to perform at 2.5 V.

analog/mixed-signal ICs<>DACs

Hybrid solutions will continue to take advantage of the fastest and greatest DAC chips on the market, combining them with the necessary functions and peripherals for a given application. In that way, they will deliver a complete high-performance solution from a single module.

Audio DACs with a 24-bit resolution and a 192-kHz sampling rate have achieved 120-dB SNR. AKM Semiconductor *(www.akm.com)* plans to integrate single-wire SPDIF interfaces on-chip to achieve performance at 3 V and below as well.

While the integration of analog and mixed-signal data converters with DSP processors or microcontrollers is common, merging a high-end DAC with a powerful DSP core on the same chip is a tough task. Analog Devices has recently made that integration possible *(www.analog.com)*. ADI's SigmaDSP line integrates a 24-bit Δ-Σ DAC with a 25-MIPS DSP engine on the same piece of silicon. In fact, there are three such DACs with a 48-kHz sampling frequency on this chip. The signal-to-noise ratio is 112 dB. The built-in DSP executes algorithms for real-world limitations of speakers, amplifiers, and listening environments of perceived audio quality.



Employing its patented self-adaptive silicon technology, startup Impinj *(www.impinj.com)* is bridging the gap between precision analog and faster digital circuits using a leading-edge digital CMOS process. The company is developing a 14-bit DAC based on TSMC's 0.25-µm CMOS, with plans to migrate to 0.18-µm and finer CMOS geometries. Characterization is in progress. However, Impinj's 14-bit DAC boasts a spurious-free dynamic range of 80 dB at a sample rate of 250 Msamples/s, while consuming only 50 mW and occupying a die area of 0.17 mm^2. The goal is to provide two orders of magnitude improvement in linearity via self trimming and calibration techniques.

Six or more high-performance, multichannel DACs are now packed on a single CMOS chip to serve surroundsound applications requiring super-audio CD (SACD) playback or other multichannel audio systems like the DVD. For high-density data-acquisition applications, octals at 12 bits and quads at 16 bits with low power consumption are adequately serving designers' needs. Texas Instruments' Burr-Brown Division *(www.ti.com)* is looking to push such density to 40 channels per chip with very fast settling times.

Makers will continue to tap the integration density and low-power benefits of deep-submicron CMOS, while driving the update rate of 12-bit parts to a new high. Combining deep-submicron CMOS with a novel-segment shuffling technique in segmented current-steering architecture, Fujitsu Microelectronics *(www.fujitsumicro.com)* has dramatically boosted the update data rate for 12-bit DACs to 400 Msamples/s. Such high-resolution, high-speed DACs also come with on-chip interpolation filters. Signal Processing Technology *(www.spt.com)* is exploiting CMOS to create high-resolution, high-speed parts with unprecedented power consumption. Its 10-bit, 400-Mword/s DAC uses 0.25-µm CMOS to keep full-speed consumption at 130 mW. The supply voltage is 3 V. For low-speed 16-bit resolution, Texas Instruments' Burr-Brown Division *(www.ti.com)* has demonstrated maximum consumption of 2 mW at 5 V, which reduces to 1 µW in the power down mode.

1954 Bernard M. Gordon co-invented the current switching DAC at EPSCO.

1970 Datel released 8-, 10-, and 12-bit DACs using discrete components. Analog Devices launched the first modular 12-bit DAC using thick-film resistors trimmed with sandblasting.

1973 Analog Devices introduced the first CMOS DAC.

1974 Analog Devices unveiled the first monolithic 10-bit CMOS chip with multiplying capability.

1982 Burr-Brown (now a division of Texas Instruments) readied the first 16-bit monolithic bipolar DAC with laser-trimmed thin-film resistors.

1986 Burr-Brown released the first CMOS DAC.

1987 Analog Devices released the first CMOS DAC with built-in reference.