GROUNDING IN MIXED SIGNAL SYSTEMS

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Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, the 12-bit AD7892 successive approximation (SAR) ADC operates on an 8MHz internal clock, while the sampling rate is only 600kSPS.

Sigma-delta (Σ-Δ) ADCs also require high speed clocks because of their high oversampling ratios. The AD7722 16-bit ADC has an output data rate (effective sampling rate) of 195kSPS, but actually samples the input signal at 12.5MSPS (64-times oversampling). Even high resolution, so-called "low frequency" Σ-Δ industrial measurement ADCs (having throughputs of 10Hz to 7.5kHz) operate on 5MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD7730 and AD7731).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

GROUND AND POWER PLANES

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high frequency currents (caused by fast digital logic) but

also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20nH/inch inductance. A transient current having a slew rate of 10mA/ns created by a logic signal would develop an unwanted voltage drop of 200mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20nH \times \frac{10mA}{ns} = 200mV.$$

For a signal having a 2V peak-to-peak range, this translates into an error of about 200mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 10.13 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

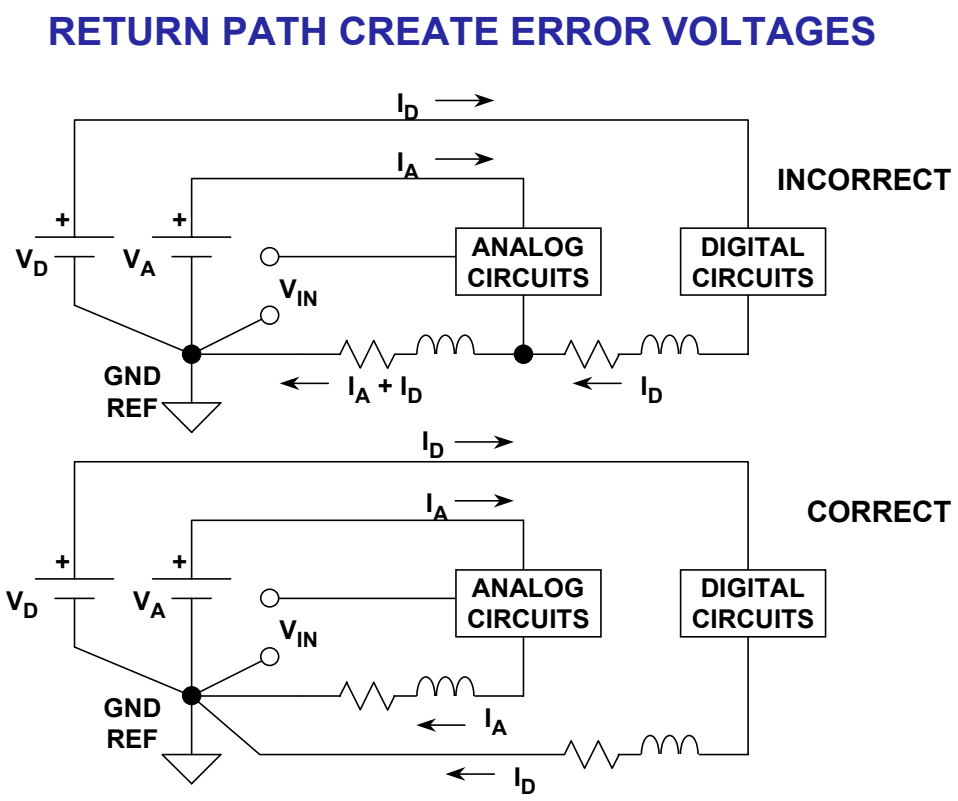

Figure 10.13

DOUBLE-SIDED VS. MULTILAYER PRINTED CIRCUIT BOARDS

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for

interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply. In most systems, 4-layers are not enough, and additional layers are required for routing signals as well as power.

GROUND PLANES ARE MANDATORY!

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
  - **Avoid High-Density Interconnection Crossovers and Vias Which Reduce Ground Plane Area**
  - **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards: Mandatory for Dense Systems**
  - **Dedicate at Least One Layer for the Ground Plane**
  - **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 10.14

MULTICARD MIXED-SIGNAL SYSTEMS

The best way of minimizing ground impedance in a multicard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 10.15.

2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

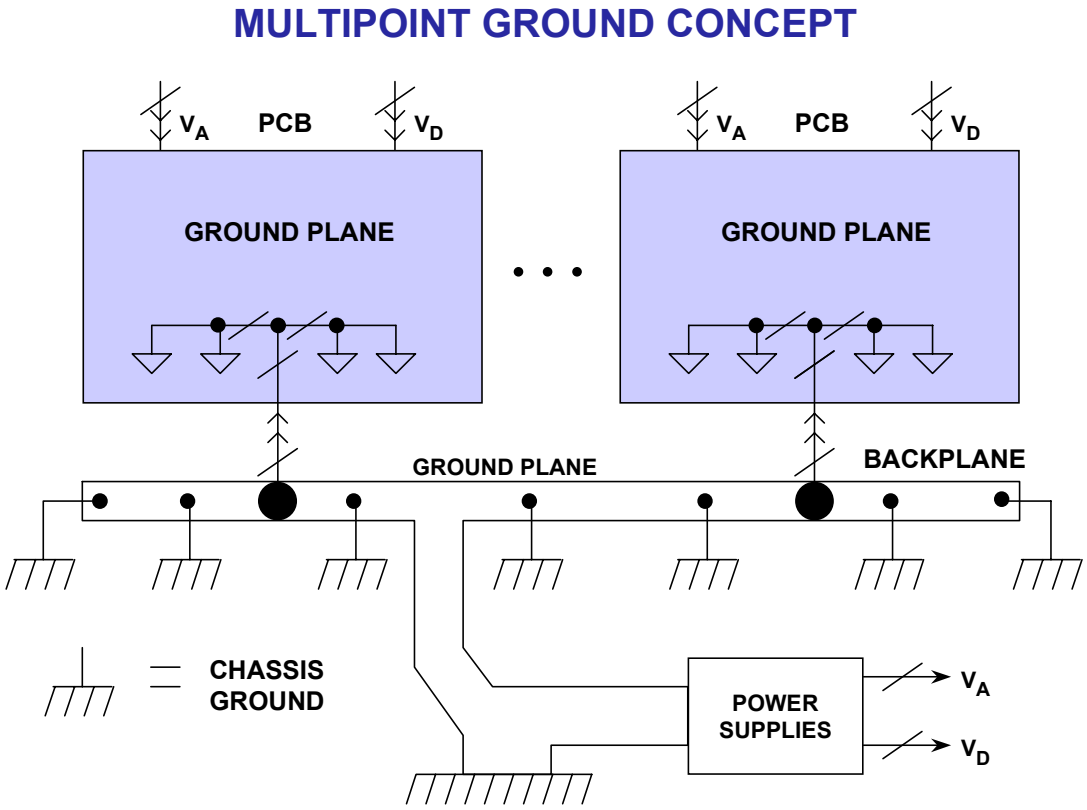

Figure 10.15

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently low and diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants further discussion.

SEPARATING ANALOG AND DIGITAL GROUNDS

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the

connector ground pins. The arrangement shown in Figure 10.16 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged. This voltage should be kept less than 300mV to prevent damage to ICs which have connections to both the analog and digital ground planes. Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents AC coupling between the analog and digital ground planes. Schottky diodes begin to conduct at about 300mV, and several parallel diodes in parallel may be required if high currents are expected. In some cases, ferrite beads can be used instead of Schottky diodes, however they introduce DC ground loops which can be troublesome in precision systems.

SEPARATING ANALOG AND DIGITAL GROUND PLANES

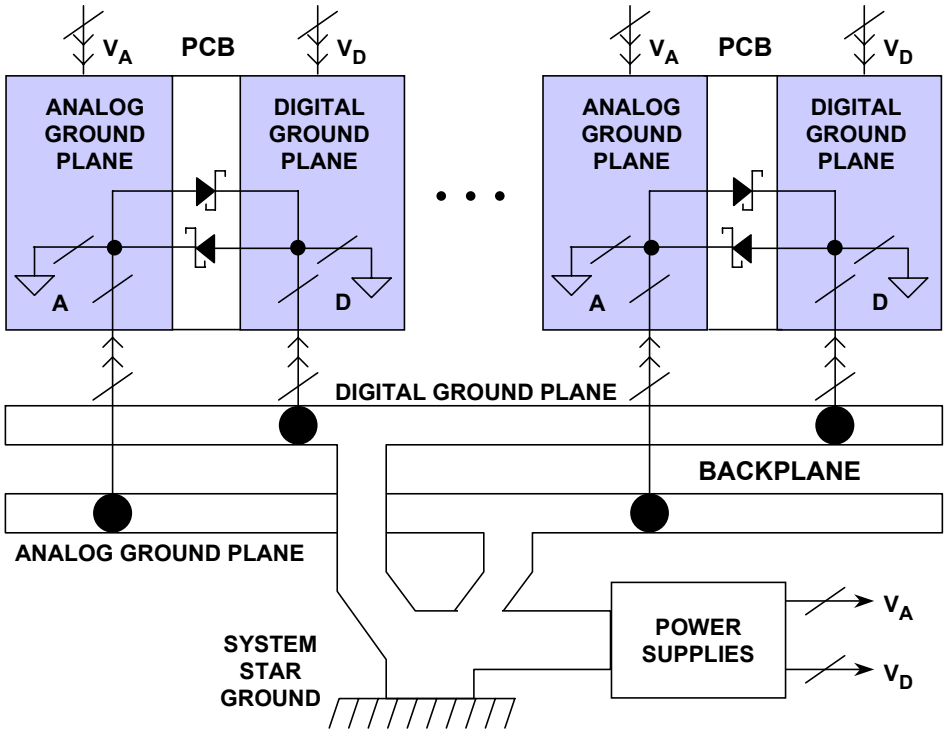

Figure 10.16

It is mandatory that the impedance of the ground planes be kept as low as possible, all the way back to the system star ground. DC or AC voltages of more than 300mV between the two ground planes can not only damage ICs but cause false triggering of logic gates and possible latchup.

GROUNDING AND DECOUPLING MIXED-SIGNAL ICS WITH LOW DIGITAL CURRENTS

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 10.17 will help to explain this seeming dilemma.

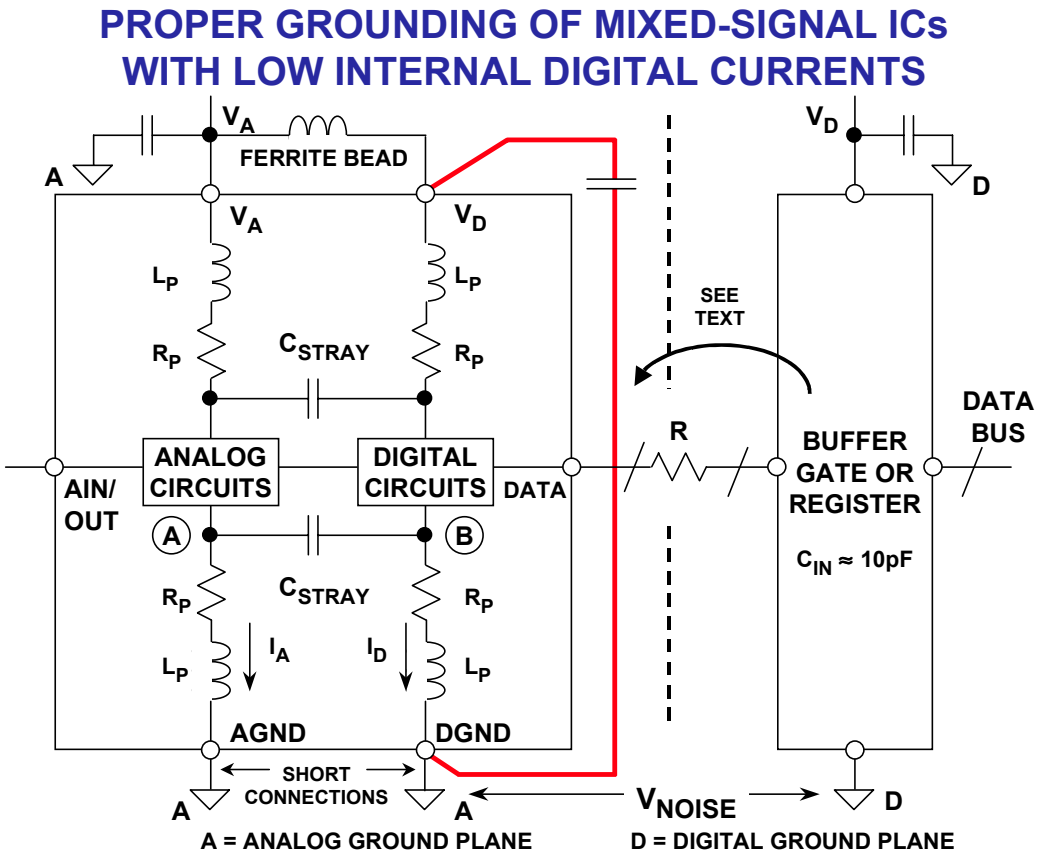

Figure 10.17

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 10.17 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 10.17. The internal transient digital currents of the converter will flow in the small loop from V_D through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop. The V_D pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01µF and 0.1µF.

TREAT THE ADC DIGITAL OUTPUTS WITH CARE

It is always a good idea (as shown in Figure 10.17) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice. In some cases it may be desirable to

add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

The series resistors (labeled "R" in Figure 10.17) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through-hole will create a load of approximately 10pF. A logic output slew rate of 1V/ns will produce 10mA of dynamic current if there is no isolation resistor:

$$\Delta I = C\frac{\Delta v}{\Delta t} = 10pF \times \frac{1V}{ns} = 10mA\ .$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\Omega \times 10pF = 11ns.$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 10.18. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5V, but the digital interface powered by +3V to interface to 3V logic. In this case, the +3V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3V digital logic supply.

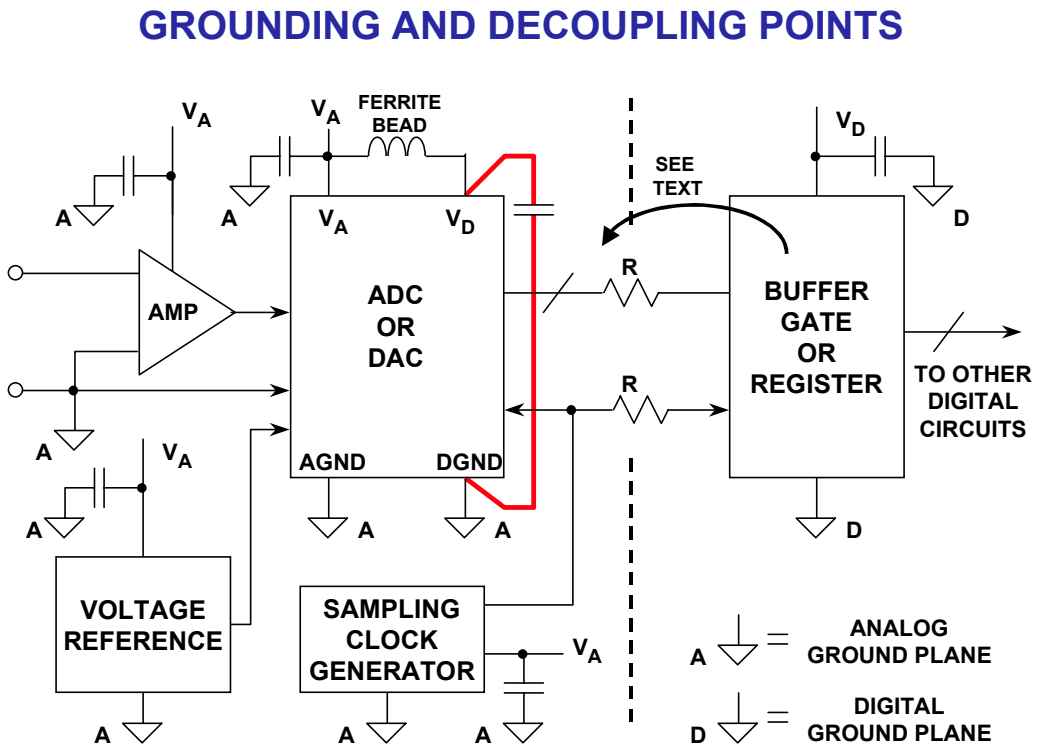

Figure 10.18

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

SAMPLING CLOCK CONSIDERATIONS

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC Signal-to-Noise Ratio (SNR) is given approximately by the equation:

$$SNR = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right],$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the RMS sampling clock jitter, t_j. Note that f in the above equation is the analog input frequency. Just working through a simple example, if t_j = 50ps RMS, f = 100kHz, then SNR = 90dB, equivalent to about 15-bits dynamic range.

It should be noted that t_j in the above example is the root-sum-square (RSS) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5ps RMS) CMOS compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801, Tel. 914-576-6570.)

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 10.19 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5V supply system, ECL logic can be connected between ground and +5V (PECL), and the outputs AC coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator.

SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES

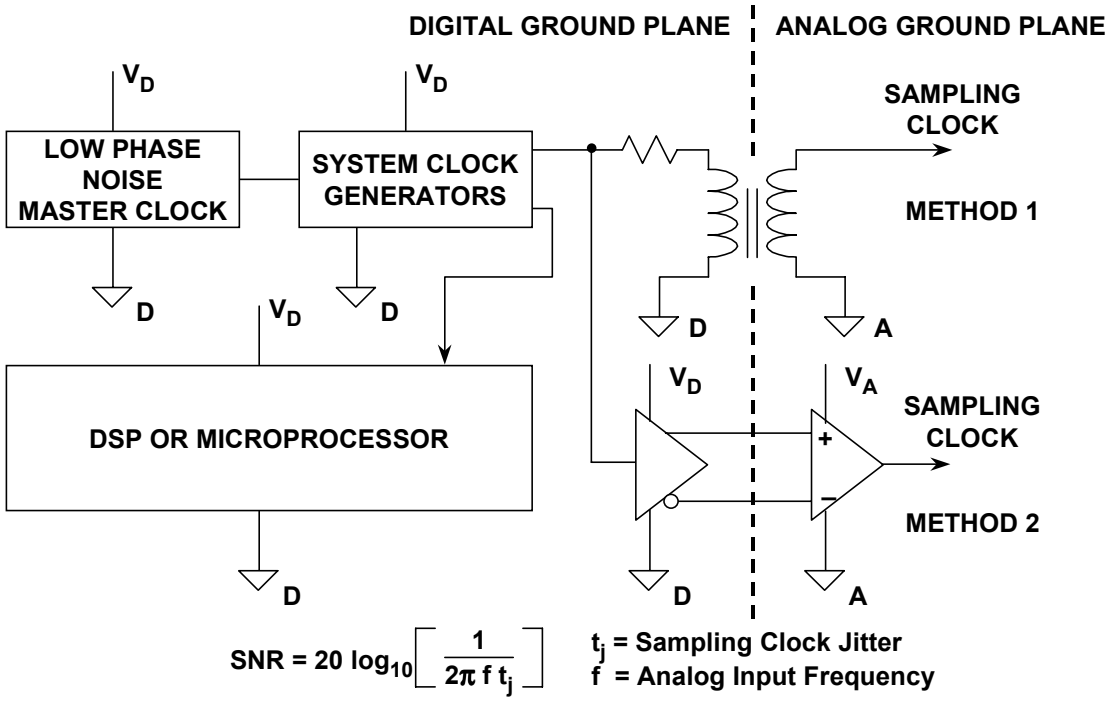

Figure 10.19

THE ORIGINS OF THE CONFUSION ABOUT MIXED-SIGNAL GROUNDING: APPLYING SINGLE-CARD GROUNDING CONCEPTS TO MULTICARD SYSTEMS

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in Figure 10.20. This essentially creates the system "star" ground at the mixed-signal device.

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multicard systems, and

the approach previously discussed should be used for mixed signal ICs with low digital currents.

GROUNDING MIXED SIGNAL ICs : SINGLE PC BOARD (TYPICAL EVALUATION/TEST BOARD)

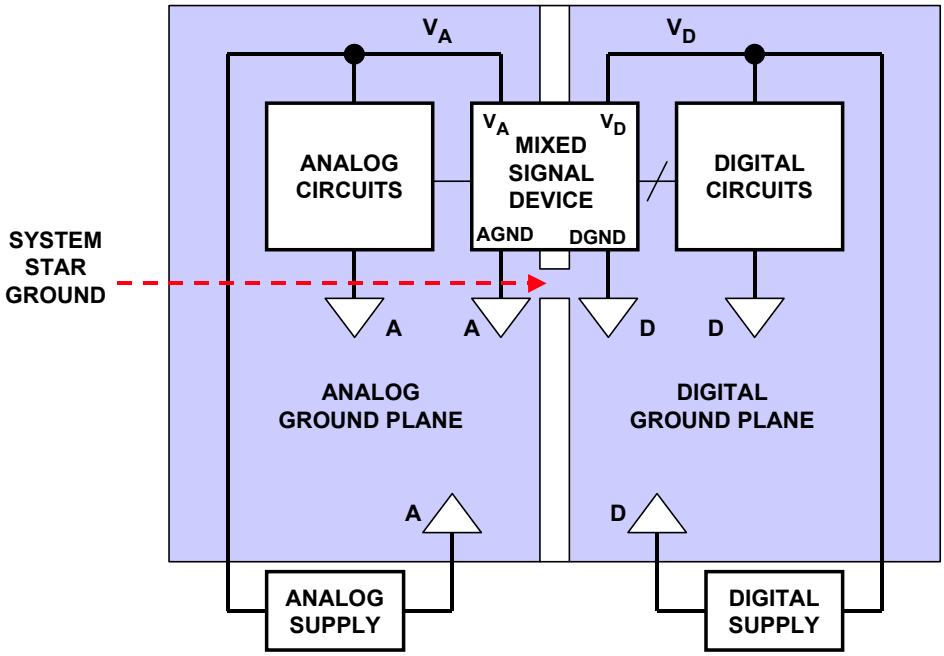

Figure 10.20

SUMMARY: GROUNDING MIXED SIGNAL DEVICES WITH LOW DIGITAL CURRENTS IN A MULTICARD SYSTEM

Figure 10.21 summarizes the approach previously described for grounding a mixed signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between V_D, the decoupling capacitor, and DGND (shown as a heavy line). The mixed signal device is for all intents and purposes treated as an analog component. The noise V_N between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300mV by using a low impedance digital ground plane all the way back to the system star ground.

However, mixed signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device. The method previously discussed depends on the decoupling capacitor between V_D and DGND to keep the digital transient currents and isolated in a small loop. However, if the digital currents are

significant enough and have components at DC or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current which flows outside the loop between V_D and DGND must flow through the analog ground plane. This may degrade performance, especially in high resolution systems.

GROUNDING MIXED SIGNAL ICs WITH LOW INTERNAL DIGITAL CURRENTS: MULTIPLE PC BOARDS

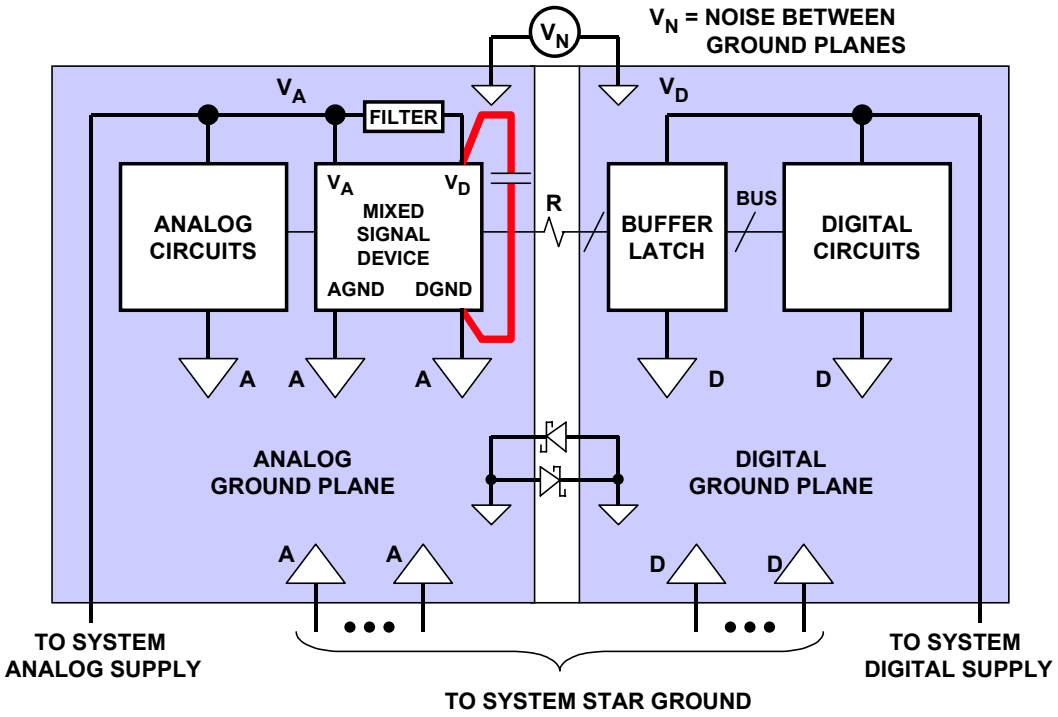

Figure 10.21

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

SUMMARY: GROUNDING MIXED SIGNAL DEVICES WITH HIGH DIGITAL CURRENTS IN A MULTICARD SYSTEM

An alternative grounding method for a mixed signal device with high levels of digital currents is shown in Figure 10.22. The AGND of the mixed signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

GROUNDING ALTERNATIVE FOR MIXED SIGNAL ICs WITH HIGH DIGITAL CURRENTS: MULTIPLE PC BOARDS

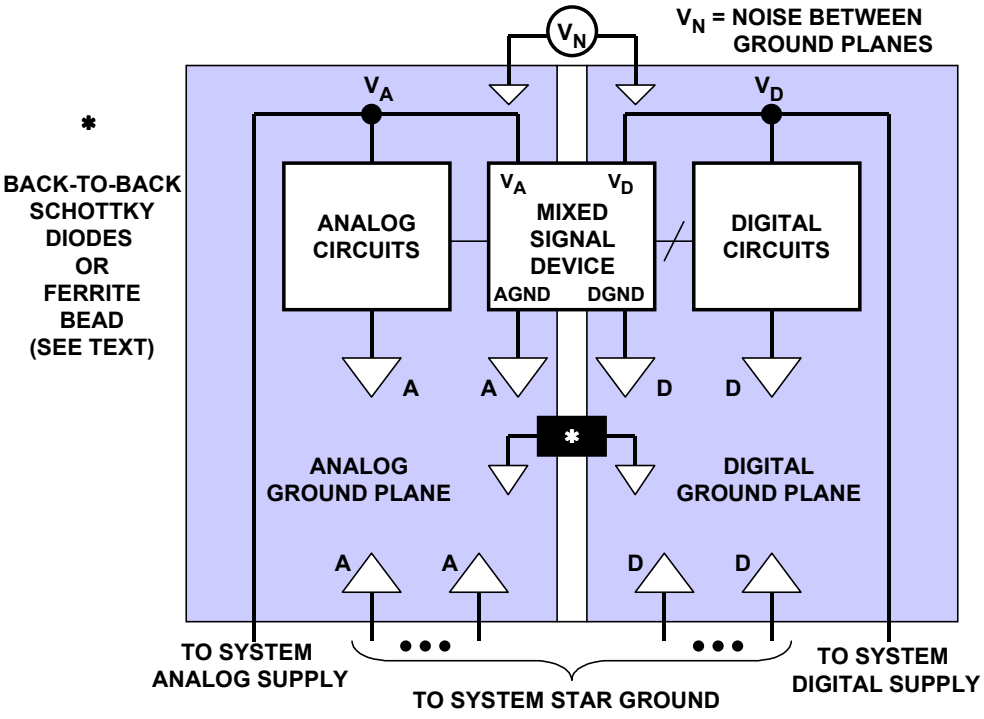

Figure 10.22

Figure 10.22 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large DC voltages or low frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed signal IC if they exceed 300mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a DC connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from DC voltages between AGND and DGND, but the DC connection provided by the ferrite bead can introduce unwanted DC ground loops and may not be suitable for high resolution systems.

GROUNDING DSPS WITH INTERNAL PHASE-LOCKED LOOPS

As if dealing with mixed-signal ICs with AGND and DGNDs wasn't enough, newer DSPs such as the ADSP-21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user-selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN. The CLKIN rate is the rate at which the synchronous external ports operates. Although this allows using a lower frequency external clock, care must be taken with the power and ground connections to the internal PLL as shown in Figure 10.23.

GROUNDING DSPs WITH INTERNAL PHASE-LOCKED-LOOPS (PLLs)

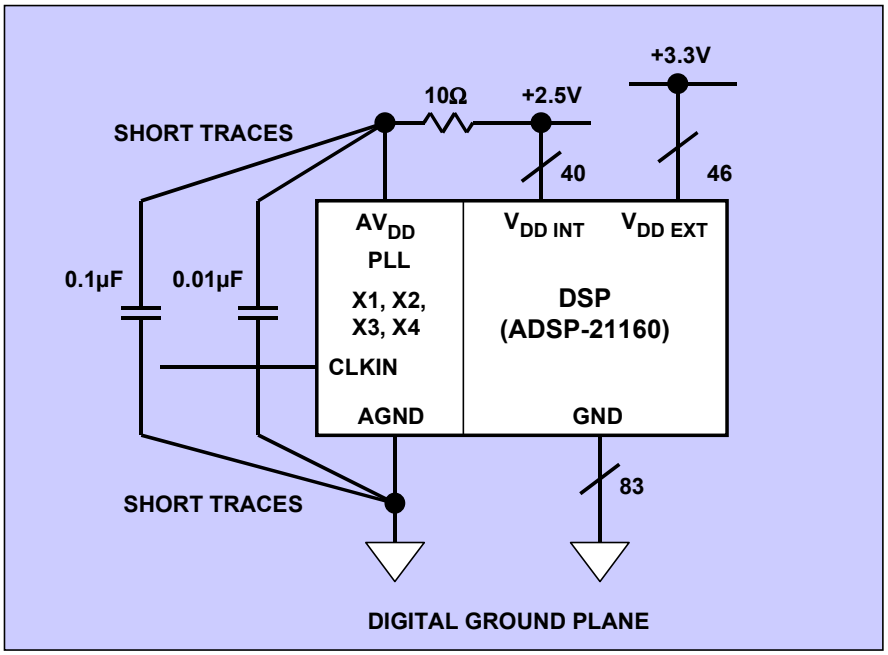

Figure 10.23

In order to prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled AV_{DD} and AGND, respectively. The AV_{DD} +2.5V supply should be derived from the $V_{DD\ INT}$ +2.5V supply using the filter network as shown. This ensures a relatively noise-free supply for the internal PLL. The AGND pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the AV_{DD} pin and AGND pin using short traces.

GROUNDING SUMMARY

There is no single grounding method which will guarantee optimum performance 100% of the time! This section has presented a number of possible options depending upon the characteristics of the particular mixed signal devices in question. It is helpful, however to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane! The initial board layout should provide for non-overlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs which have internal phase-locked-loops (PLLs), such as the ADSP-21160 SHARC. The ground pin for the PLL is labeled AGND, but should be connected directly to the digital ground plane for the DSP.

GROUNDING PHILOSOPHY SUMMARY

- **There is no single grounding method which is guaranteed to work 100% of the time!**
- **Different methods may or may not give the same levels of performance.**
- **At least one layer on each PC board MUST be dedicated to ground plane!**
- **Do initial layout with split analog and digital ground planes.**
- **Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes.**
- **Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane).**
- **Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board.**
- **Follow recommendations on mixed signal device data sheet.**

Figure 10.24

SOME GENERAL PC BOARD LAYOUT GUIDELINES FOR MIXED-SIGNAL SYSTEMS

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems. If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. Figure 10.25 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

ANALOG AND DIGITAL CIRCUITS SHOULD BE PARTITIONED ON PCB LAYOUT

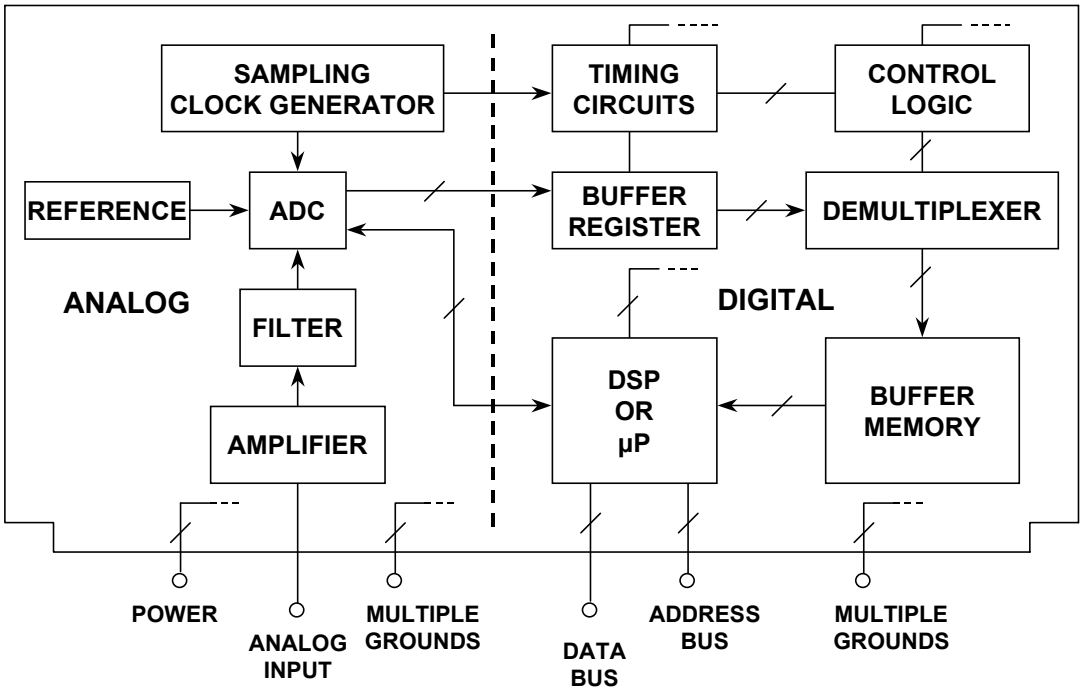

Figure 10.25

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel - it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10mΩ) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Manufacturers of high performance mixed-signal ICs like Analog Devices offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

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