Data-converter challenges in SOC design

As gate lengths shrink to deep-submicron dimensions, the promise of SOCs is becoming a reality.

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The building blocks of a generation of ICs are now major circuit elements, many of which would have been impressive stand-alone ICs a few years ago. Included on these new chips are such analog blocks as high-speed and high-resolution ADCs and DACs, PLLs, crystal oscillators, and active filters. Along with these analog circuits, deep-submicron CMOS technology allows the inclusion of major digital blocks, including digital processors, digital filters, RAMs, ROMs, and multimillion-gate blocks of random logic. Mixed-mode SOC (system-on-chip) designs cover a wide spectrum of applications, including areas as diverse as television, datacomm, fingerprint sensors, electronic games, electronic supermarket-shelf tags, and many others. The high-performance ADCs and DACs in these SOC designs present chip architects with unique challenges that they must overcome to achieve a short time to market.

Large SOC designs require a technical leader to design the IC. This person must be part system designer, part IC designer and will eventually need skills similar to those of circuit-board designers. No one person has all the technical skills to design an IC of this complexity. The technical leader, therefore, must deal with designers with different skills as well as with IP (intellectual-property) providers and IC foundries. This article presents the challenges you'll encounter when incorporating high-performance data converters into SOC designs and approaches to meeting those challenges.

Unique issues; unique solutions

In an ideal world, an SOC architect would pick an IC foundry that could meet his or her cost, schedule, and performance goals, then proceed to pick out the building blocks from an extensive catalog of available blocks already characterized in that fabrication process. With this approach, the chip designer would function much like a circuit-board designer who reads data sheets and selects components. Unfortunately, at this time, IC-fabrication advances often make processes outdated before a large library of data-converter components becomes available. Other ADC and DAC problems frustrate SOC architects. Often, designs require numerous analog blocks. If a designer is fortunate enough to find a DAC IP cell in the target process, the necessary ADC cell may be available only in another process or even in a different foundry. Because analog blocks do not directly port the way digital blocks do, designers are left with few choices. One option is to redesign the system using only the available data-converter blocks in the target process, thereby degrading system performance. Another option is for the architect to design a specific data-converter block in the target foundry to meet the size, power, and accuracy requirements. If the company developing the SOC does not have the required talent or resources available to design the block, it can contract with a services company that specializes in designing both SOC ICs and analog building blocks for SOC applications—data converters, for example.

In designing a new data-converter block for an SOC, an analog-block designer encounters a number of unique challenges that a digital designer would not face. First, he or she needs to assemble the matching information necessary to design the converter. If the design is in a CMOS process, this information will include matching information on PMOS and NMOS transistors as a function of transistor length and width, resistor-matching data, and capacitor-matching data. Many medium- and high-resolution ADCs use a pipelined switched-capacitor architecture. In many digital processes, the traditional poly capacitor is unavailable, because

the additional mask steps to add this component add too much cost to a design. It is now becoming more common for design houses to make capacitors out of the multiple layers of metal available in deep-submicron processes. Although these capacitors are less dense than poly capacitors, the multiple metal layers make this approach a cost-effective alternative. The main challenge a designer faces is deciding what size capacitor to choose for a given application. As a general rule, matching capacitors improve with the square root of area. This relationship holds until the area gets so large that gradient effects, due to oxide thickness gradients, start to dominate the matching. Proper layout techniques, such as common centroid and position scrambling, can further improve the linearity of capacitor DACs in pipeline ADCs.

ADC blocks

In a typical pipeline ADC, the capacitor DACs often limit the ADC accuracy (see **Figure 1** below). Therefore, using larger capacitors in the DACs improves accuracy. Larger capacitors are also helpful in reducing KT/C noise. Unfortunately, as capacitor size increases, the power of the subrange amplifier circuits in the ADC also increases, as does the circuit area that the capacitors take up. For this reason, you should choose the minimum capacitor size to meet both noise and accuracy requirements of the ADC. However, capacitor-matching information has been difficult to obtain from many foundries. You are even less likely to obtain matching data on metal-metal capacitors made from interconnect metal. The most reliable matching information comes from measuring the linearity of multiple ADCs and deriving data from the integral and differential linearity. From this data, you can determine random mismatching for the size capacitor you choose. You can then take this information to optimize future designs in a process. Regrettably, this approach practically assures that the first ADC designed in this manner will not have optimal power or accuracy. The long-term solution to this problem will occur only when fabrication houses characterize matching of capacitors built with interconnect metal. At least one IC foundry has solved this problem by including a special metal-metal capacitor, which uses a thin dielectric and is fully characterized for matching.

You can make some architecture trade-offs to improve your chance of success. In general, for a given total DAC capacitance in a pipeline ADC, you can obtain better differential linearity at the major subrange transitions by increasing the number of bits in the first stage. Assuming matching improves with the square root of area, each additional bit you add to the first stage improves differential linearity by a factor of the square root of two. The reason for this improvement is that even though each additional bit reduces the unit cell capacitance by a factor of two, the matching is only reduced by the square root of two. Because there are now twice as many unit cells, each unit cell represents half as many quanta, so differential linearity actually improves by the square root of two. Integral linearity however is relatively independent of the number of bits in the first stage of the pipeline ADC.

A Monte Carlo simulation calculates the expected integral nonlinearity and differential nonlinearity of a pipeline ADC for a given standard deviation of capacitor matching in the first-stage DAC. This simulation assumes ideal performance in the following stages. **Figure 2** below shows integral-nonlinearity results for a 10-bit pipeline ADC example, in which the first stage has a 4-bit quantizer and a DAC. In the simulation run, the standard deviation of unit-cell capacitance is assumed to be 0.2%. **Figure 3** below shows a Monte Carlo run of the differential-linearity errors expected at the major subrange transitions.

Another approach in SOC ADC design is to choose a folding-ADC architecture over a pipeline approach. The advantage of a folding ADC is that its accuracy is based on resistor and transistor matching instead of capacitor matching. **Figure 4** below shows a generalized block diagram of a typical folding architecture. When designing a folding ADC in deep-submicron processes, you must be careful during layout so that antenna effects do not degrade matching of the transistors used in the interpolation, folding, and comparator stages.

You can prevent this degradation by ensuring that all gates of the transistors that must match are tied directly with metal to a drain or source or to a diode connected to the substrate. By making this connection, you can prevent excess charge from building up on the gates during processing, which can greatly degrade transistor-threshold matching.

In any ADC architecture, the chip designer must take great care to ensure that the clock reaching the ADC has jitter low enough for the application. The SNR of a sampling system is limited by aperture jitter to be no better than $1/(2*\pi*f*\tau)$, where f is the input frequency to the ADC in hertz, and τ is the aperture jitter in seconds rms. In systems in which the ADC is doing super Nyquist sampling, the high input frequencies involved can easily cause aperture jitter to be the limiting factor in the system. The chip designer must treat the ADC clock as an analog signal. If low jitter is required, any circuitry the clock passes through should be powered from a clean analog supply. If the clock is run through a gate that is powered from a noisy digital supply, the variation in supply voltage will modulate the propagation delay of the gate causing aperture jitter. If the gate is instead tied to the analog supply, the power-supply rejection of the ADC will attenuate any clock noise that gets on the analog supply, and the sampling function of the ADC will alias the clock frequency to dc. In many system designs, subsequent processing removes dc offset of the ADC, so this clock coupling to the analog supply will not affect system performance.

A necessary practice in keeping noise out of SOC ADCs is the careful positioning of aperture time of the S/H clock so that the clock strobe is inactive when data is changing in the digital sections of the IC. This limitation means that for high-dynamic-range systems, the digital circuitry cannot have sections of circuitry running asynchronously with the S/H clock. It is possible to have sections of digital circuitry running at multiples of the ADC clock as long as the digital clocking scheme does not allow data transitions at the aperture time.

High-speed-DAC block design

Another type of block that SOC designs commonly require is a high-speed DAC. The most common architecture is a highly segmented current DAC in which the output current is used differentially to reduce noise pickup on chip. Current sources in the DAC are laid out using pseudorandom common centroid patterns to reduce the effects of gradients. This DAC architecture needs no matched capacitors but does require that the transistors in the process be characterized for current-source matching. This process information is usually available from the foundry. DACs of 10-bit resolution performing 1G-sample/sec conversions have been fabricated (**Reference 1**).

In some situations, DACs are fabricated using switched capacitor approaches. A 12-bit, 22-MHz DAC for a VDSL application is described in (**Reference 2**). It uses a switched-capacitor approach. Switched-capacitor and ADC-capacitor approaches raise the same issues of capacitor matching.

As with the ADC blocks, high-speed DACs also often require the clock to have low jitter. So, as with the ADC, you should treat the clock as an analog signal. Also, you need to lay out both the ADC and the DAC in a manner that minimizes noise pickup from the substrate. Common noise-reduction techniques include guard rings, isolation wells, tying the substrate in the analog section with multiple taps to a quiet ground, and as much physical separation between the analog blocks and the noisy digital sections as practical. Analog circuitry should be differential, and you should lay it out in a symmetrical pattern where possible to cancel noise pickup from the substrate. Sometimes you can tie the substrate in the digital circuitry to a separate quiet ground to avoid connecting the noisy digital ground to the substrate. Often, however, the digital library employed does not permit the use of a separate ground for substrate ties, or the extra ground pin is unavailable.

Test and characterization circuitry

Test and characterization circuitry must be designed into the SOC to allow for evaluation of ADC and DAC blocks. For characterization, it is desirable to have access to the digital outputs of the ADC and the digital inputs of the DAC. You can often multiplex these digital signals with other digital inputs entering or leaving a chip. In a similar manner, you can often design the S/H clock of an ADC with an alternate set of input switches to allow sampling of an auxiliary set of test inputs. If it is desirable to monitor interior nodes in the ADC or DAC, you can use a dedicated analog test bus that runs through multiple analog blocks. Select lines are used during testing to select which internal nodes are to be switched to the test bus. When the analog test bus is not in use, you should switch it to ground to reduce the possibility of noise coupling. Typical nodes that an analog test bus in a pipeline ADC might sample include the S/H input and output, subrange amplifier outputs, internal reference voltages, internal power and grounds, and replicas of reference currents. It is desirable to run a positive and negative test bus together to allow for simultaneous viewing of differential signals. When problems arise, the ability to quickly probe internal nodes greatly speeds SOC debugging and improves time to market. Once a block is fully characterized and the block is in use, you can configure the analog test bus to always select ground. Or, you can even remove it.

Recent advances in SOC technology hold great promise for shrinking systems and their costs, but they also hold new challenges for designers. You cannot design analog blocks, such as ADCs and DACs, using the same strategies as full-chip implementations. Design teams must represent a variety of talents for them to achieve time-to-market goals.

References

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2. Sands, Nicholas P, Eric Naviasky, William Evans, Martin Mengele, Kevin Faison, Craig Frost, Michael Casas, and Michelle Williams, “An Integrated Analog Front-end for VDSL,” 1999 IEEE ISSCC Digest of Technical Papers, February 1999, San Francisco, pg 246 to 247.

Author biography

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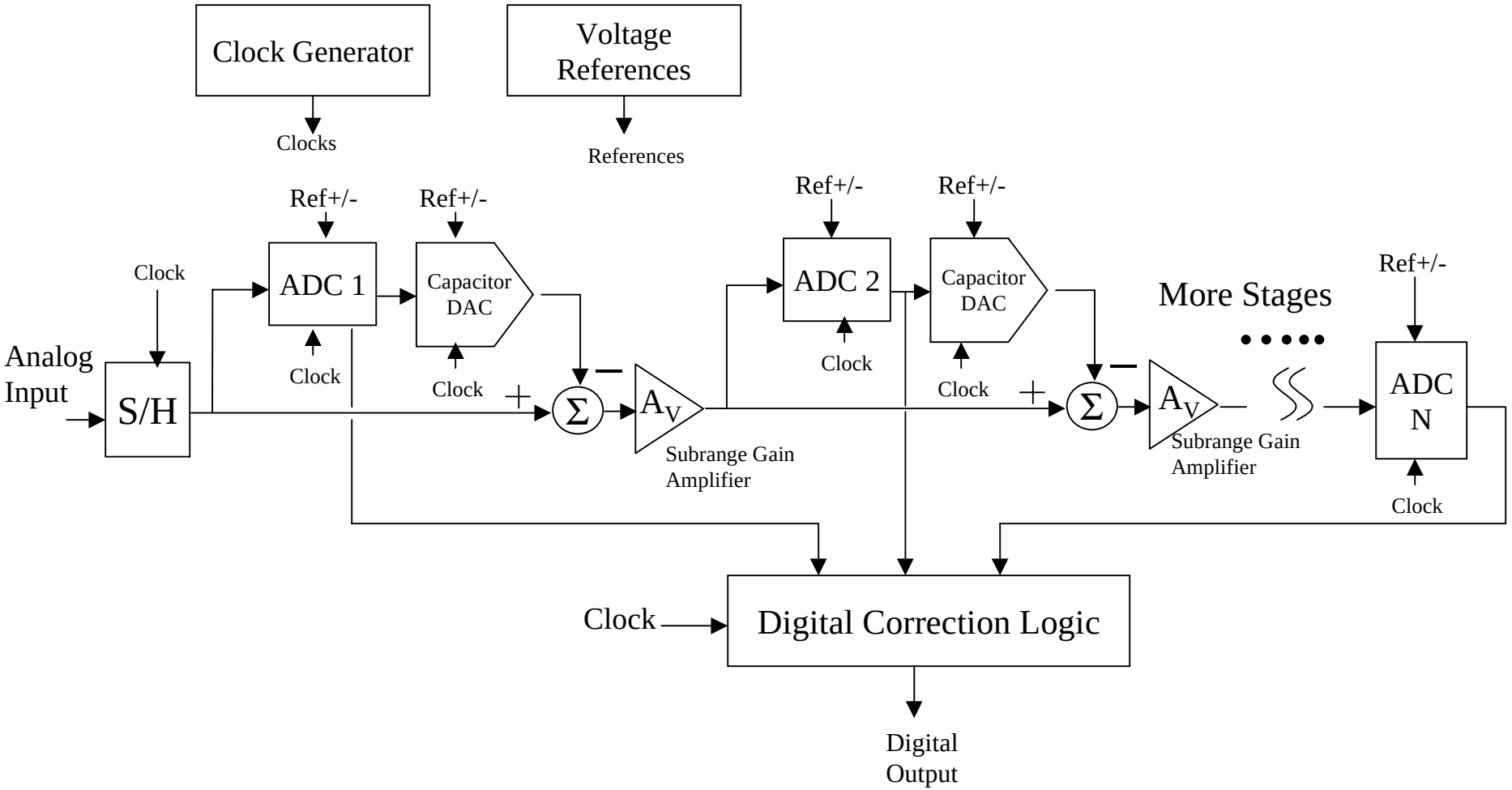

Figure 1--Pipeline ADC Block Diagram

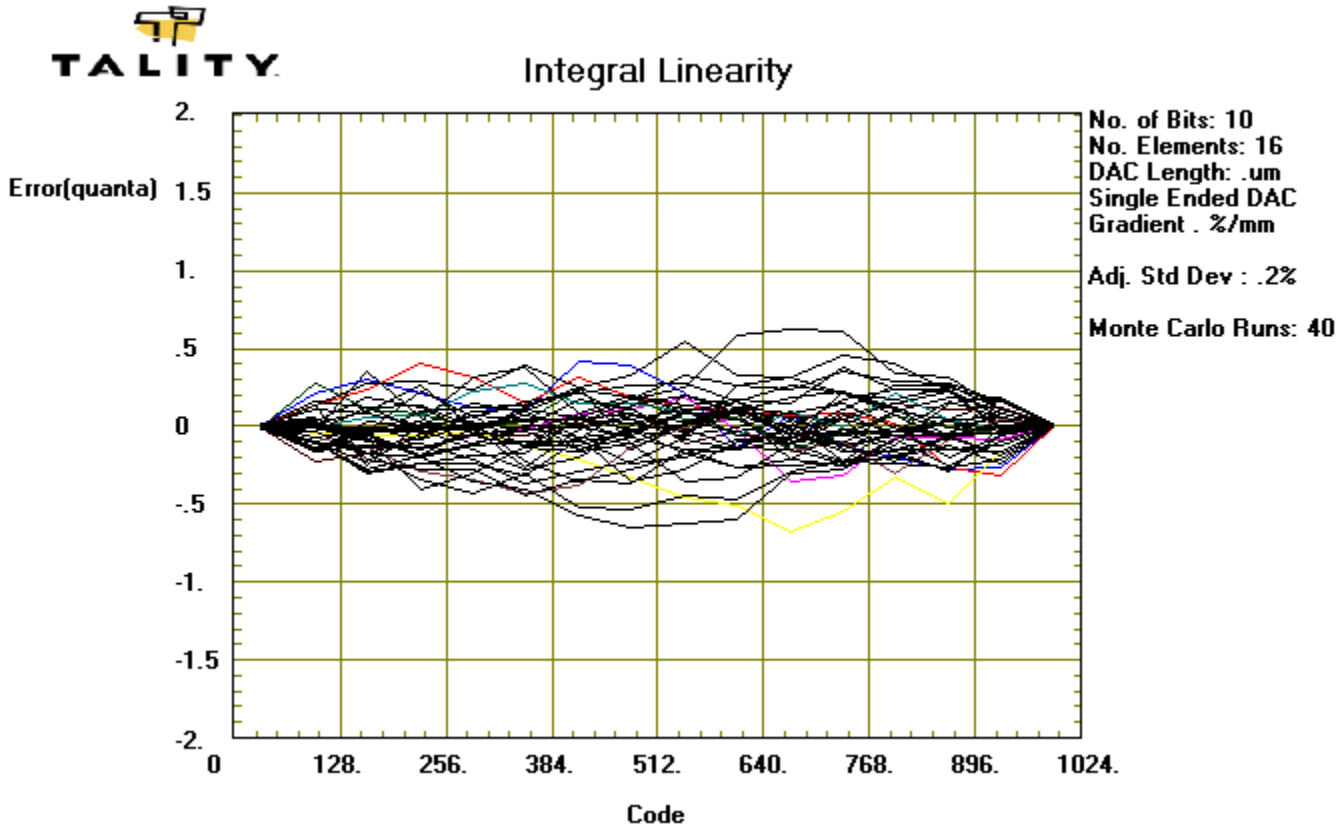
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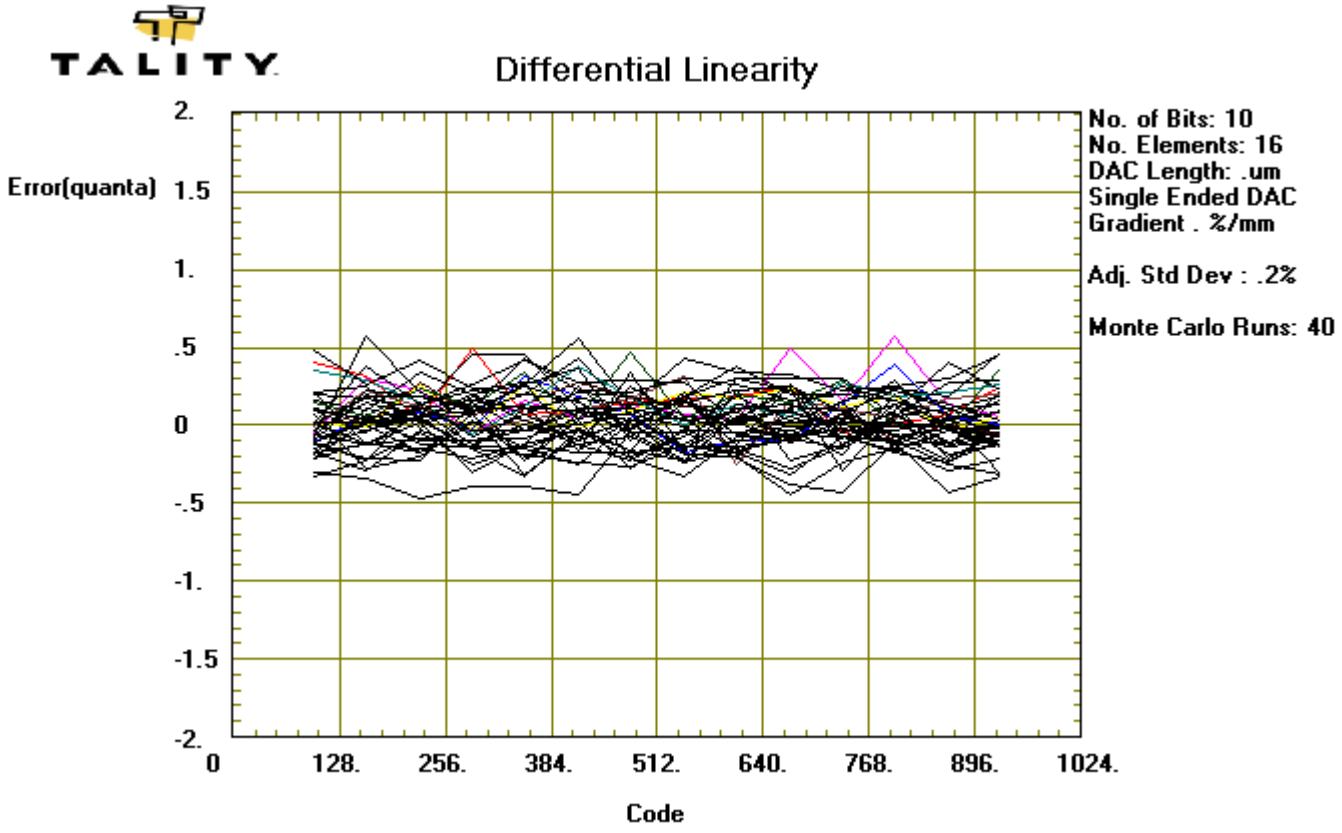
Figure 2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Code
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Figure 3

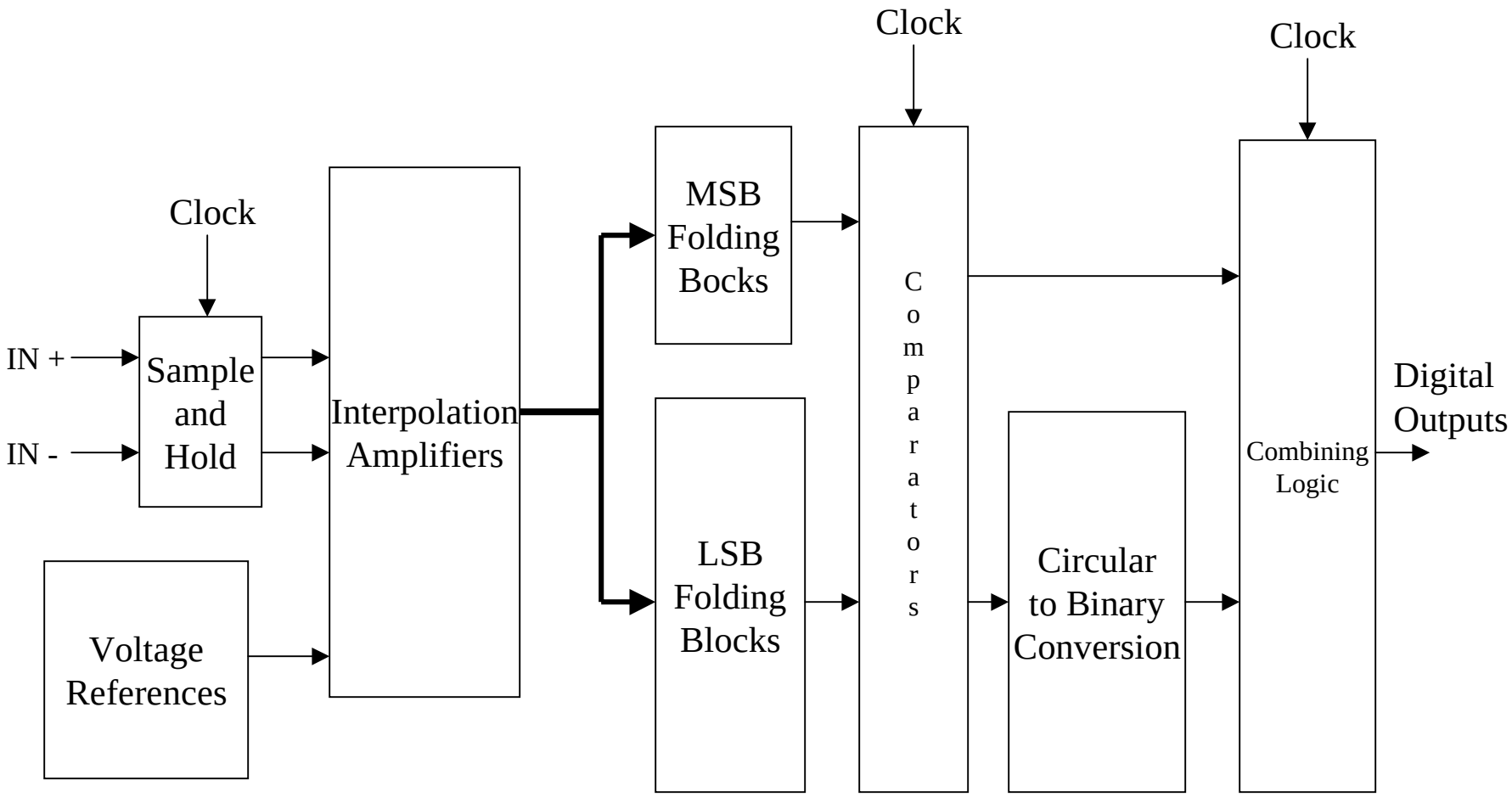

Figure 4--Typical Folding ADC Block Diagram