High-speed ADC techniques
- overview and scaling issues -

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Outline

- High-Speed ADC applications
- Basic ADC performance metrics
- Architectures – overview
- ADCs in 90s
- Limiting factors
- Conclusion

High-speed ADC applications

- Wireless LAN Data Channel (1-50MS/s, 6-10b)
- Magnetic Storage Read Channel (200-1000MS/s, 6-8b)
- ADSL data channel (3-10MS/s, 12-16b)
- Digital Multi-Standard TV Baseband ADC (20MS/s, 8-10b)
- CATV Decoder Modem ADC (10-20MS/s, 8-10b)
- HDTV – various apps (50-75MS/s, 10b)
- Digital-IF for Multi-standard Broadcast TV rcvr (100-200Mb/s, 8-12b)
- Serial high-speed links with MPAM modulation (5-10Gs/s, 4-6b)

Basic ADC performance metrics

- **Aperture time uncertainty**
- **Peak SNR**

SNRp=6.02N+1.76 [dB]

- **Effective # of bits**

SNDR=6.02ENOB+1.76[dB]

- **Dynamic range**

$DR=P_{full\ scale\ sin}/P_{sin@0dB\ SNR}$

- **Spurious Free Dynamic Range**

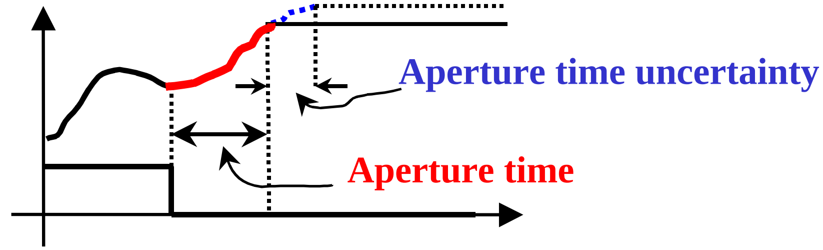
- **Static errors:**

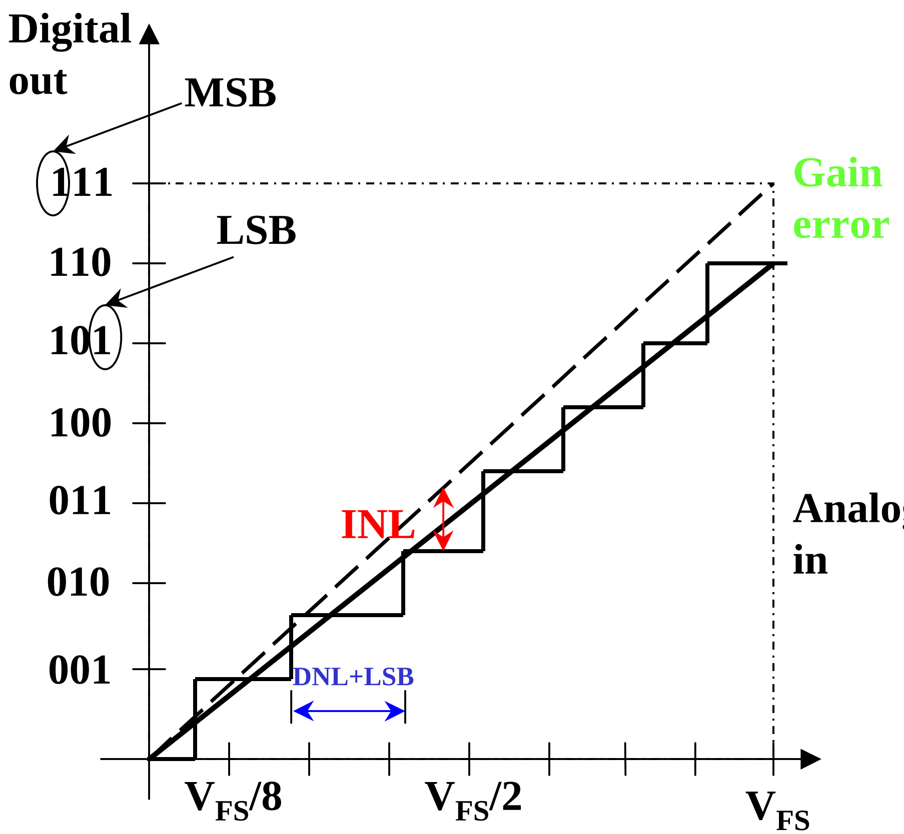
DNL - differential non-linearity

INL - integral non-linearity

Offset

Gain error





Architectures

- Flash
  - Interpolation
  - Averaging
- Folding
  - Folding and Interpolation
- Two-step
  - Subranging
  - Flash
- Pipeline
  - Per-stage calibration

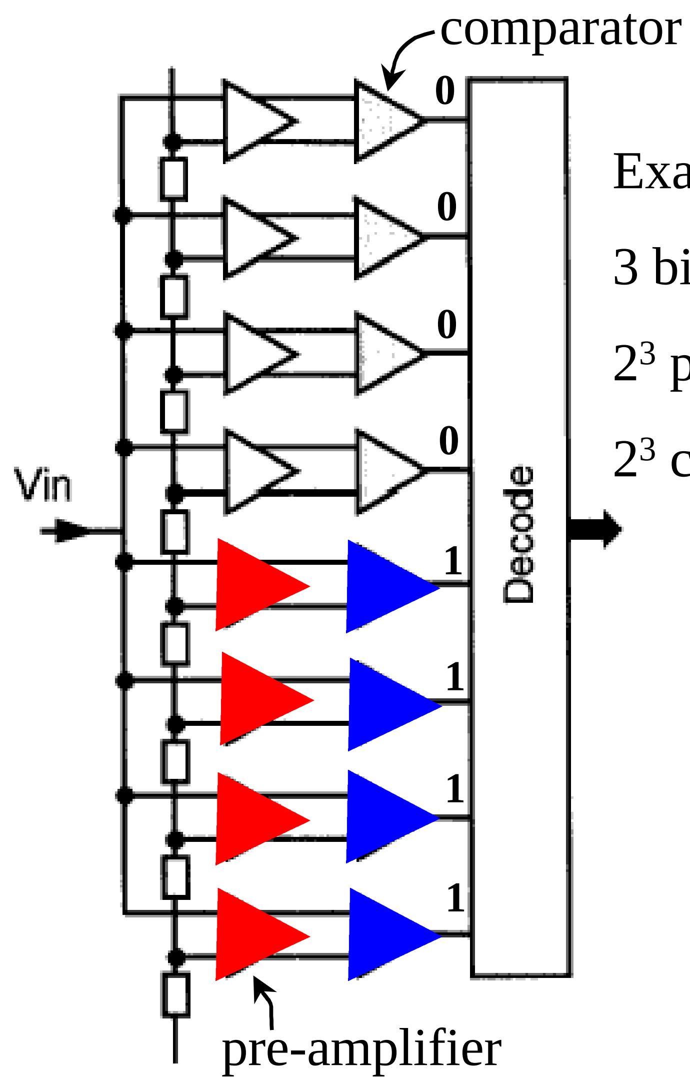
Flash ADC

Best up to 8 bits:

+ Speed

+ Simplicity

- Exponential complexity
- Big input capacitance
- Bubbles in thermo code
- Power
- Difference in signal delay to each comparator



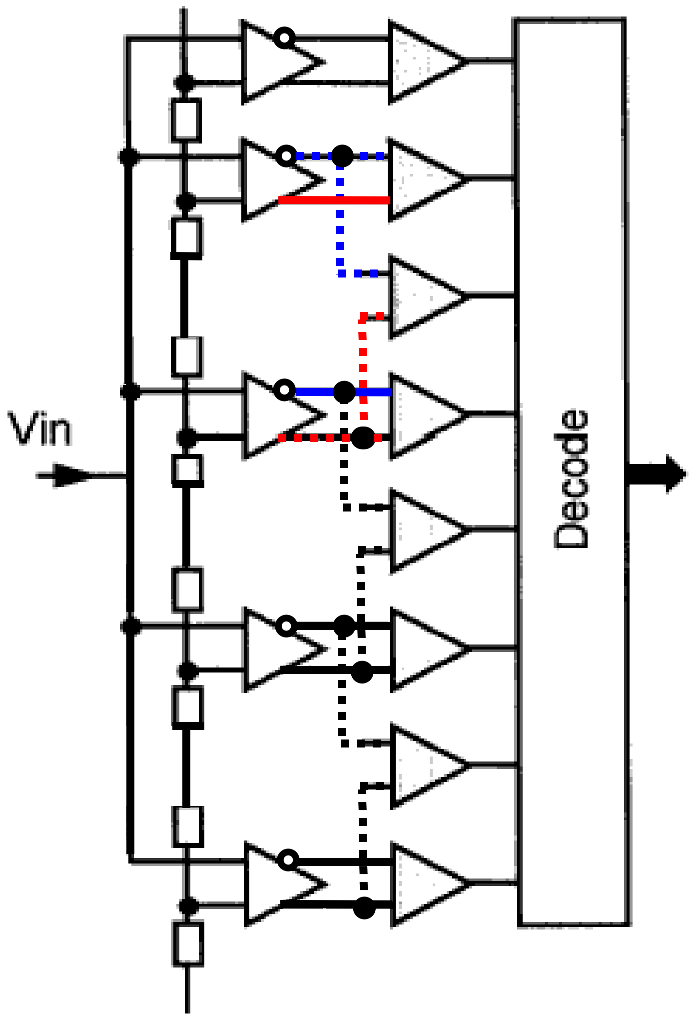
Example:

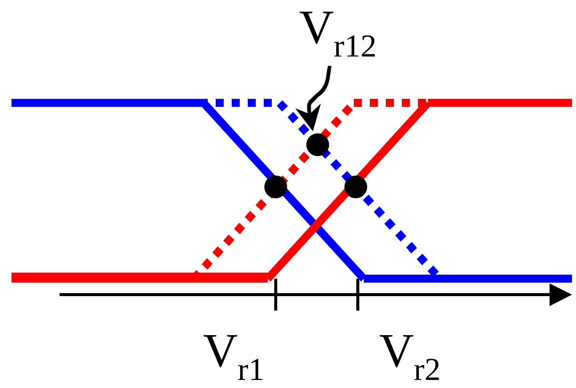
3 bit Flash ADC

2^3 pre-amplifiers

2^3 comparators

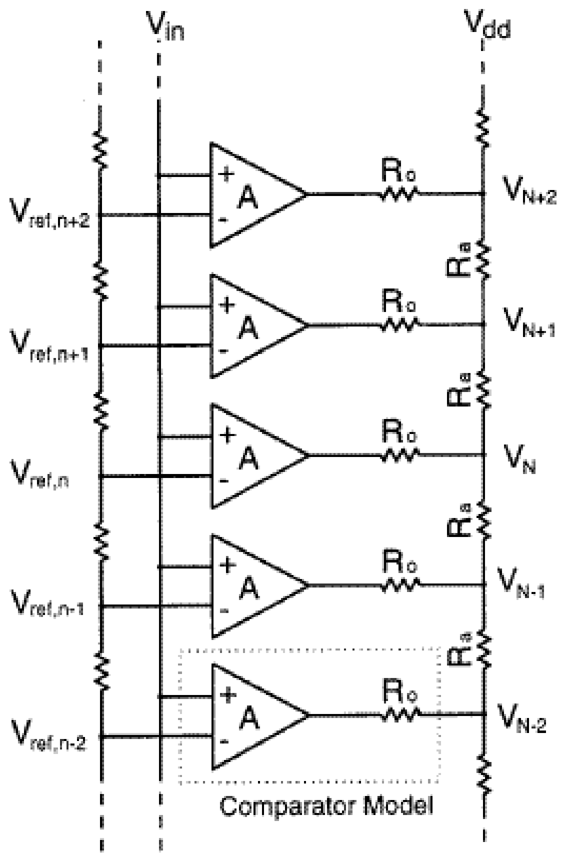
Interpolation in Flash ADC

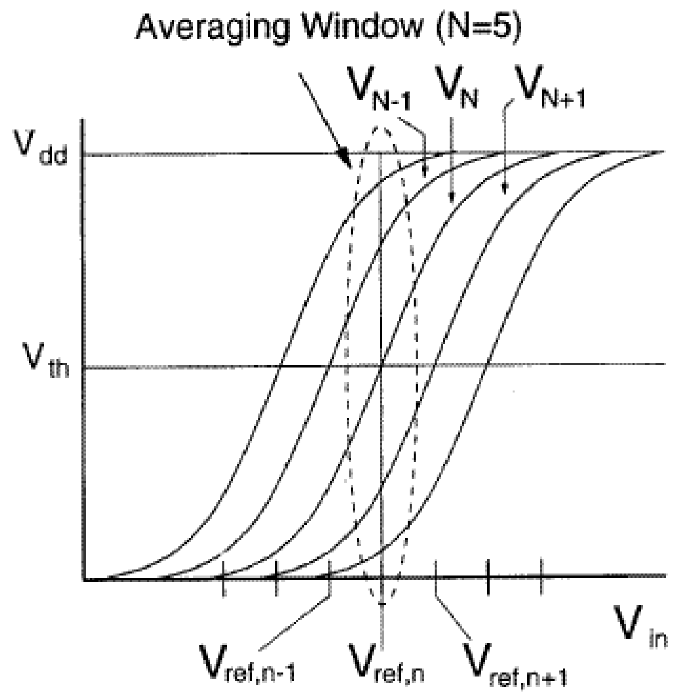




- Reduced # of pre-amps
  - smaller input capacitance
  - less power than full flash
- Improved DNL due to distribution of errors

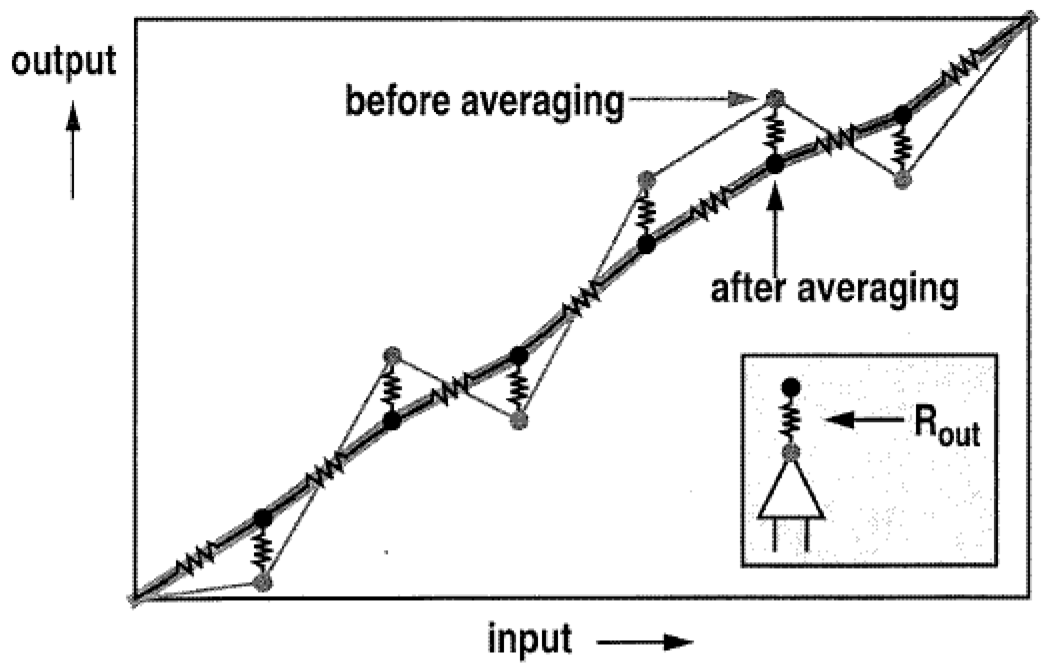
Averaging in Flash ADC





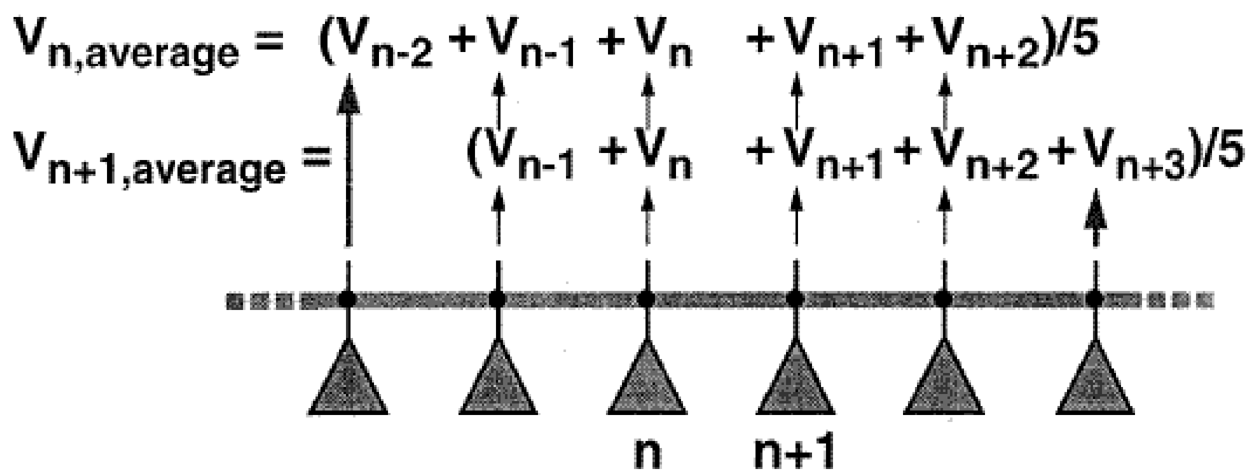
Pre-amps reduce effect of comparator offset (~ 15-50mV)
But introduce offsets (~3mV-10mV)
Solution – Average out the pre-amplifier offsets with resistor network

Effect of Averaging



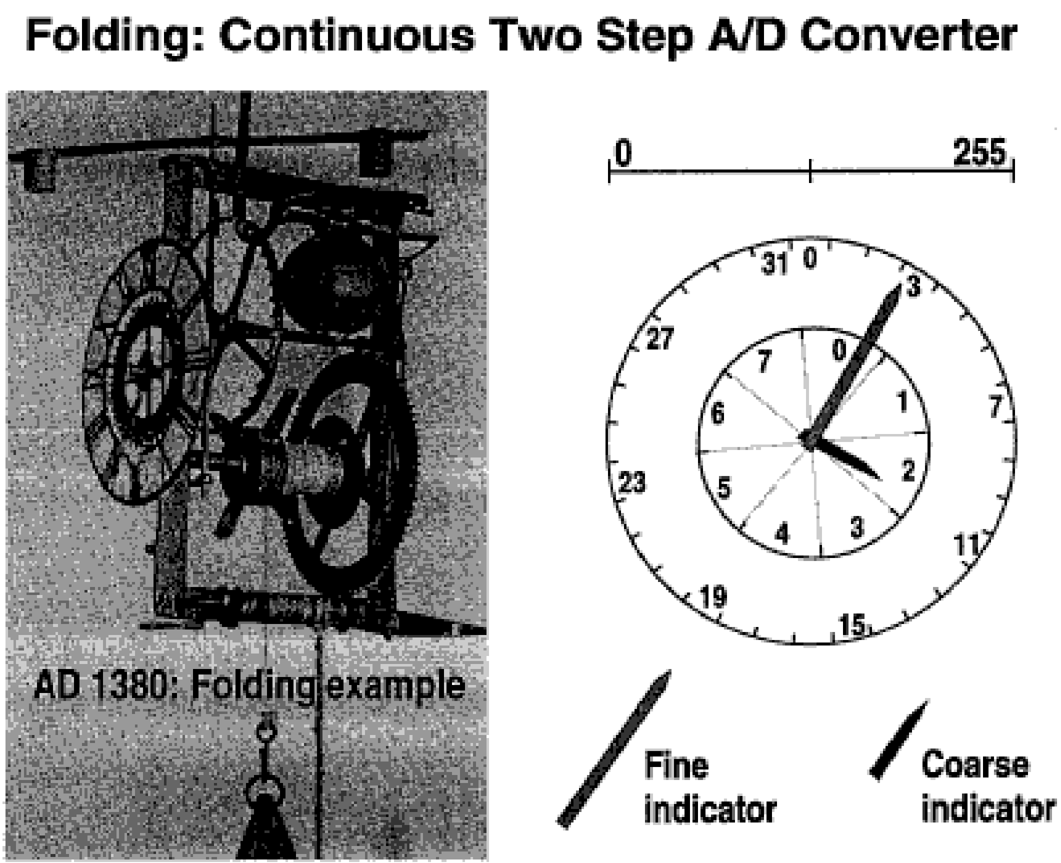
- averaging pulls amplifier outputs on to straight line
- amplifier output impedance must be high !

Averaging effect on offset, INL, DNL



- neighboring signals highly correlated after averaging
- $\Delta=(V_{n-2}-V_{n+3})/5$ and $s_{average} = \frac{s_{individual}}{\sqrt{5}}$
-
- DNL improves with # of averaging stages
- INL, offset improve with square-root of averaging stages

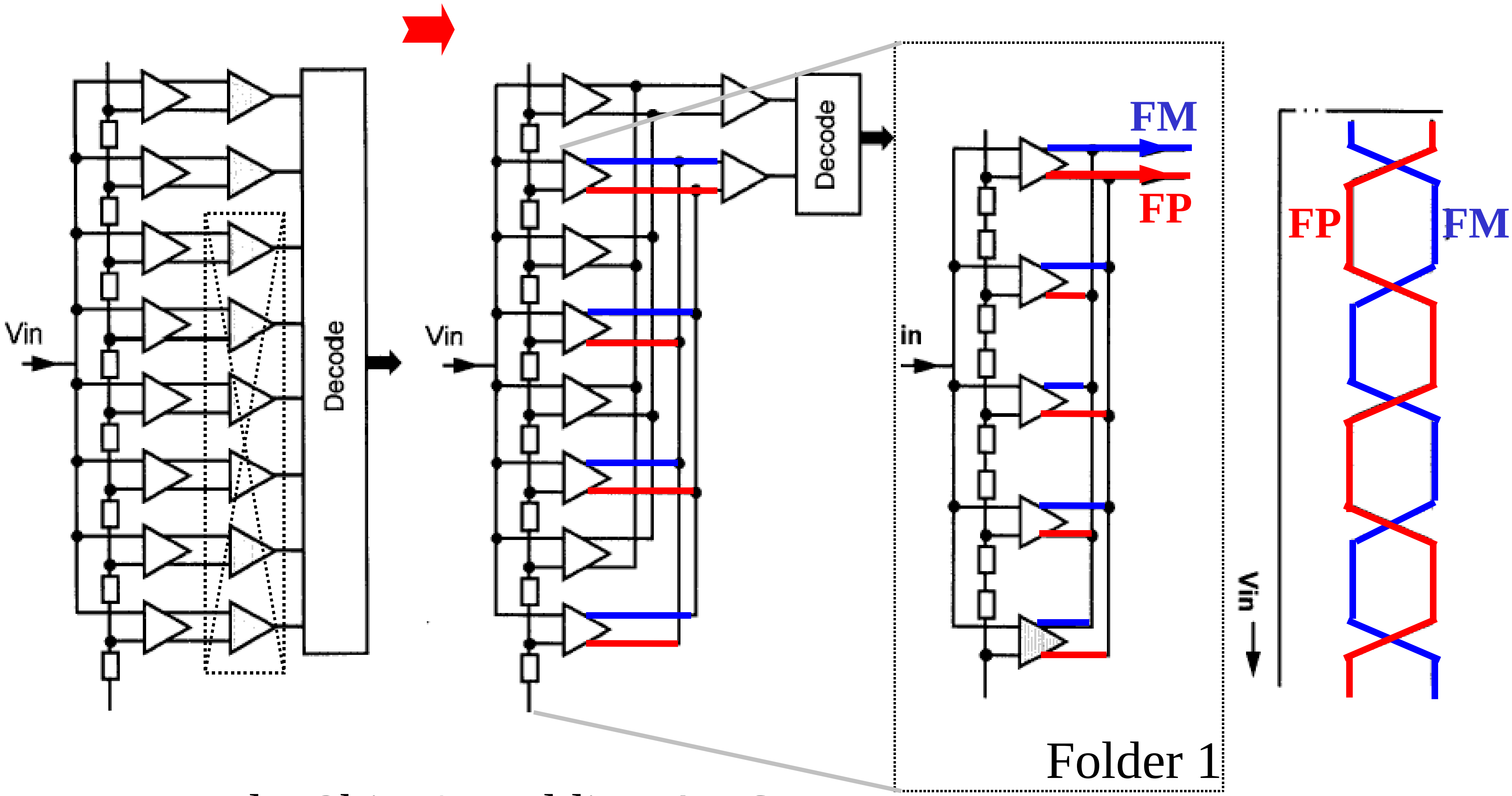
Folding and Two-step ADCs



Two architectures, same idea:
- Folding
- Two-step

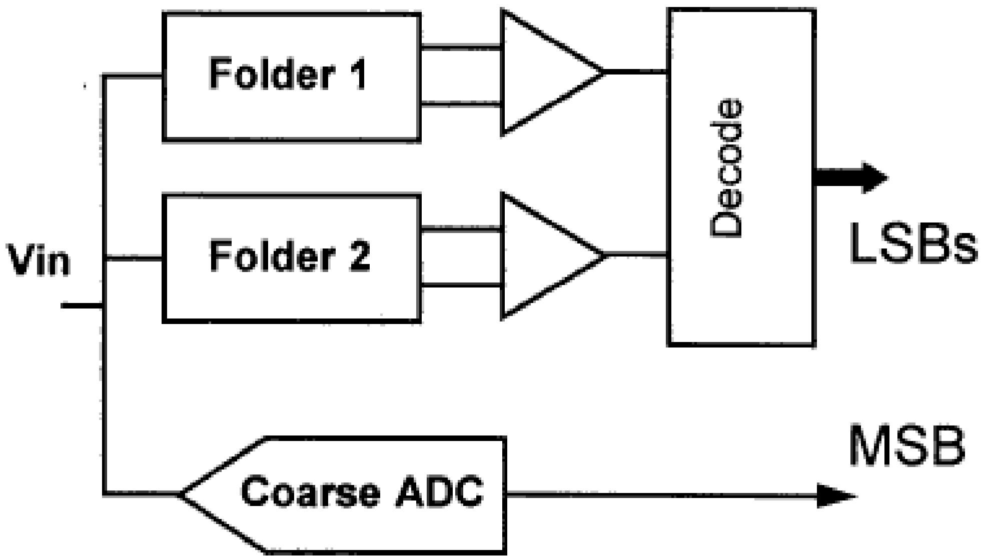
- Coarse ADC gets MSBs and residue
- Fine ADCs get LSBs from residue

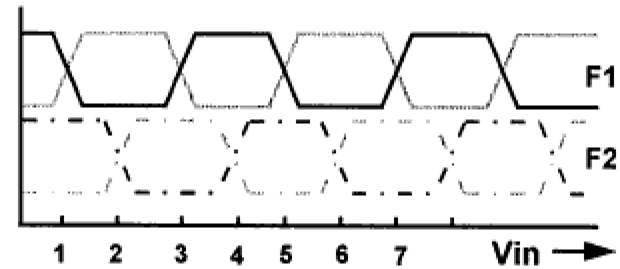
Folding ADC



Example: 3bit, 4x Folding ADC

Folding ADC: Block Diagram





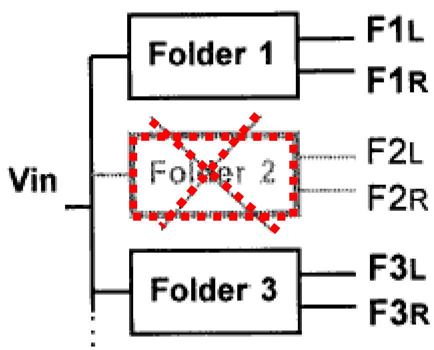
- Folding tradeoff
  + Fewer comparators
  - Faster signals

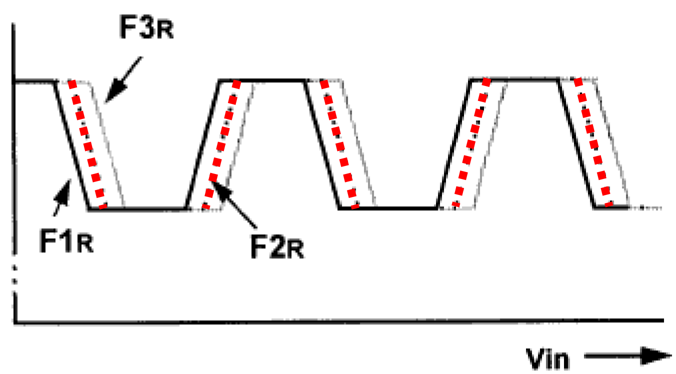
- Fold x 4
  + From 8 to 2 comparators
  - max. Fout > 4 Fin

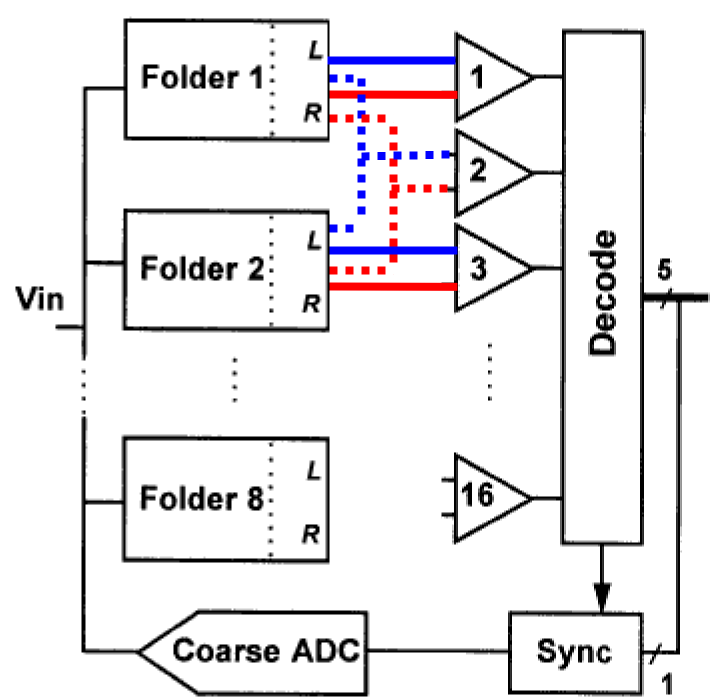
- Critical issue is to match timing of coarse ADC and fine (folded) ADCs
- Non-linearity around the folding point significantly reduces performance if amplitude is quantized

Folding & Interpolating ADC

Example: 6bit, 4x fold, 2x interpolate ADC







With interpolation – only detect zero crossing points

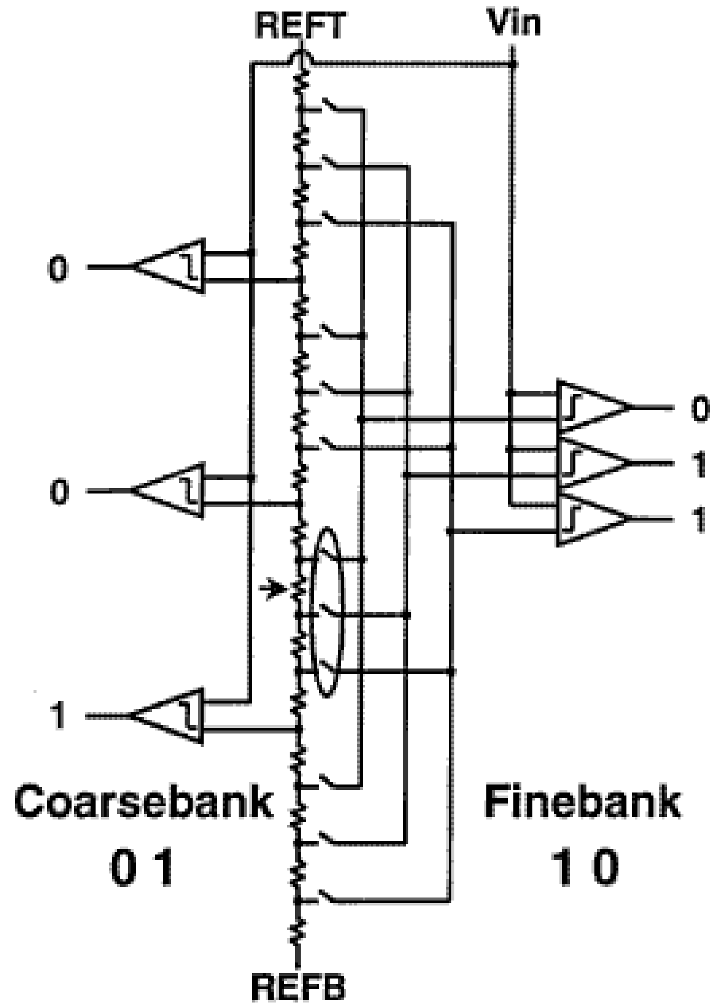
Two-step: subranging ADC

+ $2(2^{N/2}-1)$ comparators

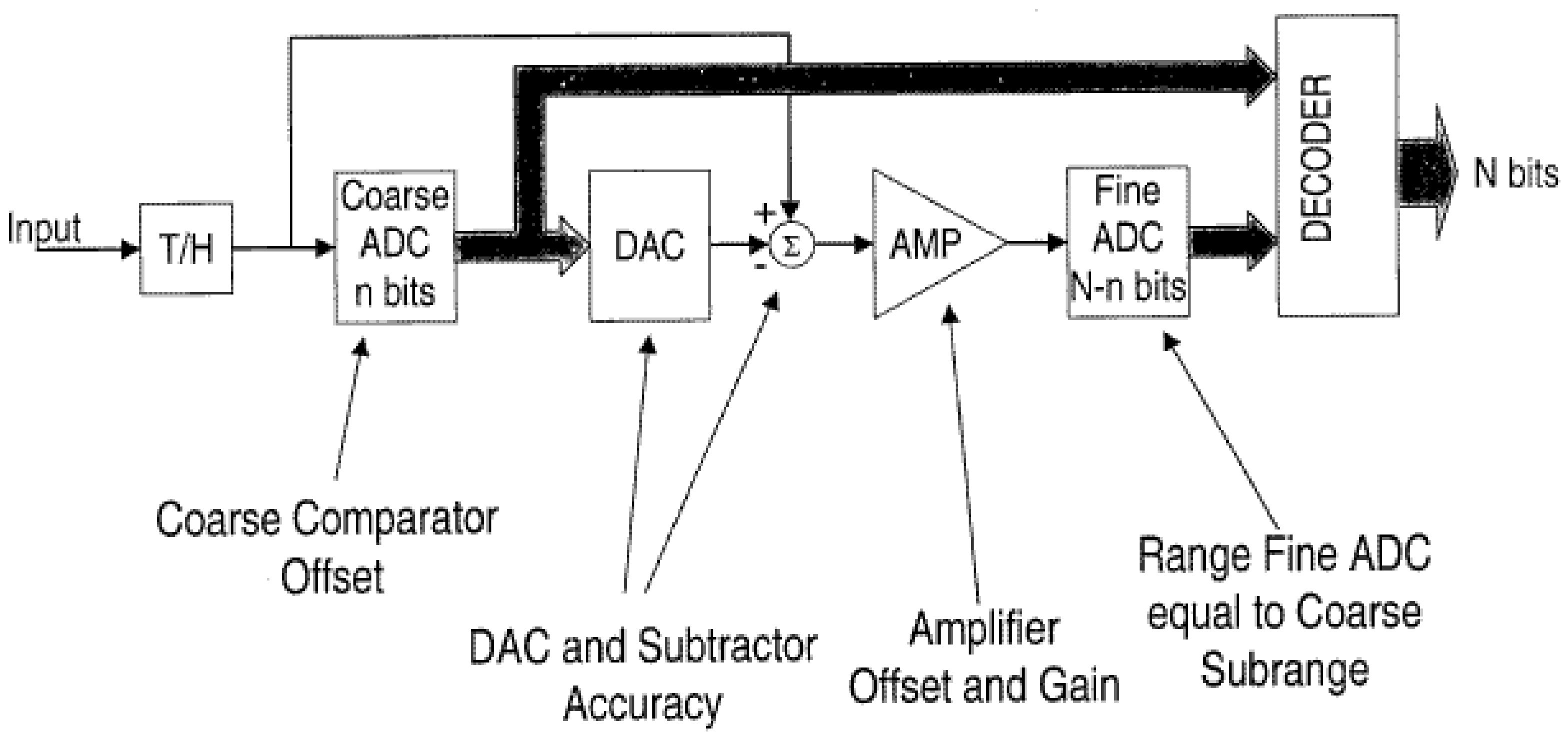
  Coarse bank selects which part of reference ladder to connect to fine bank

- Speed limited by settling of fine references

  parasitic capacitance from > 2^N switches + large kickback

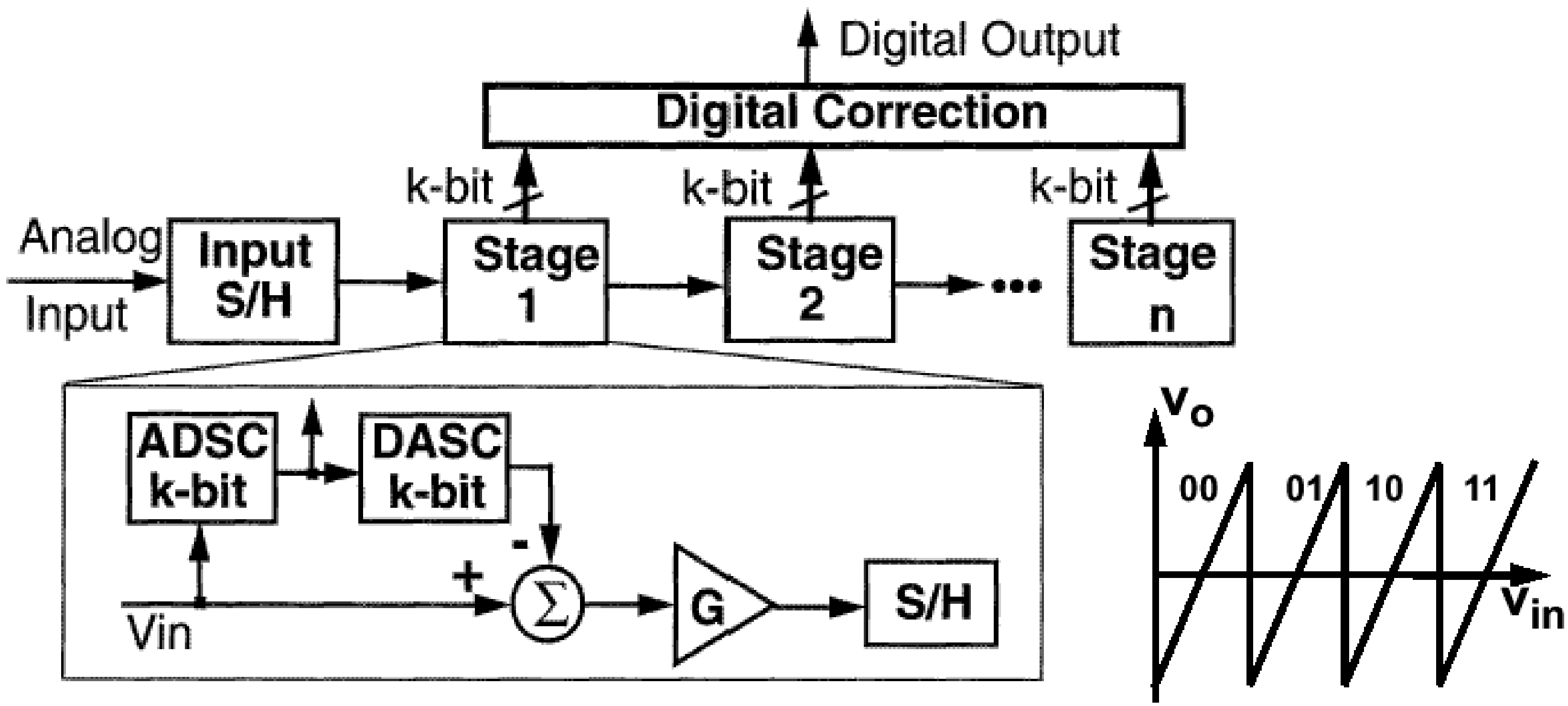


Two-step: Flash ADC



- Two-step ADC accuracy challenges

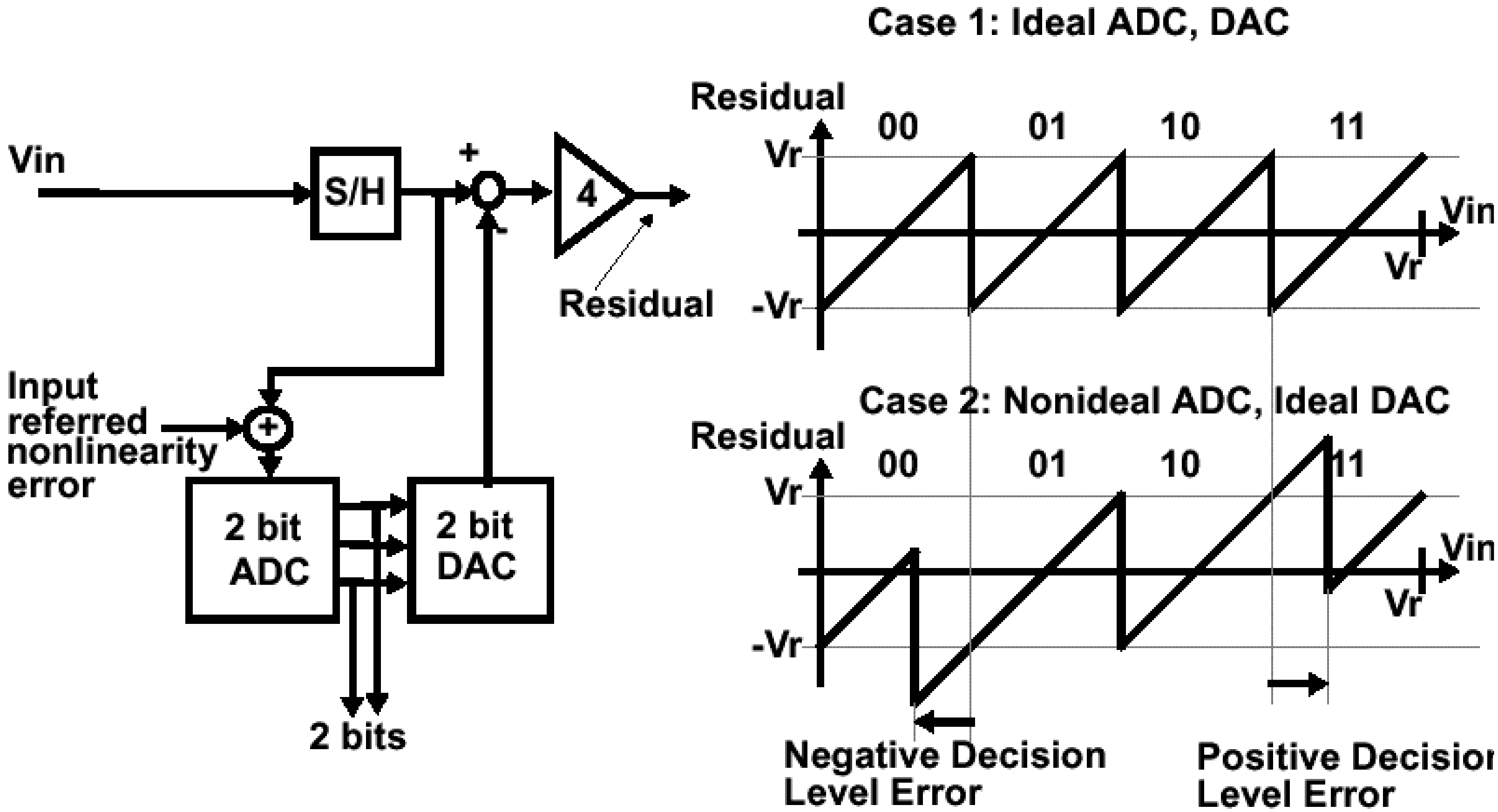
Pipelined ADC



- All stages process different data simultaneously
  - throughput only depends on speed of each stage
  - complexity traded for latency

Effect of stageADC non-linearity errors

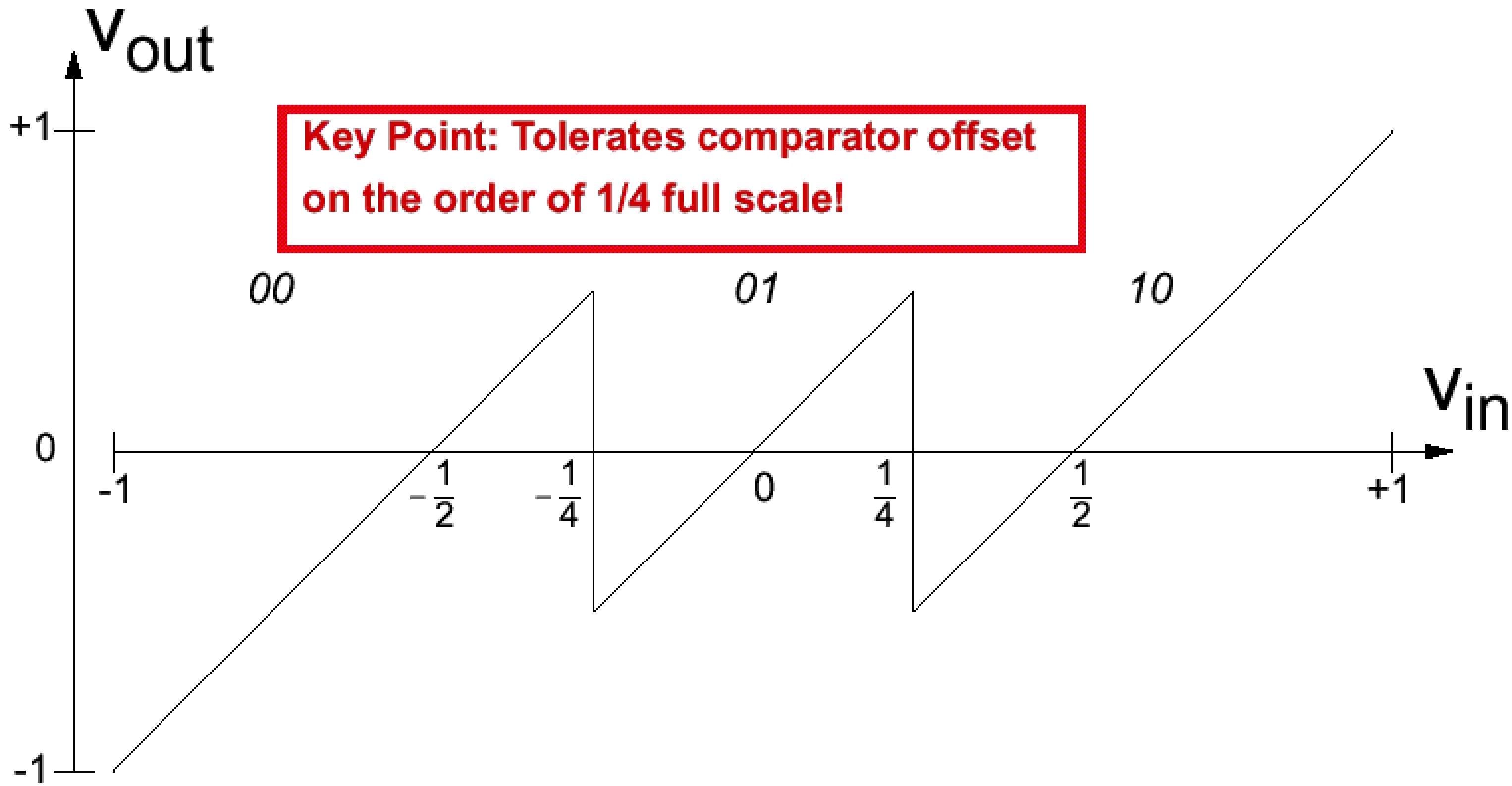
2-bit example:



Key Point: Can remove ADC Errors by Increasing ADC range in next stg

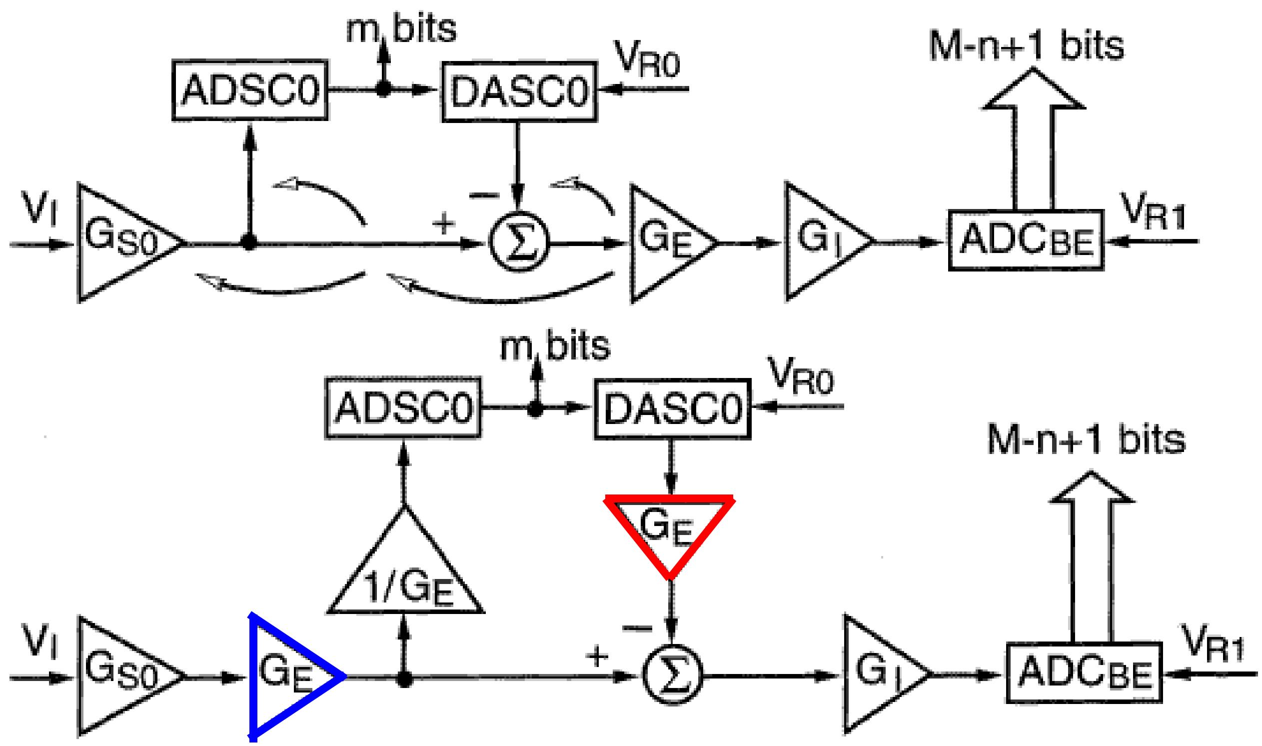
Removing stageADC non-linearity errors

Important Case: 1.5 bit/Stage with Digital Correction



Final Result: DAC Linearity and amplifier gain errors ultimately limit linearity

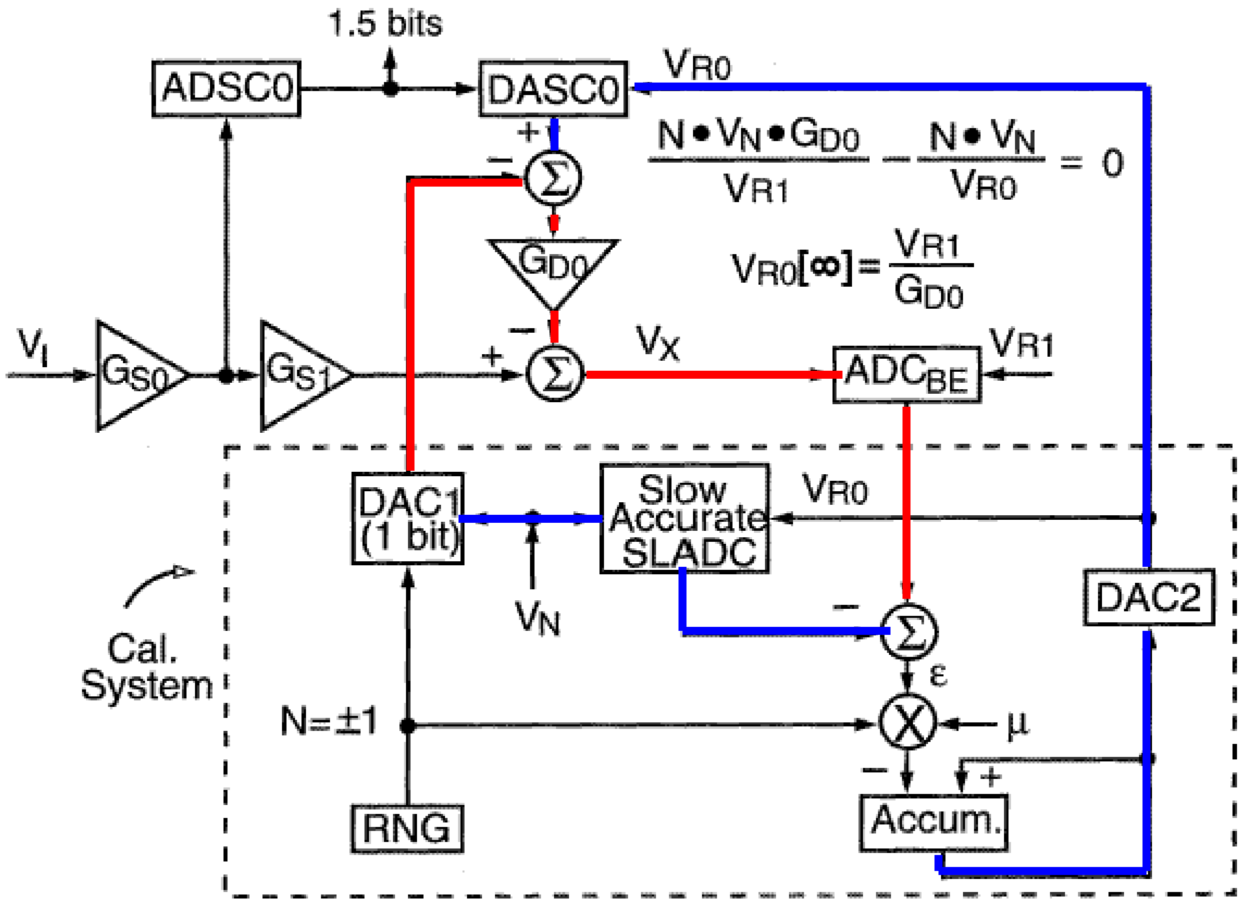
Interstage gain error propagation



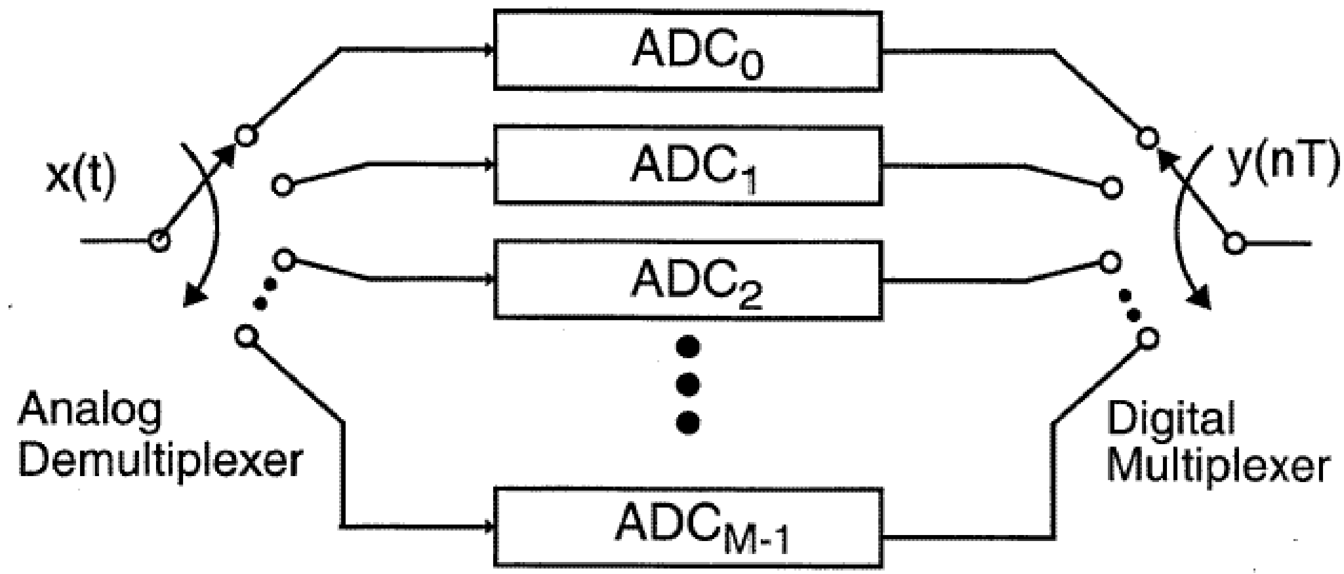
G_E models interstage gain error

Only need to correct for the red block in each stage !

Interstage gain error calibration



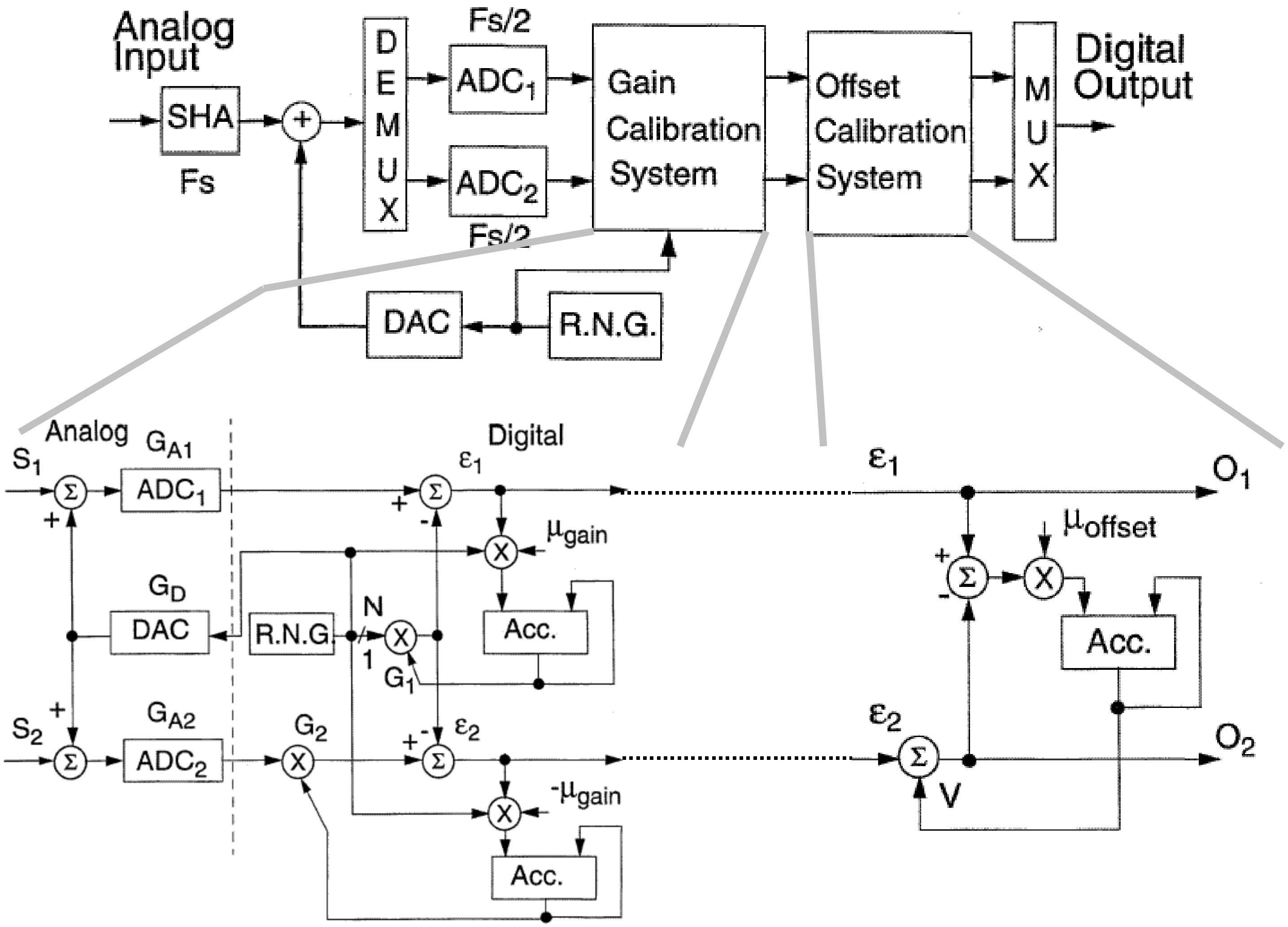
Time-Interleaved, pipelined ADCs



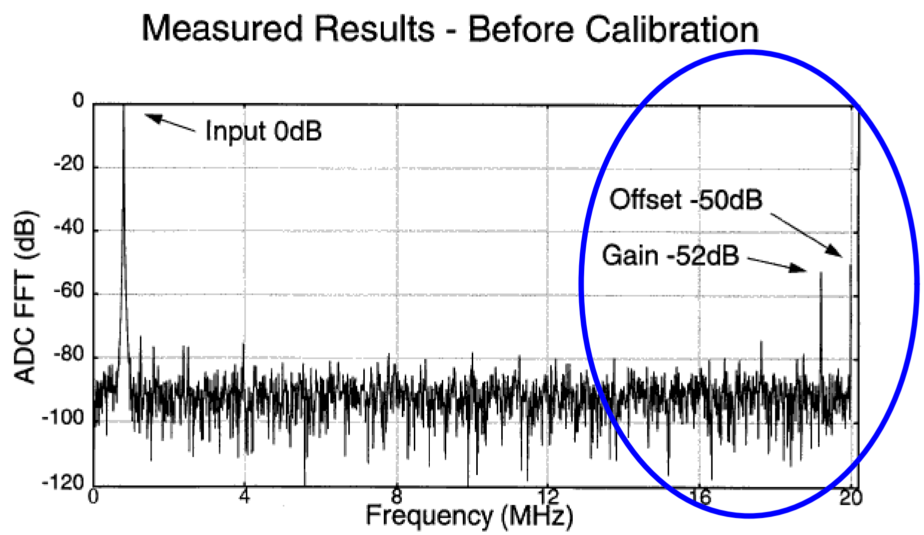
- Clock each ADC at F_s/M
- Increase throughput and area M times

Gain mismatch => Amplitude Modulation
Offset mismatch => Additive Tones
Timing mismatch => Phase modulation

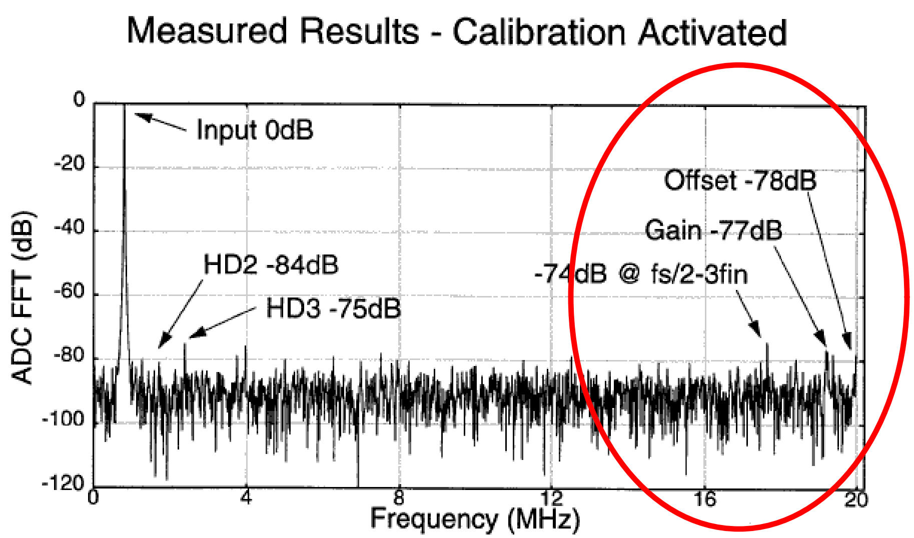
Gain and offset calibration



Calibration results



SNDR limited by mismatches



SNDR limited by non-linear mismatches

ADCs in ’90s

- Analyzed a bunch of ADCs
  - different technologies
  - different specs

  } How to compare?
- Use metrics from digital domain to see how ADCs scale with mainstream digital CMOS
- Two main metrics:
  - Delay of fan-out of 4 inverter (FO4)
  - Energy dissipated driving the gate of minimum size inverter (MSI)

Metrics …

- Unit Delay

$$FO4 = \frac{500\,ps}{mm} L_{ch}[mm]$$

- Unit Energy

$$Cg_{MSI} = (4+8)\,l\,\frac{2\,fF}{mm} = \frac{12\,fF}{mm} L_{ch}[mm]$$

$$MSI = \frac{6\,fF}{mm} L_{ch}[mm] \times Vdd^2$$

- Approach:
  - Normalize sampling period to FO4
  - Energy/sample=Power/Rate
  - Normalize Energy/sample by MSI
  - ED=normalized Energy * normalized Sampling period
  - Figure of merit FM~ Resolution*ln2 – ln(ED)

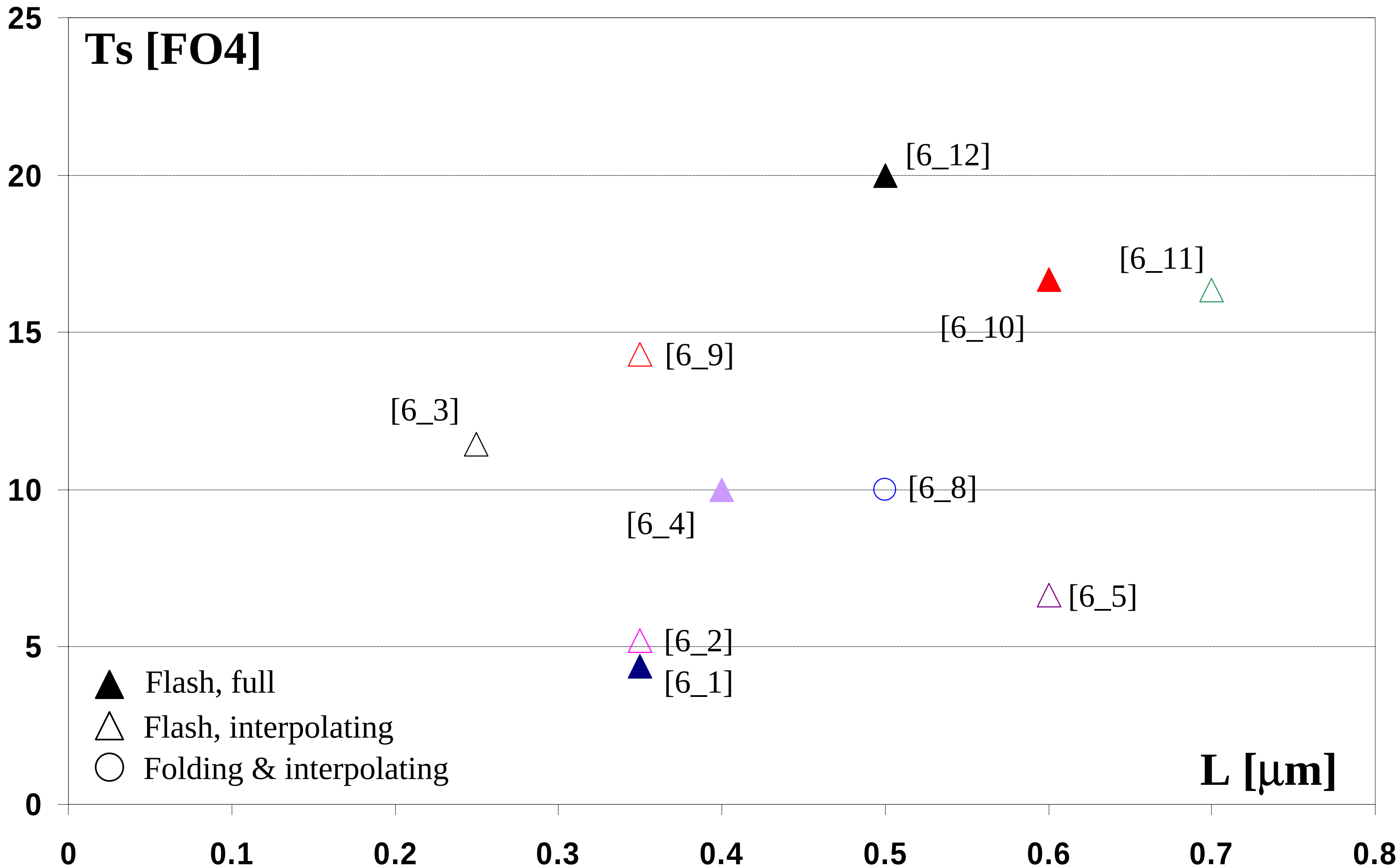
ADCs in '90s: Raw data

Author	Conf/Jour.	Resolution	peed [MS/	Tech. [um]	P [mW]	Vdd [V]	A [mm2]	INL [LSB]	DNL [LSB]	ENOB	SNDR	SFDR	Cin [fF]	Style
M. Choi	ISSCC 01	6	1300	0.35	250	3.3	0.8	0.35	0.2	5	32	44	1	Full-Flash with preamp & two stage averaging
G. Geelen	ISSCC 01	6	1100	0.35	300	3.3	0.35	0.6	0.7	4.5	29	40		Flash, 3 avg, 2 interpolate, distrib T/H
K. Nagaraj	JSSC 00	6	700	0.25	190	3.3	0.45	0.4	0.4	4.7	30	40		Flash, interleaved S/H, interpolation
Y. Tamba	ISSCC 99	6	500	0.4	400	3.3	2.4	0.55	0.65	5.4	34	45		Flash, offset comp. per comp, distrib T/H
K.Yoon	ISSCC 99	6	500	0.6	330	3.3	4	0.5	0.4	3.6	23	34		Flash, interpol., auto-zero (bg), intern T/H
B. Song	VLSI 99	6	50	0.35	20	1	4.8	0.7	0.6	4.2	27			Flash,Current Interpolation, low-supply
K. Nagaraj	JSSC 99	6	75	0.5	110	3.3	1	1	1	5.2	33			Flash with 1-bit folding
M. Flynn	ISSCC 98	6	400	0.5	200	3.2	0.6	0.5	0.5	4	26		1.2	Flash,Folding,interpolating current mode
.Tsukamot	ISSCC 98	6	400	0.35	190	3	1.2	0.25	0.2					Full-Flash with interleav. auto-zero error cor
J. Spalding	ISSCC 96	6	200	0.6	400	5	2.7	0.5	0.5	5	32	35		Full-Flash, auto-zero comparators
R. Roovers	JSSC 96	6	175	0.7	160	3.3	12	1	0.8	4	26		4	Current Interpolation
.Tsukamot	JSSC 96	6	200	0.5	110	3	1.6	0.5	0.3	4	26	32		Full-Flash, interl auto-zero, chopper comp
J. Ming	ISSCC 00	8	80	0.5	250	3	10.3	0.5	0.3	7.3	46	59		pipelined, inter-stage bg calibration
K. Yoon	VLSI 00	8	125	0.35	110	3.3	0.8	1.5	0.7	6.4	40			Flash, fold. & interpol, w. equalizing preamp
Y-T. Wang	JSSC 00	8	150	0.6	400	3.3	1.8	1.24	0.6	6.4	40		1.5	Sliding window pipe. interpolation, dual ch.
M-J. Choe	VLSI 00	8	100	0.5	165	5	1.7	1.3	0.4	6.1	38			pipelined folding
W. Bright	ISSCC 98	8	75	0.5	70	3.3	5.5	0.5	0.5	6.85	43			parallel, pipelined, dual sampling, 1.5b/stage
K. Nagaraj	JSSC 97	8	52	0.9	250	5	15	1	0.2	7.2	45	55		parallel, pipelined, dual sampling, 1.5b/stage
A. Venes	ISSCC 96	8	80	0.5	80	3.3	0.3	0.8	0.45	6.6	42		2	folding&interp, distrib T/H
M.Flynn	ISSCC 95	8	100	1	250	3.3	4			7.2	45		5	folding&interp, current mode interpolation
B. Nauta	ISSCC 95	8	70	0.8	110	5	0.8	0.5	0.2				4.8	folding&interpolating
M.Pelgrom	JSSC 94	8	25	1	250	5	2.8	0.5	0.5	6.4	40			Full-Flash optimized for random offset
C. Conroy	JSSC 93	8	85	1	1100	5	25	1	0.8	6.5	41	46	2	4-way interleaved, pipelined 1.5b/stage
Y. Park	ISSCC 01	10	100	0.18	80	1.8	2.5	0.76	0.66	9	56	64		pipelined, 1.5b/stage, no calibration
B. Brandt	ISSCC 99	10	20	0.5	75	3.3	1.6	0.5	0.4	9.5	59			Two-step, subranging, interpolated comps
H. v.d.Ploeg	ISSCC 99	10	25	0.35	195	3.3	0.66	0.9	0.7	8.2	54	60		Two-step, offs comp res. amp, ladder sharing
K. Dyer	ISSCC 98	10	40	1	650	5	47	0.48	0.3	9	56	74		3-way interl, pipelined, mix signal bg calib
D. Fu	ISSCC 98	10	40	1	565	5	42	0.3	0.14	7.7	48	72		2-way interl, pipelined, digital bg calib LMS
A. Abo	VLSI 98	10	14	0.6	36	1.5	5.8	0.7	0.5	8.2	54			pipelined, 1.5b/stage, no calib, low power
K. Bult	ISSCC 97	10	50	0.5	240	5	2	1.1	0.6	8	50	52		Flash, improved averaging, folding

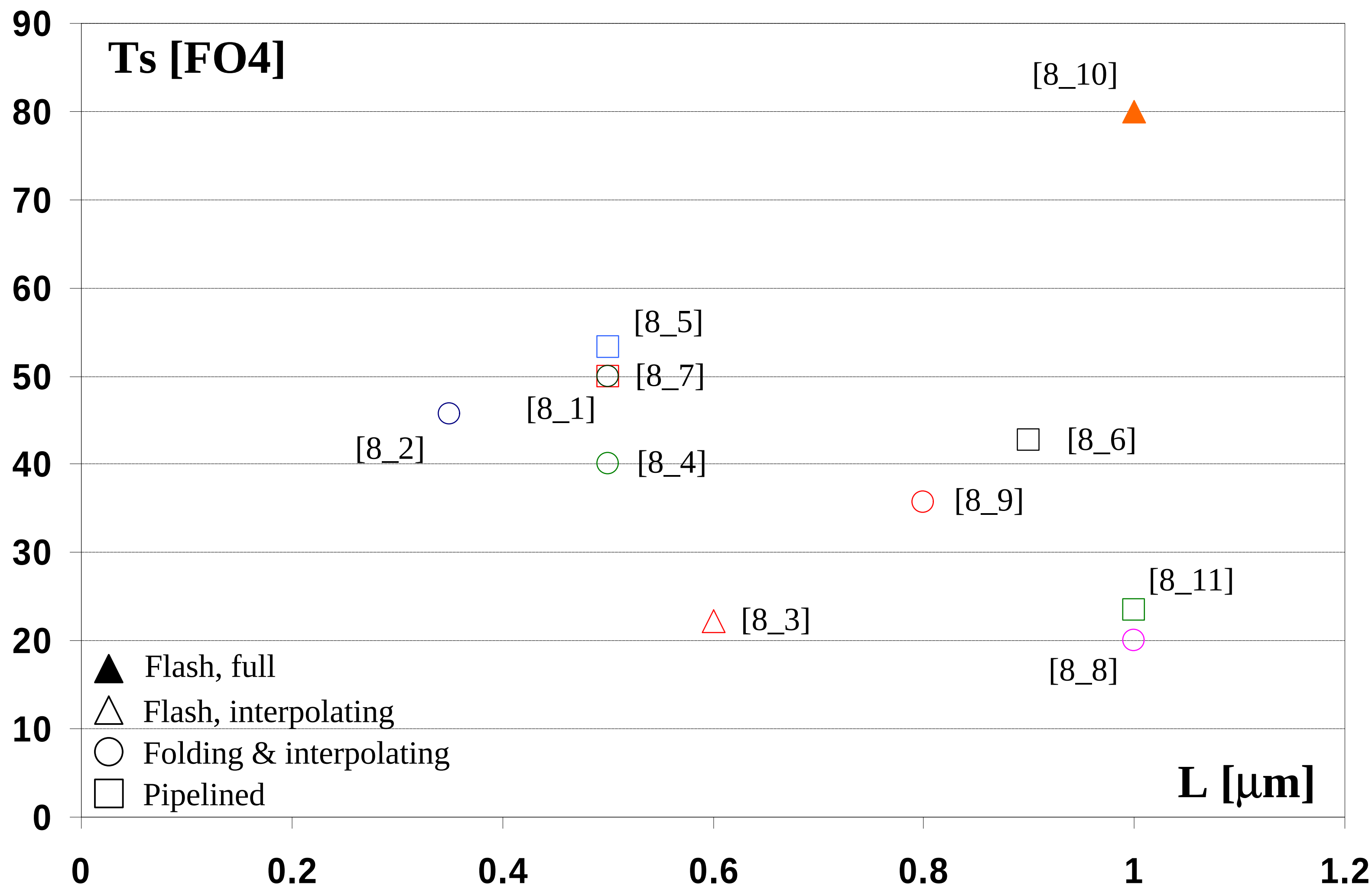
ADCs in ’90s: Scaled data

Labels	Author	Resolution	Ts [FO4]	Tech. [um]	Vdd [V]	A [M]	ED/s	E/s[k MSI]	Emsi [fJ]	E/s [fJ]	FM	Style
[6_1]	M. Choi	6	4	0.35	3.3	26	37	8	23	192308	15	Full-Flash with preamp & two stage averaging
[6_2]	G. Geelen	6	5	0.35	3.3	11	62	12	23	272727	14	Flash, 3 avg, 2 interpolate, distrib T/H
[6_3]	K. Nagaraj	6	11	0.25	3.3	29	190	17	16	271429	12	Flash, interleaved S/H, interpolation
[6_4]	Y. Tamba	6	10	0.4	3.3	60	306	31	26	800000	11	Flash, offset comp. per comp, distrib T/H
[6_5]	K.Yoon	6	7	0.6	3.3	44	112	17	39	660000	13	Flash, interpol., auto-zero (bg), intern T/H
[6_6]	B. Song	6	114	0.35	1	157	21769	190	2	400000	2	Flash,Current Interpolation, low-supply
[6_7]	K. Nagaraj	6	53	0.5	3.3	16	2394	45	33	1466667	7	Flash with 1-bit folding
[6_8]	M. Flynn	6	10	0.5	3.2	10	163	16	31	500000	12	Flash,Folding,interpolating current mode
[6_9]	.Tsukamot	6	14	0.35	3	39	359	25	19	475000	10	Full-Flash with interleav. auto-zero error cor
[6_10]	J. Spalding	6	17	0.6	5	30	370	22	90	2000000	10	Full-Flash, auto-zero comparators
[6_11]	R. Roovers	6	16	0.7	3.3	98	326	20	46	914286	11	Current Interpolation
[6_12]	.Tsukamot	6	20	0.5	3	26	407	20	27	550000	10	Full-Flash, interl auto-zero, chopper comp
							x100					
[8_1]	J. Ming	8	50	0.5	3	165	58	116	27	3125000	8	pipelined, inter-stage bg calibration
[8_2]	K. Yoon	8	46	0.35	3.3	26	18	38	23	880000	10	Flash, fold. & interpol, w. equalizing preamp
[8_3]	Y-T. Wang	8	22	0.6	3.3	20	15	68	39	2666667	10	Sliding window pipe. interpolation, dual ch.
[8_4]	M-J. Choe	8	40	0.5	5	27	9	22	75	1650000	11	pipelined folding
[8_5]	W. Bright	8	53	0.5	3.3	88	15	29	33	933333	10	parallel, pipelined, dual sampling, 1.5b/stage
[8_6]	K. Nagaraj	8	43	0.9	5	74	15	36	135	4807692	10	parallel, pipelined, dual sampling, 1.5b/stage
[8_7]	A. Venes	8	50	0.501	3.3	5	15	31	33	1000000	10	folding&interp, distrib T/H
[8_8]	M.Flynn	8	20	1	3.3	16	8	38	65	2500000	12	folding&interp, current mode interpolation
[8_9]	B. Nauta	8	36	0.8	5	5	5	13	120	1571429	13	folding&interpolating
[8_10]	M.Pelgrom	8	80	1	5	11	53	67	150	10000000	8	Full-Flash optimized for random offset
[8_11]	C. Conroy	8	24	1	5	100	20	86	150	12941176	10	4-way interleaved, pipelined 1.5b/stage
							x1000					
[10_1]	Y. Park	10	111	0.18	1.8	309	25	229	3	800000	7	pipelined, 1.5b/stage, no calibration
[10_2]	B. Brandt	10	200	0.5	3.3	26	23	115	33	3750000	8	Two-step, subranging, interpolated comps
[10_3]	H. v.d.Ploeg	10	229	0.35	3.3	22	78	341	23	7800000	5	Two-step, offs comp res. amp, ladder sharing
[10_4]	K. Dyer	10	50	1	5	188	5	108	150	16250000	11	3-way interl, pipelined, mix signal bg calib
[10_5]	D. Fu	10	50	1	5	168	5	94	150	14125000	11	2-way interl, pipelined, digital bg calib LMS
[10_6]	A. Abo	10	238	0.6	1.5	64	76	317	8	2571429	5	pipelined, 1.5b/stage, no calib, low supply
[10_7]	K. Bult	10	80	0.5	5	32	5	64	75	4800000	11	Flash, improved averaging, folding

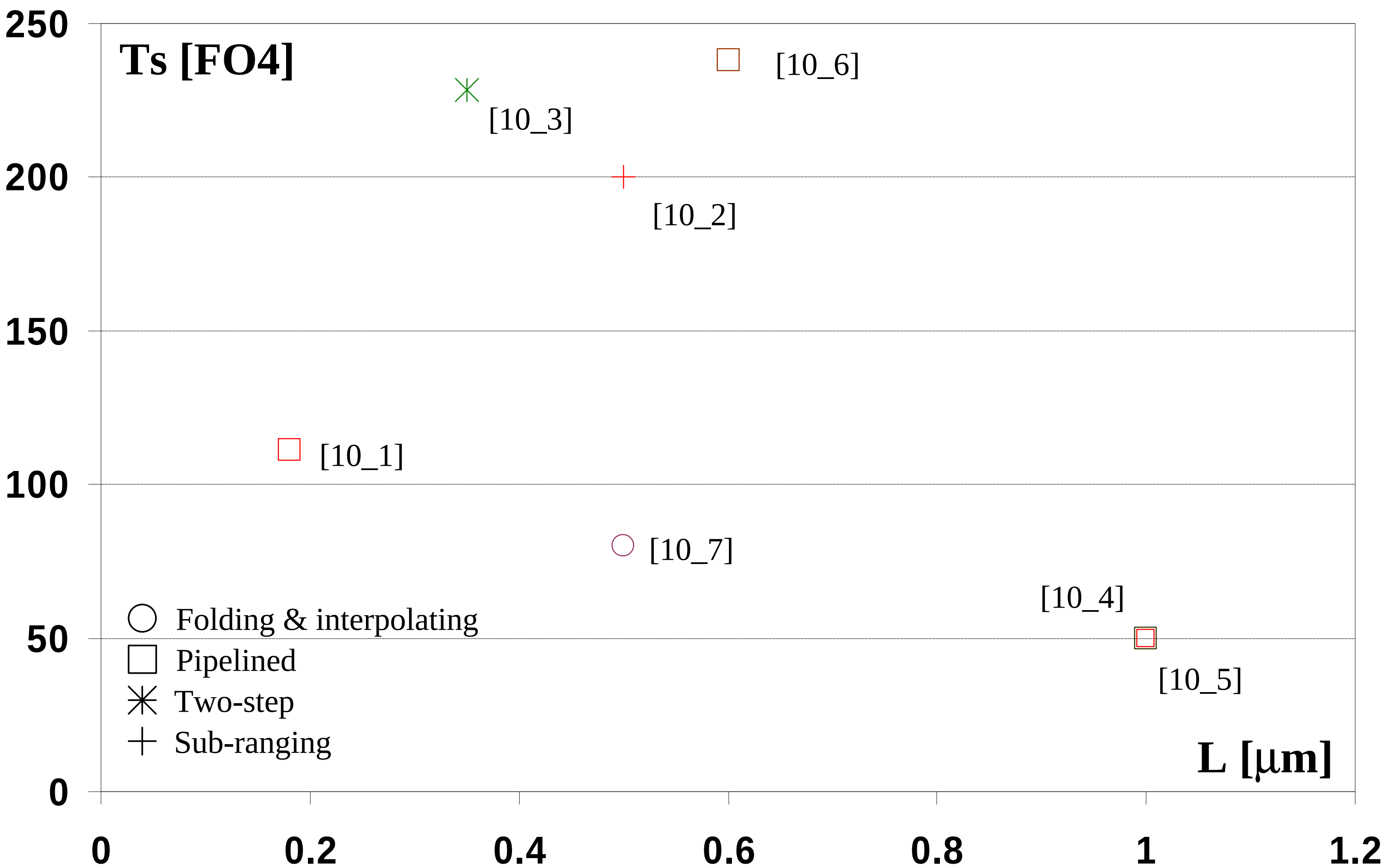
Sampling period vs. technology - 6bit



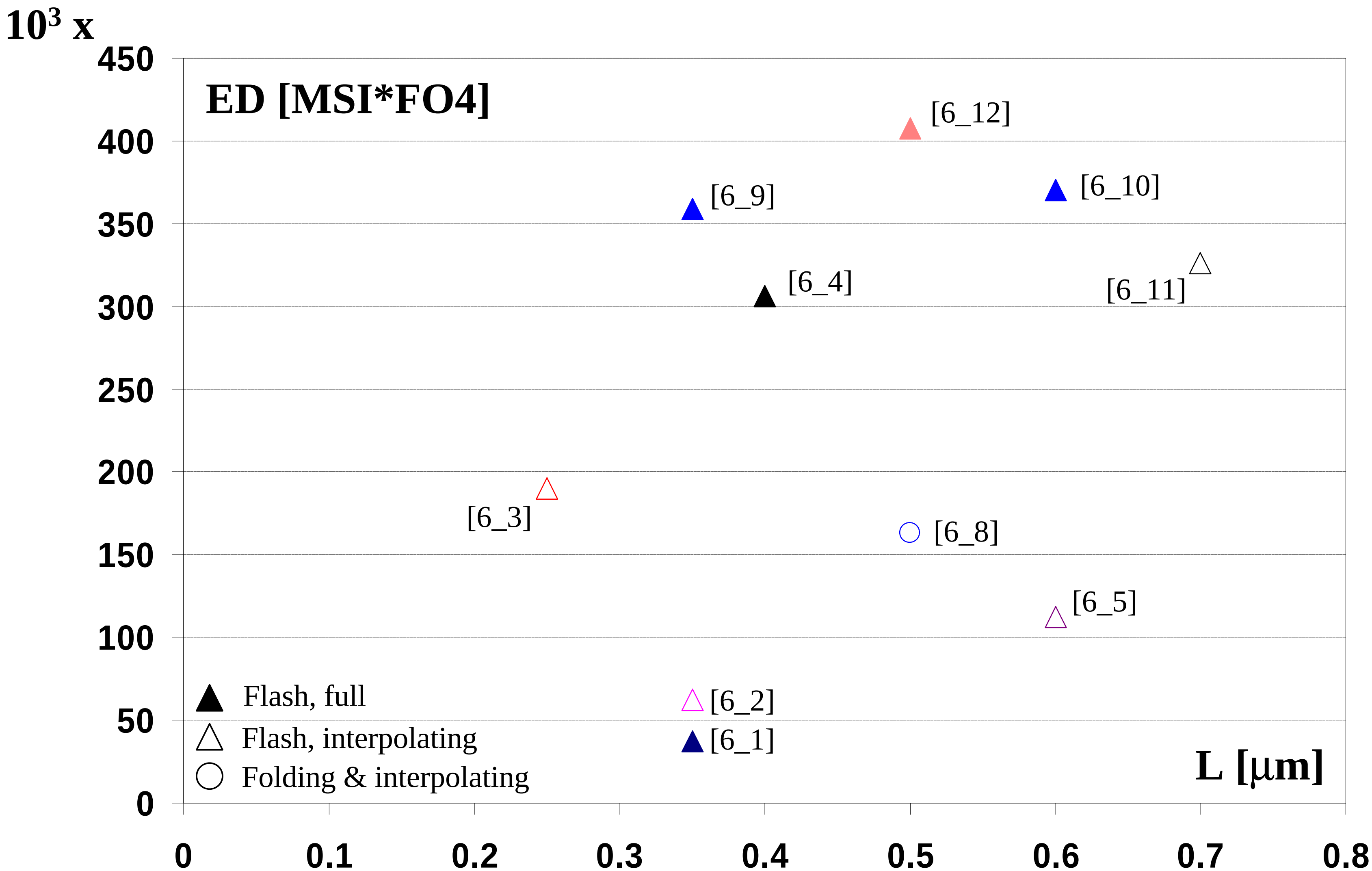
Sampling period vs. technology - 8bit



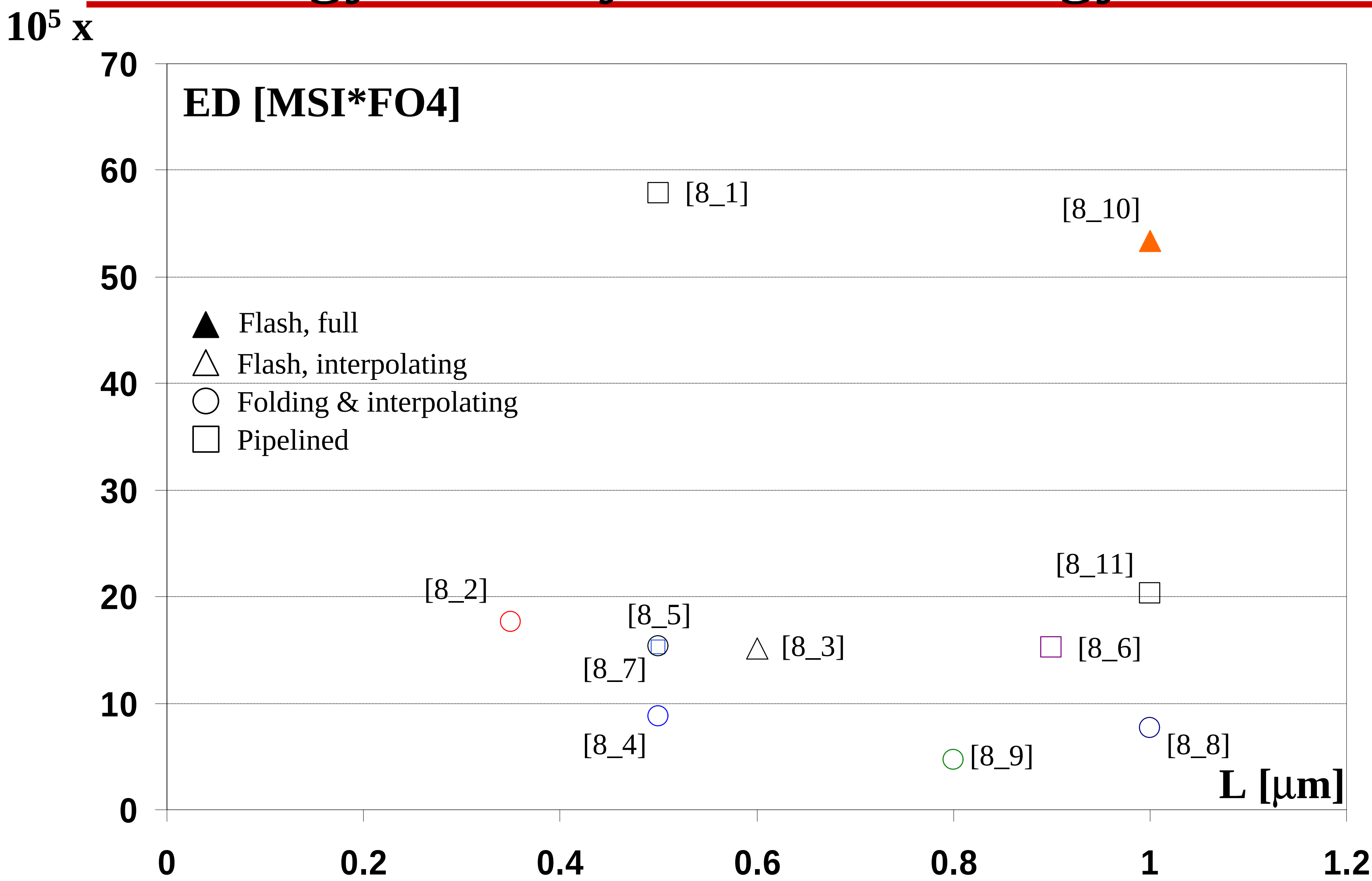
Sampling period vs. technology - 10bit



Energy*"Delay" vs. technology - 6bit



Energy*"Delay" vs. technology - 8bit



Energy*"Delay" vs. technology - 10bit

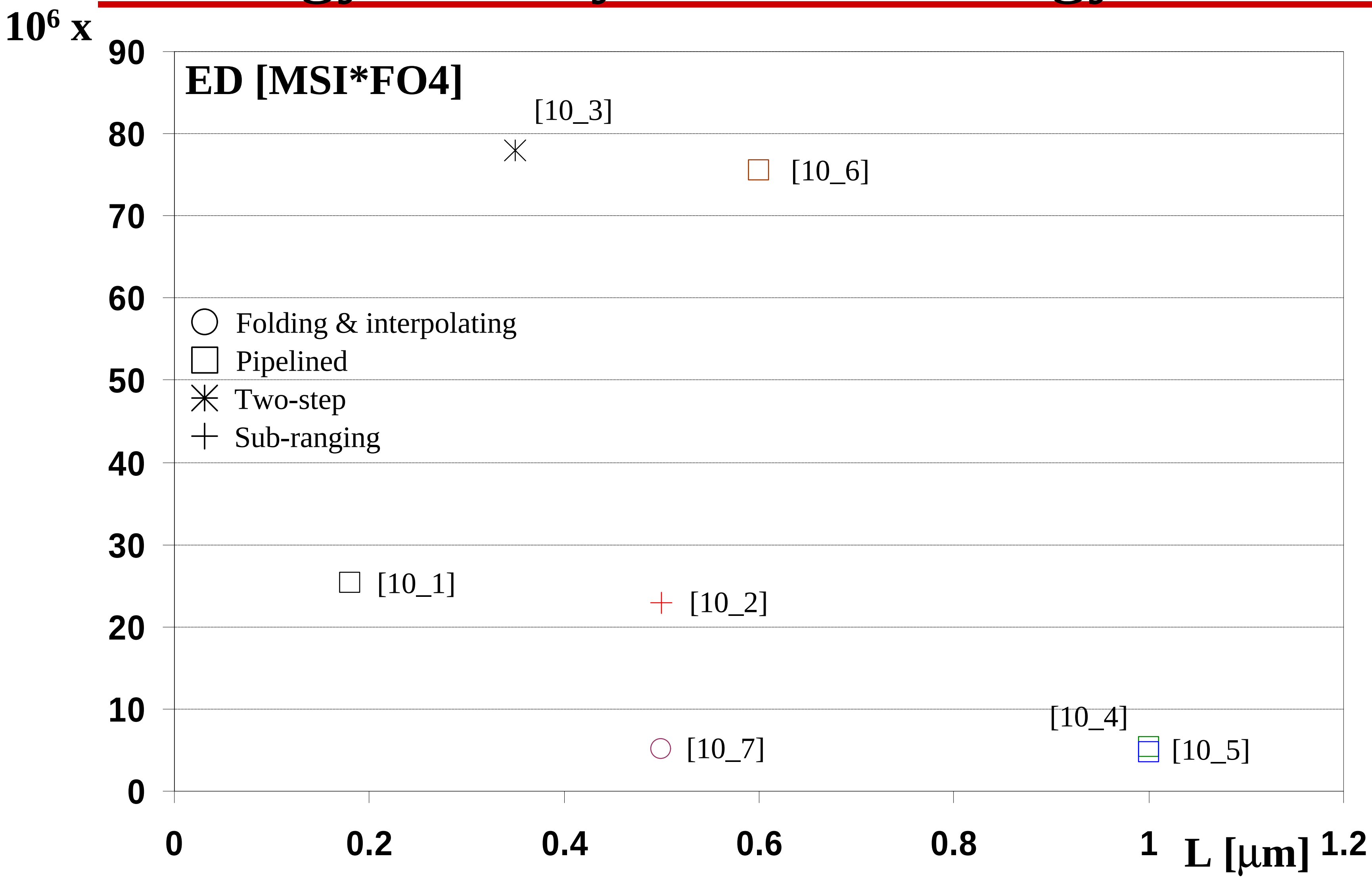
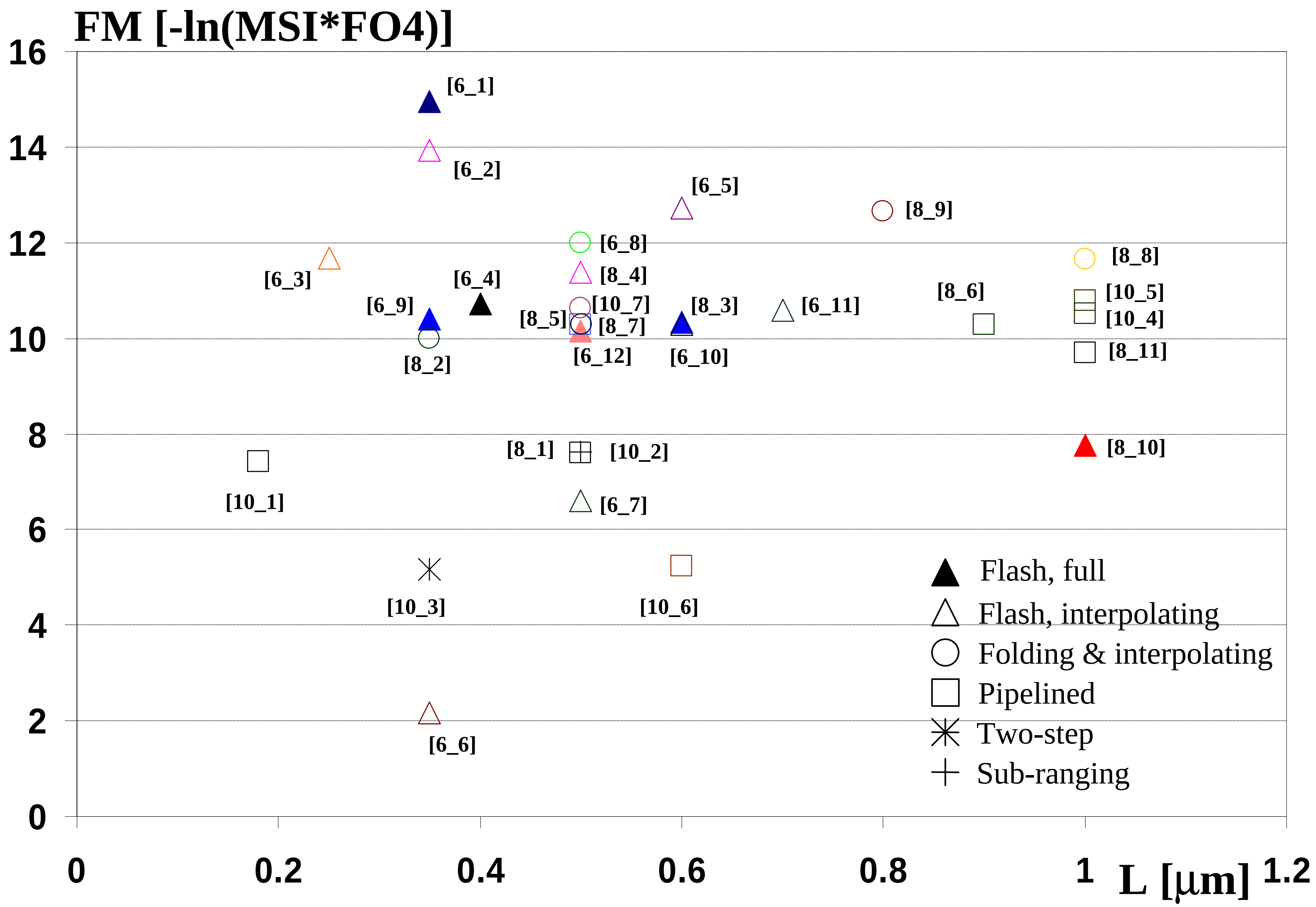


Figure of merit vs. technology



Limiting factors

- Timing errors
  1. Sampling clock jitter
  2. Limited rise/fall time of sampling clock
  3. Skew of clock & input signal at different places on the chip
     (1ps =100-200 μm on a die)
  4. Signal-dependent delay
- Distortion errors
  1. Sampling comparators' aperture time
  2. Distortion in the linear part of the input amplifier
  3. Changes in the reference voltage values & comparator offsets, also kickback
  4. Delays of analog signal and clock signal

Timing Error performance limitations

- Definition A:

$$SNR = -20\log10(2pf_{in}e_{t\_rms})$$

$$e_{t\_rms} < \frac{10^{-(6.02\,ENOB\,+1.76)/20}}{2pf_{in}}$$

- Definition B:

For max fin=1GHz

N	A:ε_{trms}[ps]	B:ε_{trms} [ps]	C:ε_{trms} [ps]
2	33	27	53
4	8	7	27
6	2	2	14
8	0.5	0.4	7
10	0.1	0.1	3

$$2pf_{in}A\Delta t < 1LSB = \frac{2A}{2^N}$$

$$e_{t\_rms} < \frac{1}{3p\;2^N\;f_{in}}$$

- Definition C:

$$e_{t\_rms} < \frac{1}{3p\;2^{LENOB\;/2}\;f_{in}}$$

Taking into account both transmitter and receiver noise and budgeting 50% for other noise

Conclusion

- Future – very high speed ADCs
  - Digitally corrected interpolated Flash
  - Time-Interleaved pipelined ADC with channel mismatch calibration
- Big problem – timing errors
  - Most of all jitter – after all it is Gaussian noise limit
  - Jitter is less of a problem for digital data communications
- Spectrum allocation limitations for wireless
  - Most of ADCs need not be very, very high speed

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