mum and minimum power spectral density (PSD) levels. In the case of a single-channel receiver, this implies the gain control range of the VGA, while in a multi-channel receiver the variation of the rms power of all the received channels must be added to the A/D converter dynamic range. In WCDMA specifications, e.g. the dynamic range at antenna connector in the 3.84 MHz band is -25 dBm-( -106.7 dBm)=81.7 dB.

### 2.3.3 Linearity

Nonlinearity is another point of major concern in receiver design. The linearity of an A/D converter is commonly characterized by the level of harmonic distortion (HD), which, as presented above, is closely linked to the intermodulation distortion (IMD), which in turn is usually the base of the linearity characterization of a radio receiver [7].

In the case of an IF-sampling super heterodyne receiver, the third-order intercept point, IP3, is of major importance, while in a direct conversion receiver the second-order intercept point, IP2, is of equal interest. Both parameters can be tested for the whole receiver with the two-tone test. The third-order input intercept point of the whole receiver consisting of cascaded stages can be calculated with an equation

$$\frac{1}{iip3} = \frac{1}{iip3_1} + \frac{G_1}{iip3_2} + \frac{G_1 G_2}{iip3_3} + \ldots + \frac{\prod_{i=1}^{n-1} G_i}{iip3_n}, \tag{2.22}$$

where $iip3_i$ and $G_i$ are the input intercept point and power gain of the $i^{th}$ block as absolute values. The last analog block in a receiver chain is the ADC, which results $iip3_n = ip3_{ADC}$. A similar equation holds for $iip2$ as well. The filters attenuating the interferers along the chain must be taken into account. If a steep channel selection filter is placed before the A/D converter, the unwanted tones are filtered sufficiently and the contribution of the ADC to the receiver linearity is negligible. This is the case in a direct conversion receiver, while in an IF-sampling super heterodyne receiver, the attenuation of the IF-filter can be traded with the linearity of the A/D converter.

Specifications for IP2 and IP3 in a WCDMA system can be calculated from the standard [8, 13].

## 2.4 A/D Converter Survey

The high and medium speed Nyquist rate ADCs reported in the Custom Integrated Circuits Conference (CICC), International Solid-State Circuits Conference (ISSCC), Journal of Solid-Sate Circuits (JSSC), and Symposium on VLSI Circuits during the period 1995-2001 are plotted in Fig. 2.6. The three most common architectures, i.e.

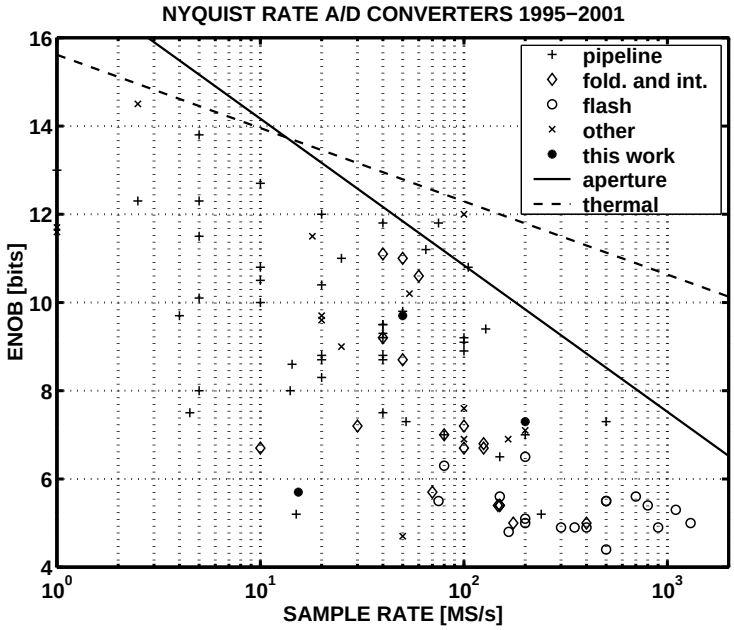


**Figure 2.6** High-speed A/D converters from years 1995-2001.

pipelined, folding and interpolating, and flash A/D converters, are labeled, as well as the experimental pipeline ADCs included in this thesis. The trade off between the resolution, in terms of the effective number of bits (ENOB), and sample rate, is apparent. Furthermore, different architectures have specified application ranges. The flash ADCs are optimal for very high sample rate and low resolution, while the folding and interpolating architecture is applied for medium and low resolution up to a 400-MS/s sample rate. The pipeline ADCs cover the largest range reaching from 14-bit 5-MS/s up to 7-bit 500-MS/s performance. $\Delta\Sigma$-modulators, not shown in Fig. 2.6, employ oversampling and noise-shaping to achieve the best performance at signal frequencies up to a few megahertz.

At high resolutions the spectral noise density at the A/D converter input is dominated by the thermal noise inherited from the sampling operation. If the thermal noise is considered as the only noise source, the attainable resolution $N_{thermal}$ is calculated in appendix A to be

$$N_{thermal} = \frac{1}{2}\log_2\left(\frac{V_{FS}^2}{6kTR_{eff}f_S}\right) - 1, \tag{2.23}$$

where $k$ is the Boltzmann's constant, $T$ the temperature, $f_S$ the sample rate, and $R_{eff}$ an effective thermal resistance, which includes the effects of all noise sources. Especially at high sample rates, the resolution is limited, in turn, by the aperture uncertainty

resulting from a random deviation of the sample interval. An rms aperture jitter $\sigma_a$ is shown in appendix A to limit the effective resolution to

$$N_{aperture} = \log_2\left(\frac{2}{\sqrt{3}\pi f_S \sigma_a}\right) - 1. \tag{2.24}$$

Both of these ADC resolution boundaries are plotted as references in Fig. 2.6 with parameters $R_{eff} = 3000\,\Omega$ and $\sigma_a = 3$ ps. The thermal noise is actually becoming to limit the resolution above 14-bit, and is thus more suitable to characterize ΔΣ-modulators. The resolution boundary set by the aperture jitter is clearly more relevant when Nyquist rate ADCs are considered. As crystals with a relative dependence of the jitter on the frequency are used as ADC clocks, the aperture jitter is actually increasing with the sample rate. This is visible in Fig. 2.6 as a steeper slope for the attainable resolution at a given sample rate than that calculated from Eq. 2.24. However, neither of these limitations is even close to the ultimate limits dictated by physical laws, like, for example, Heisenberg uncertainty principle, leaving an attractive field for engineers to improve the implementations [15].

When quantifying the efficiency of the A/D converter implementations, power dissipation should be included in the resolution and sample rate. However, power dissipation is a nonlinear function of the resolution and sample rate and a wide variety of figures of merit exist to relate all these parameters. The most widely accepted measure of the effectiveness of the design is the energy per conversion step, defined as

$$E_{conv} = \frac{P_D}{2^N \cdot f_S}, \tag{2.25}$$

where $P_D$ is the power dissipation, $N$ the resolution, and $f_S$ the sample rate. Comparison of the same designs using Eq. 2.25 is given in Fig. 2.7, where power dissipation is plotted as a function of $2^N \cdot f_S$. The lower the energy per conversion step the better the ADC. However, it should be noted that the reported A/D converter power dissipations are often excluding output buffers and references. The solid and dash dotted lines, within which all the state-of-the-art Nyquist rate ADCs fall, represent constant $E_{conv}$ levels of 0.5 pJ and 50 pJ, respectively. The pipeline A/D converters tend to be more efficient than those that are folding and interpolating, while the flash ADCs show the highest energy per conversion step. The designs presented in this thesis employ good energy efficiency.

In addition to the power dissipation, the silicon area contributes significantly to the effectiveness of an A/D converter implementation. A similar figure of merit that relates

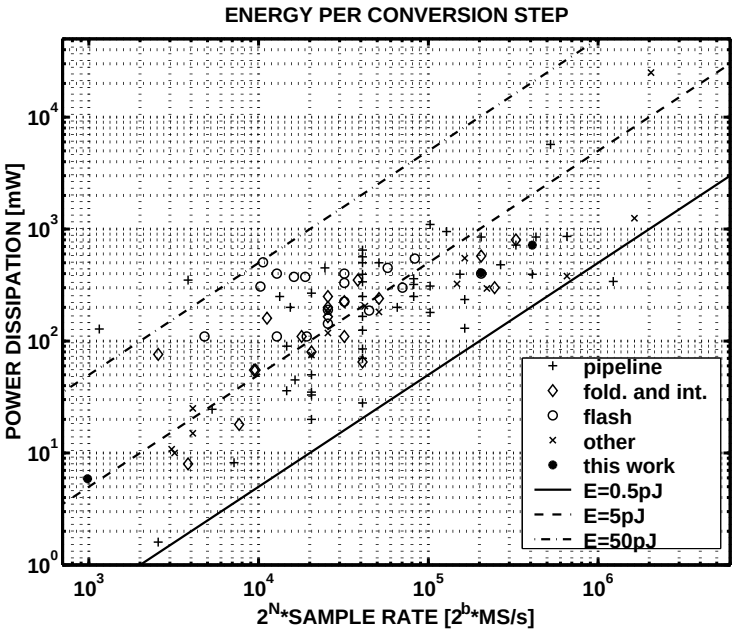


**Figure 2.7** Power dissipation plotted as a function of the number of the quantization levels times sample rate for Nyquist rate ADCs published 1995-2001.

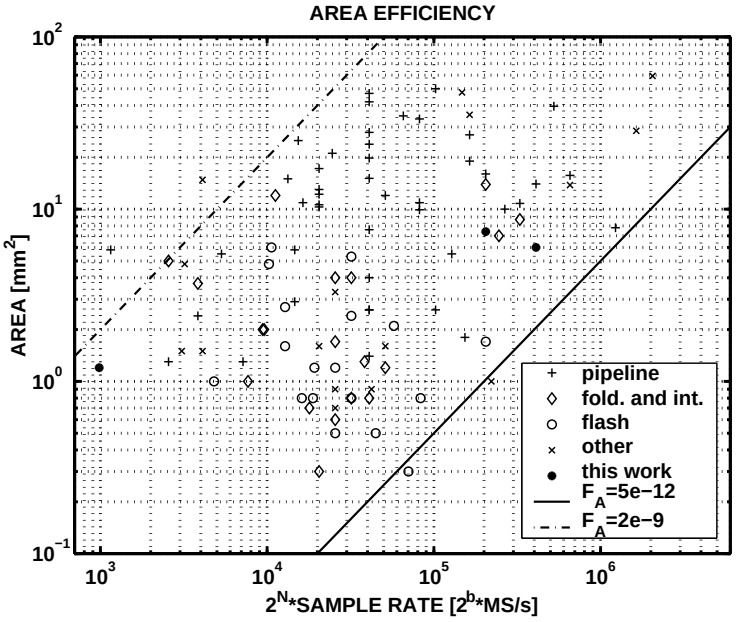


**Figure 2.8** Active area plotted as a function of the number of the quantization levels times sample rate for Nyquist rate ADCs published 1995-2001.

the area $A$, resolution $N$ and sample rate $f_S$ can be derived from equation

$$FOM_A = \frac{A}{2^N \cdot f_S}. \tag{2.26}$$

In Fig. 2.8 the active silicon area of the recently reported ADCs is plotted as a function of the number of conversion steps times the sample rate. It should be noted that the total die area only was reported for some of the referred designs, which distorts the comparison. The straight lines in Fig. 2.8 represent the figure of merit levels of $5 \cdot 10^{-12} m^2/Hz$ and $2 \cdot 10^{-9} m^2/Hz$. Compared to the efficiency figure of the same A/D converters, the spread is much larger in the case of $FOM_A$ and no clear tendencies between the different architectures exist. Furthermore, as most of the published Nyquist rate A/D converters are academic demonstration circuits, their layout is seldom area-optimized and no state-of-the-art silicon process is employed. As can be seen, the prototypes included in this thesis do very well when compared to other pipeline ADCs. The flash ADCs tend to be area-efficient, while the pipeline ones have the worst figures of merit, which is a result of the predominating switched capacitor (SC) realization leading to a large area consumption. However, the efficiency per conversion step is a better figure of merit than the area when comparing the designs.

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