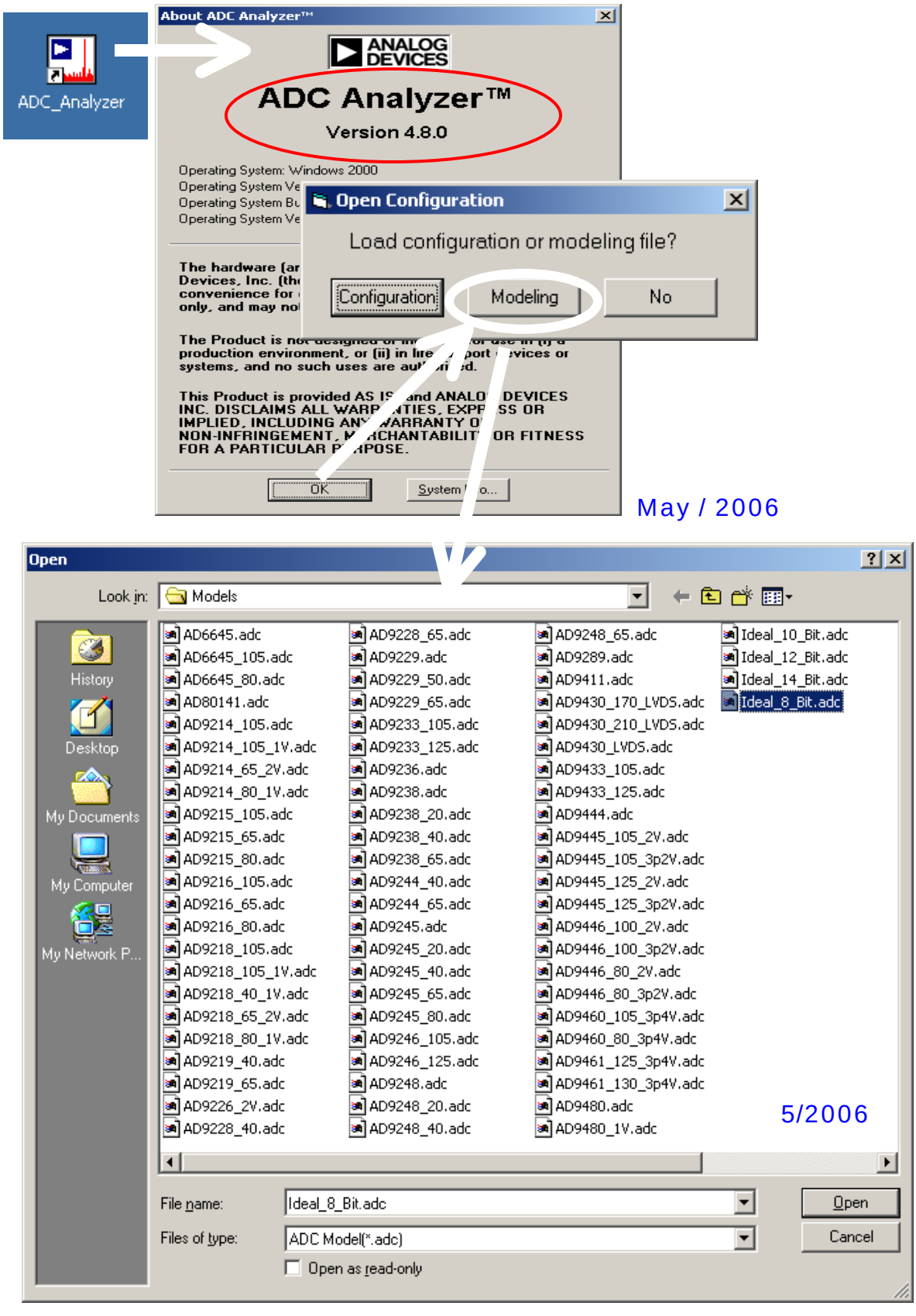
ADC_Analyzer
About ADC Analyzer™
ANALOG DEVICES
ADC Analyzer™
Version 4.8.0
Operating System: Windows 2000
Open Configuration
Load configuration or modeling file?
Configuration
Modeling
No
OK
May / 2006
Open
Look in:
Models
History
Desktop
My Documents
My Computer
My Network P...
AD6645.adc
AD6645_105.adc
AD6645_80.adc
AD80141.adc
AD9214_105.adc
AD9214_105_1V.adc
AD9214_65_2V.adc
AD9214_80_1V.adc
AD9215_105.adc
AD9215_65.adc
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AD9218_65_2V.adc
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AD9289.adc
AD9411.adc
AD9430_170_LVDS.adc
AD9430_210_LVDS.adc
AD9430_LVDS.adc
AD9433_105.adc
AD9433_125.adc
AD9444.adc
AD9445_105_2V.adc
AD9445_105_3p2V.adc
AD9445_125_2V.adc
AD9445_125_3p2V.adc
AD9446_100_2V.adc
AD9446_100_3p2V.adc
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AD9461_125_3p4V.adc
AD9461_130_3p4V.adc
AD9480.adc
AD9480_1V.adc
Ideal_10_Bit.adc
Ideal_12_Bit.adc
Ideal_14_Bit.adc
Ideal_8_Bit.adc
5/2006
File name:
Ideal_8_Bit.adc
Files of type:
ADC Model(*.adc)
Open
Cancel
Open as read-only

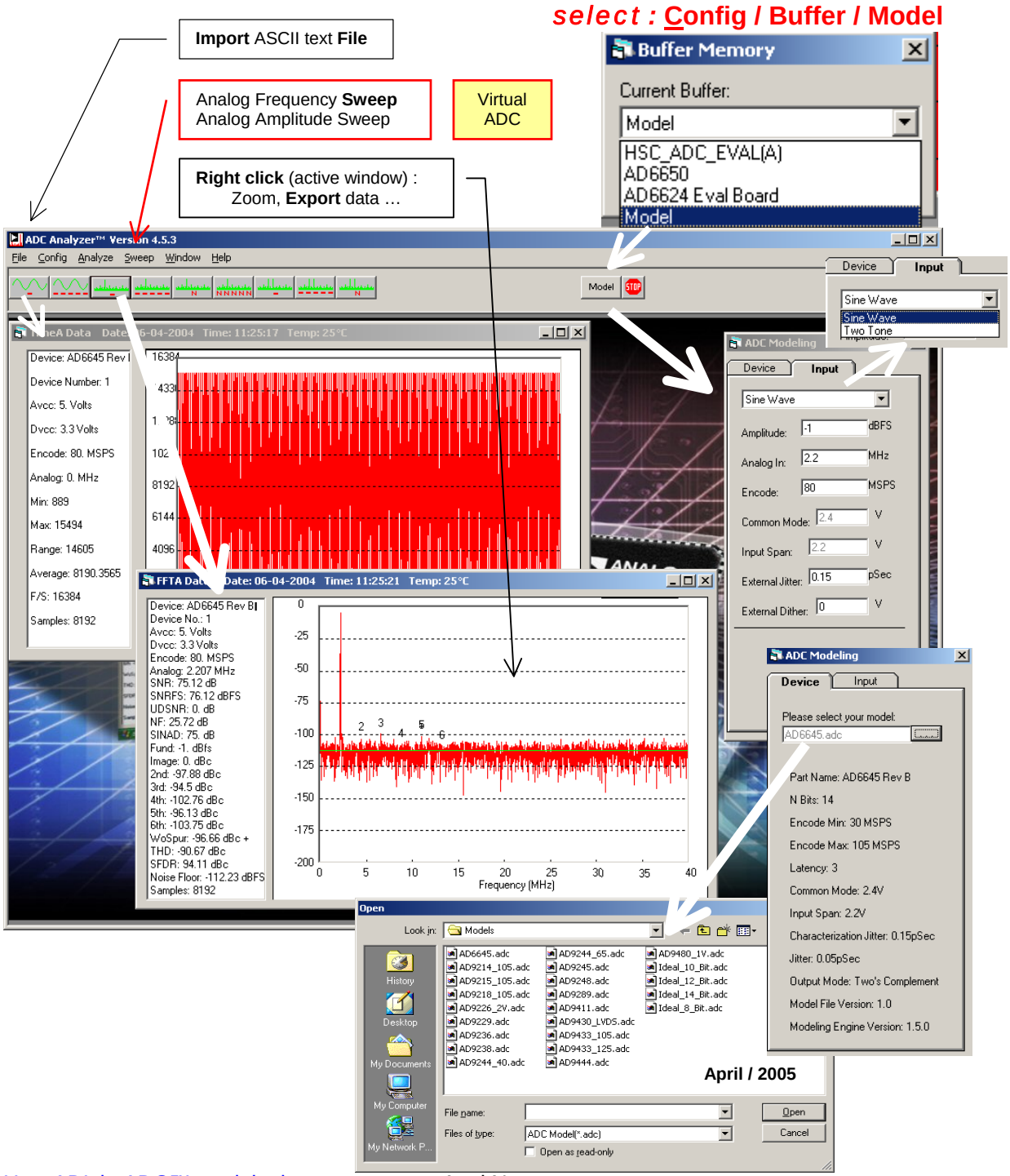
ADC Analyzer ™

http://www.analog.com/ADIsimADC – Live data sheets; virtual ADC evaluation

ADC Analyzer incorporates **ADIsimADC™** modeling tool in conjunction with **product model files**.

The techniques used within ADIsimADC models are based on *behaviors* exhibited by a specific device under *typical* operating conditions using the *recommended* layout highlighted in the datasheet.

No hardware is required.



How ADIsimADC™ models data converters– Appl Note

High Speed ADC USB FIFO Evaluation Kit – ADC Analyzer functions

High Speed ADCs (>10 MSPS) `...models` **April / 2005**

- ✔ **Ideal 8/10/12/14 bit** ADC
- ✔ AD6645 **14-Bit, 80 / 105 MSPS** A/D Converter
- ✔ AD9214 **10-Bit, 65/80/105 MSPS,** +3.3V A/D Converter
- ✔ AD9215 **10-Bit, 65/80/105 MSPS** 3 V A/D Converter
- ✔ AD9218 **Dual 10-Bit 40 / 65 / 80 / 105 MSPS** A/D Converter
- ✔ AD9226 **12-Bit, 65 MSPS** A/D Converter
- ✔ AD9229 **Quad 12-Bit, 50/65 MSPS,** Serial LVDS A/D Converter
- ✔ AD9236 **12-Bit, 80 MSPS** 3 V A/D Converter
- ✔ AD9238 **12-Bit, 65 MSPS** 2 V A/D Converter
- ✔ AD9244 **14-Bit 40/65 MSPS** IF Sampling A/D Converter
- ✔ AD9245 **14-Bit, 80 MSPS** 3 V A/D Converter
- ✔ AD9248 **14-Bit, 65 MSPS** 2 V A/D Converter
- ✔ AD9289 **8 bit 65 MSPS** 2V A/D Converter
- ✔ AD9411 **10-Bit, 170 / 200 MSPS** 3.3 V A/D Converter
- ✔ AD9430 **12-Bit, 170 / 210 MSPS** 3.3 V A/D Converter LVDS Output Mode
- ✔ AD9433 **12-Bit 105 / 125 MSPS** IF Sampling A/D Converter
- ✔ AD9444 **14-Bit, 80 MSPS** 2 V A/D Converter
- ✔ AD9480 **8 bit 250 MSPS** 1V A/D Converter

TERMINOLOGY**:** **SINGLE-TONE FFT**

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components, *excluding* the first five harmonics and dc. It is reported in dBc.

Signal-to-Noise Ratio Full Scale (SNRFS)
The ratio of the rms signal amplitude related to full scale (0 dB) to the rms value of the sum of all other spectral components, *excluding* the first five harmonics and dc. It is reported in dBFS.

User Defined Signal-to-Noise Ratio (UDSNR)
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components within a specified band set by the user, *excluding* harmonics and dc. It is reported in dB.

Noise Figure (NF)
The noise figure is the ratio of the noise power at the output of a device to the noise power at the input to the device, where the input noise temperature is equal to the reference temperature (273 K). The noise figure is expressed in dB.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components, *including* harmonics but *excluding* dc. It is reported in dB.

nonHarmonic Distortion, Image
The ratio of the rms signal amplitude to the rms value of the **non**harmonic component generated from the clocking phase difference of **two** ADCs, reported in dBc.
Note: This measurement result is valid *only* when analyzing **demultiplexed** ADCs.

Harmonic Distortion, Second (2^{nd})–Sixth (6^{th})
The ratio of the rms signal amplitude to the rms value of the fundamental related harmonic component, reported in dBc.

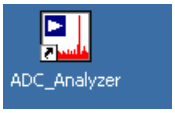
Worst Other Spur (WoSpur)
The ratio of the rms signal amplitude to the rms value of the worst spurious component (*excluding* all harmonically related components) reported in dBc.

Total Harmonic Distortion (THD)
The rms value of the sum of *all* spectral harmonics *specified by the user*. It is reported in dBc.

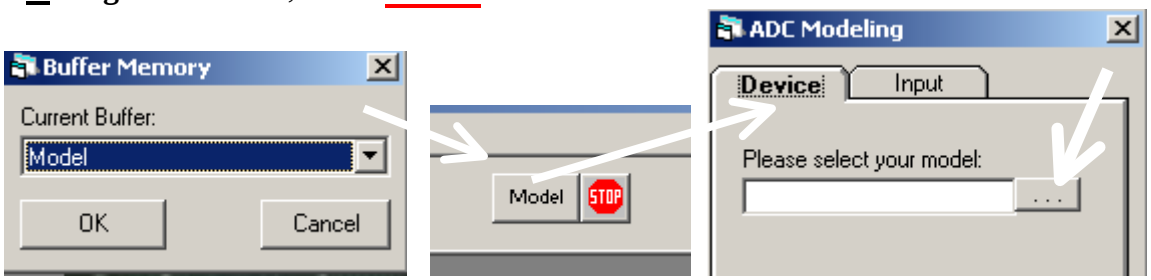
Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It is reported in dBc.

Noise Floor
The rms value of the sum of all other spectral components, *excluding* the fundamental, its harmonics, and dc referenced to full-scale and reported in dBFS.

ADC_analyzer with ADIsimADC
(Virtual Evaluation Board. **No** hardware is required.)

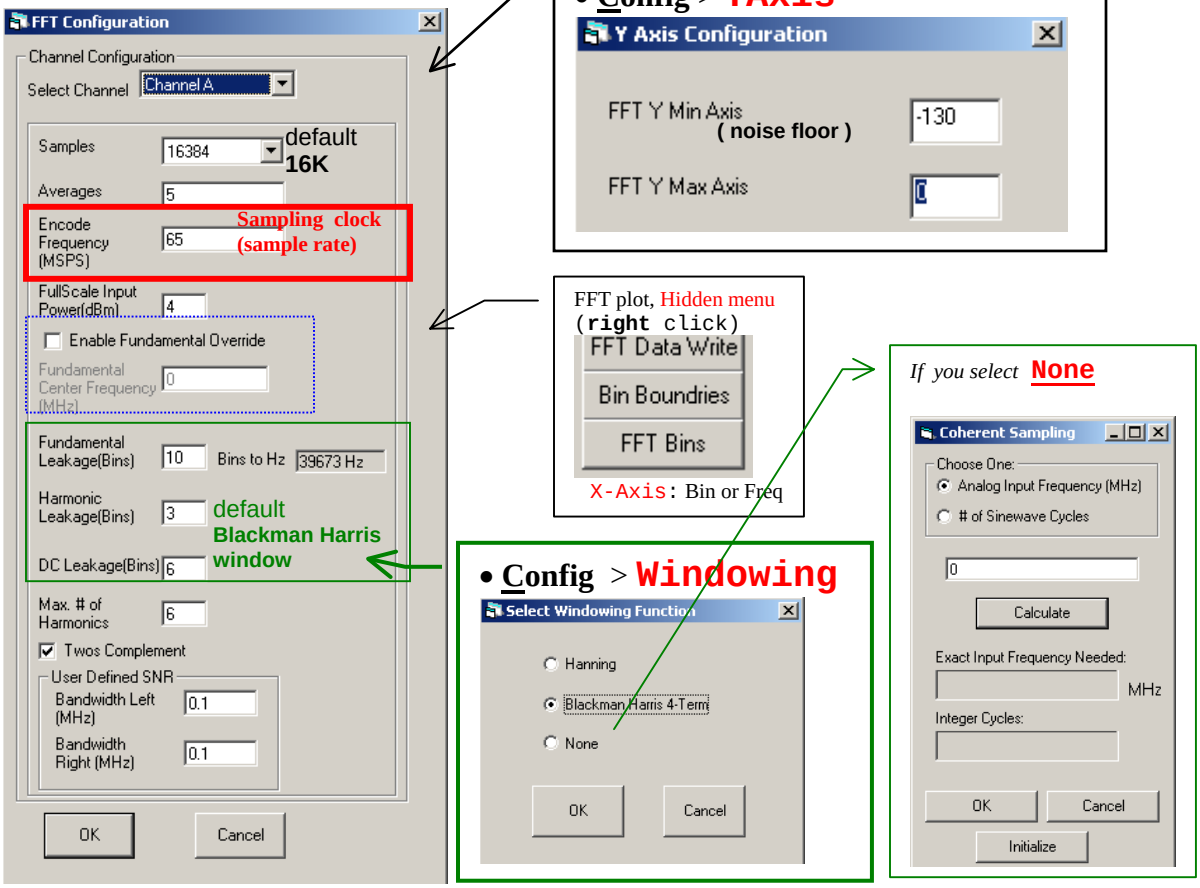
Run: 

• **C**onfig > **Buffer**, *select* **Model**



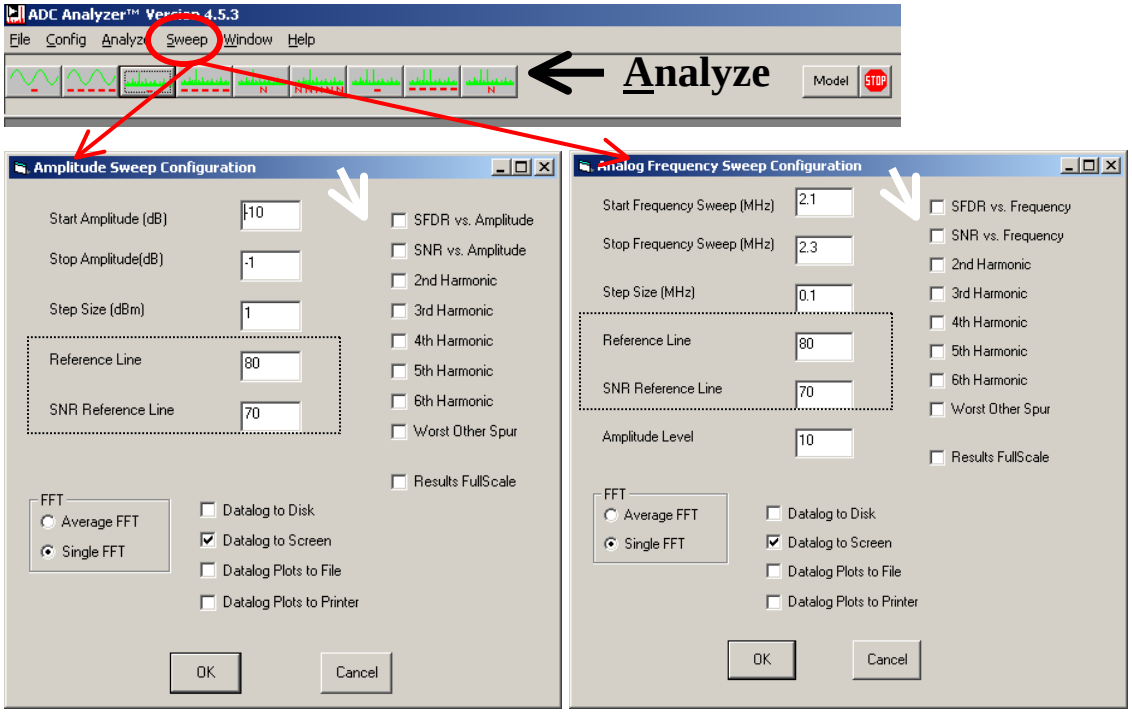
Models in the default directory
c:\program files\adc_analyzer\models

• **C**onfig > **FFT**



Note: if Enable Fundamental Overdrive is checked, the Fundamental Center Frequency (MHz) box is enabled for the user to specify. (Default: the highest spur as the fundamental freq.)

- **Analyze** (Time Domain, FFT, Avg FFT, Two Tone)
  or
- **Sweep**ing of the analog input level (amplitude) and frequency [**virtual ADC** only]



To zoom in a displayed analog signal or FFT, select the portion of the signal by holding down the `left mouse` button and dragging across the area of interest.
Bring up a hidden menu by clicking the **`right`** `mouse` in the active window.

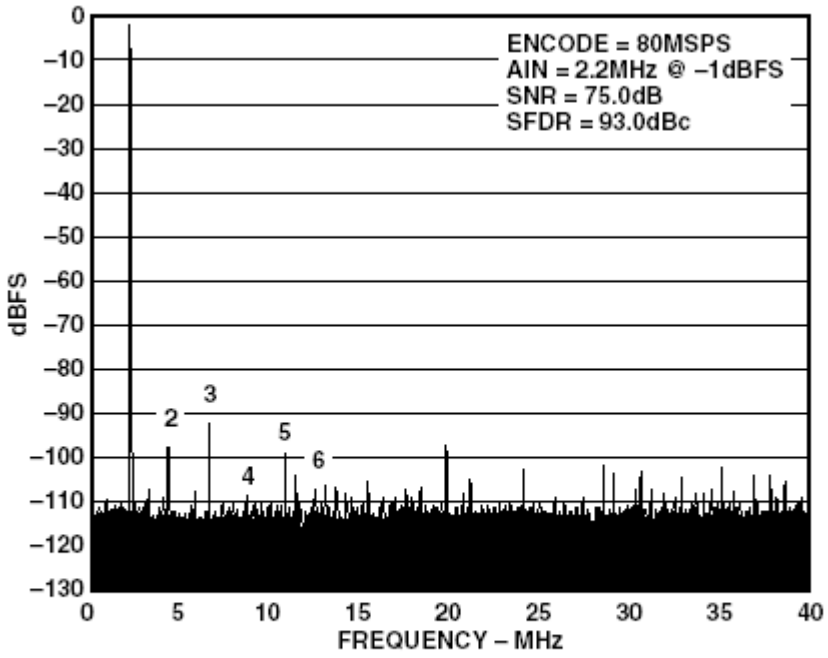
******

"Modeling a system or even just an ADC, should never be a substitute for building and characterizing a real system. As any RF engineer will tell you, it is one thing to **model** a circuit, but it is completely another to actually **build** it up and **test** it. As with any analog or mixed signal device, proper layout and configuration is required to achieve the performance shown in simulation.

ADIsimADC™ is targeted at providing realistic performance of real devices based on recommend layouts as shown in the data sheet."

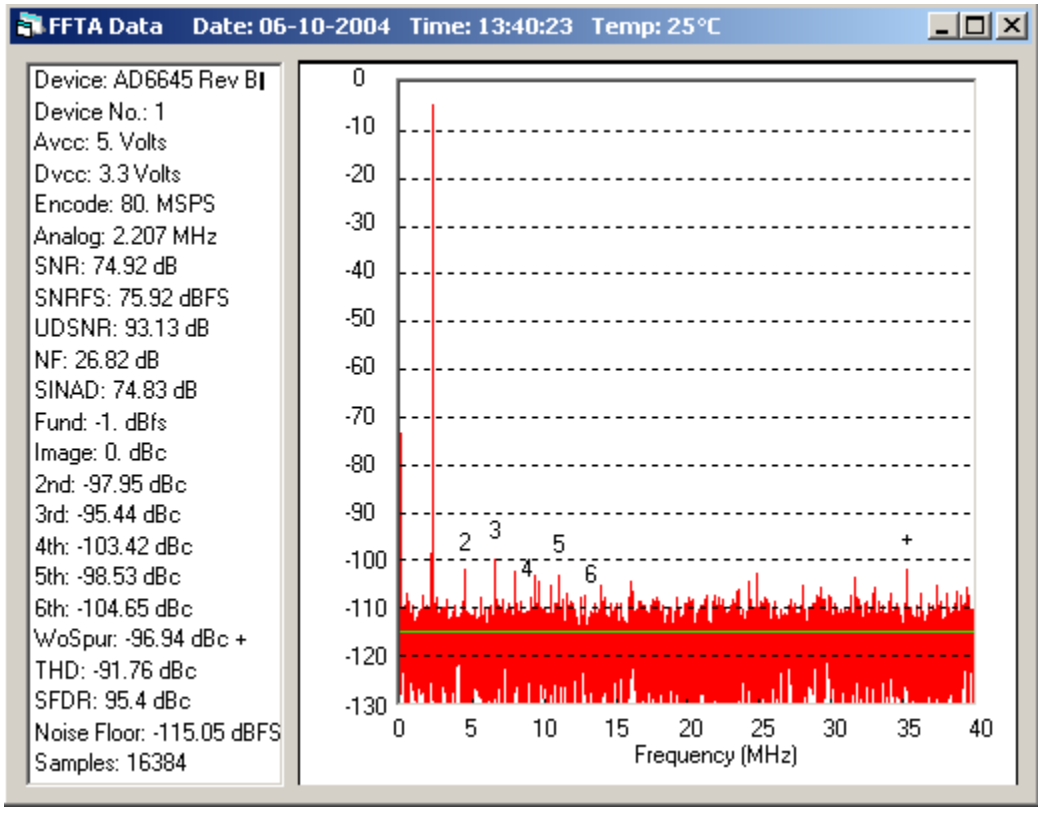
Typical Performance Characteristics–AD6645

Data Sheet:



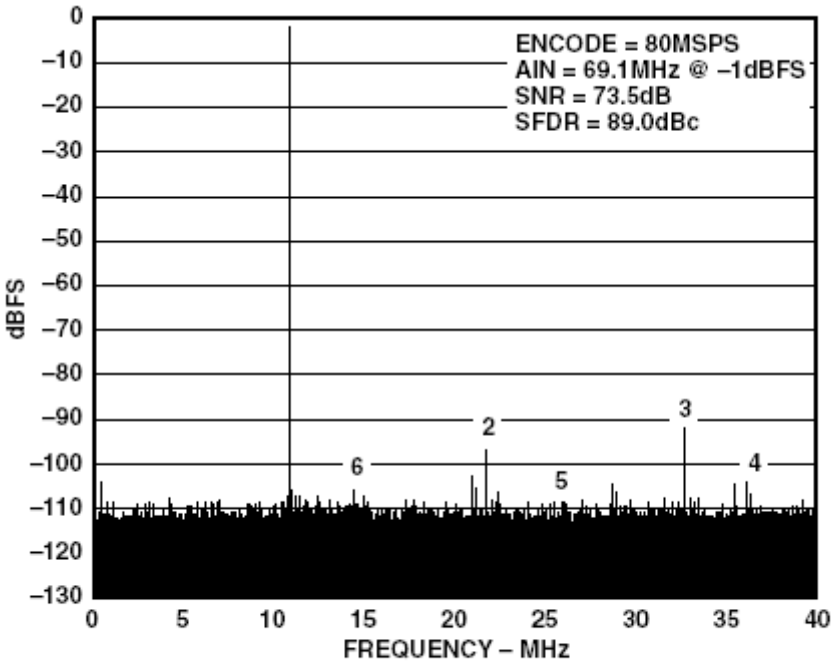
TPC 1. Single Tone @ 2.2 MHz

ADIsimADC:



Typical Performance Characteristics–AD6645

Data Sheet:



TPC 4. Single Tone @ 69.1 MHz

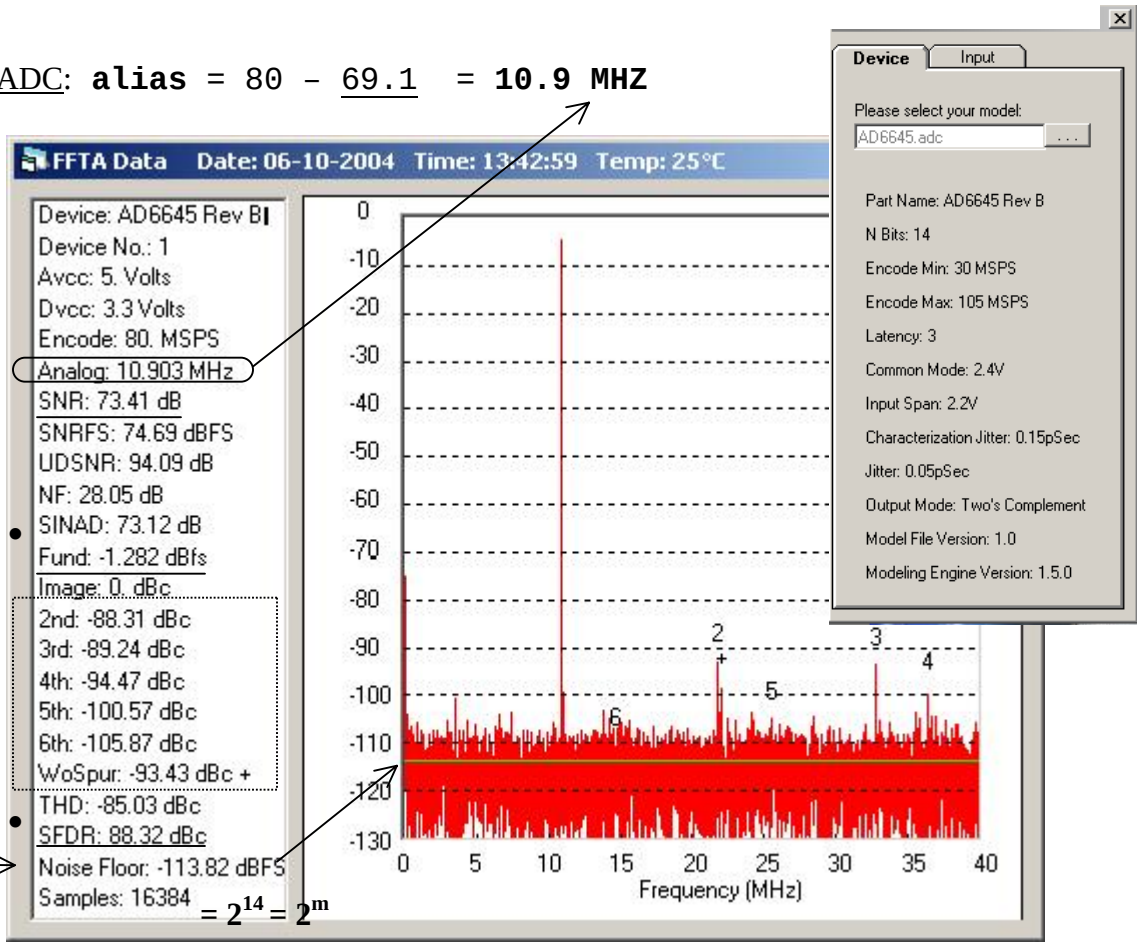
ADIsimADC: **alias** = 80 – 69.1 = **10.9 MHZ**

UDSNR:
User **D**efined SNR (within a specified band)

NF:
Noise Figure

WoSpur:
Worst **o**ther Spur (**+**)

Noise**Fl**oor ≈ SNR+3·(**m**-1) = 112.41



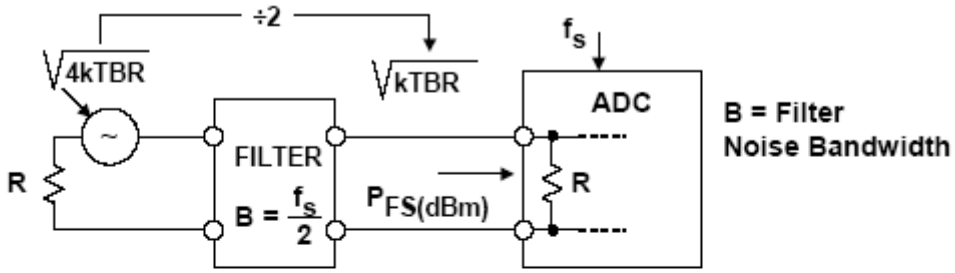
$= 2^{14} = 2^{m}$

Noise Factor (F) and **Noise Figure (NF) – AD6645**

The *noise factor*, F, is simply defined as the *ratio* of the total effective input noise power of the ADC to the amount of that noise power caused by the source resistance alone. (See Note) Because the **impedance is matched**, the square of the voltage noise can be used instead of noise power.

The ***noise figure*, NF**, is simply the noise factor expressed in dB, **NF** = $10\log_{10}(F)$.

The amount of the input voltage noise due to the source resistance is the voltage noise of the source resistance √(4kTBR) divided by two, because of the 2:1 attenuator.



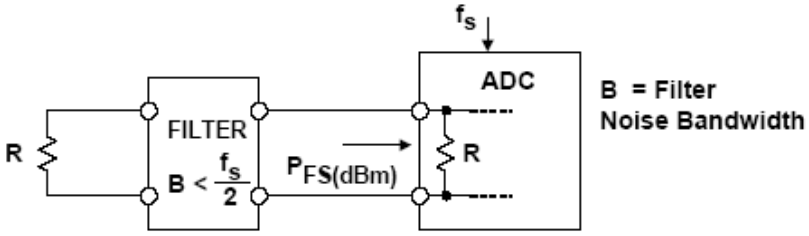
$$V_{NOISE\text{-}RMS} = V_{FS\text{-}RMS}\, 10^{-SNR/20}$$

$$F = \frac{V_{NOISE\text{-}RMS}^{2}}{kTRB} = \left[\frac{V_{FS\text{-}RMS}^{2}}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-SNR/10}\right]\left[\frac{1}{B}\right]$$

$$NF = 10\log_{10}F = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B,$$

where SNR is in dB, B in Hz, T = 300K, $k = 1.38 \times 10^{-23}$ J/K

Oversampling and filtering can be used to decrease the noise figure as a result of the process gain.



$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}\left[\frac{f_S/2}{B}\right] - 10\log_{10}B,$$

Measured DC to $f_s/2$ — Process Gain

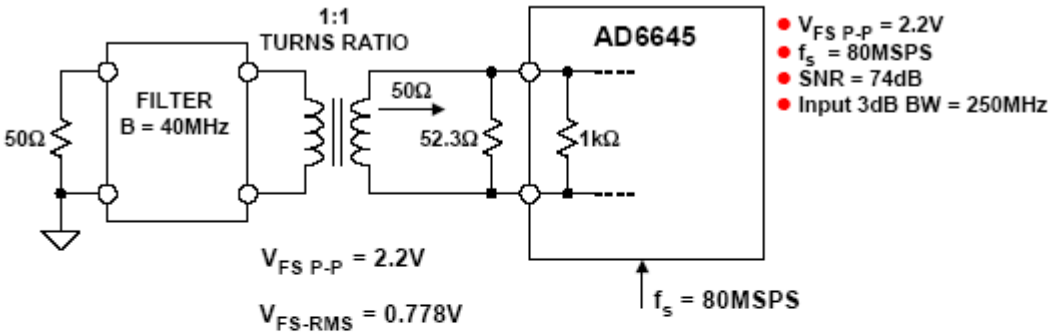
Note: *noise factor* of a device is

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{(G\cdot S_{in})/[G\cdot(N_{in}+N_{dev})]} = 1 + \frac{N_{dev}}{N_{in}} \approx \frac{N_{dev}}{N_{in}} \qquad F >> 1$$

… an ADC does not provide any gain (just numerical quantization)

Although NF is not normally associated with data converter, it can be calculated for a single set of operating conditions.

Figure shows an example NF calculation for the **AD6645** 14-bit, 80-MSPS ADC. A 52.3Ω resistor is added in parallel with the AD6645 input impedance of 1 kΩ to make the net input impedance 50Ω. The ADC is operating under Nyquist conditions, and the SNR of 74 dB is the starting point for the calculations.



$$V_{FS\ P-P} = 2.2V$$

$$V_{FS\text{-}RMS} = 0.778V$$

$$P_{FS} = \frac{(0.778)^2}{50} = 12.1mW$$

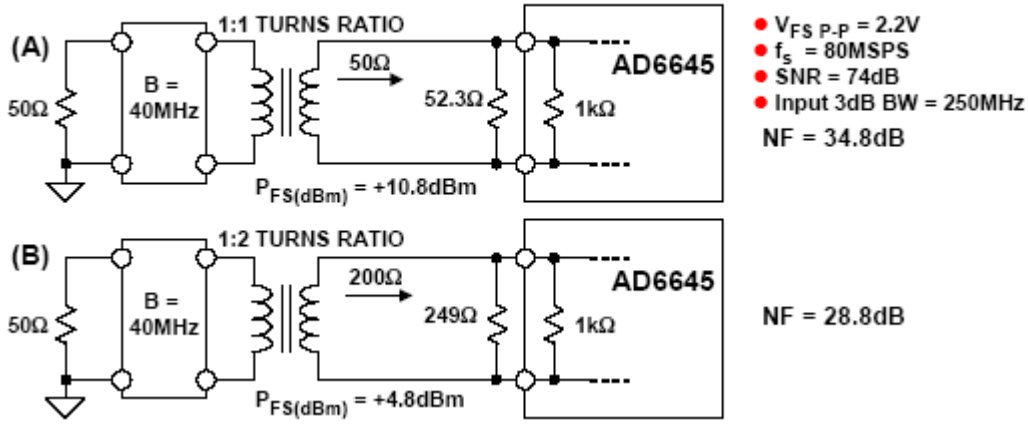
$$P_{FS(dBm)} = +10.8dBm$$

$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B$$

$$= +10.8dBm + 174dBm - 74dB - 10\log_{10}(40 \times 10^6)$$

$$= 34.8dB$$

Using an RF transformer with voltage gain can improve the noise figure. Figure**A** shows a 1:1 turns ratio, and the noise figure is 34.8. Figure**B** shows a transformer with a 1:2 turns ratio. The 249Ω resistor in parallel with the AD6645 internal resistance results in a net input impedance of 200Ω. The noise figure is improved by 6 dB because of the "noise-free" voltage gain of the transformer.



Even with the 1:4 turns ratio transformer, the overall noise figure for the AD6645 was still 22.8 dB, still relatively high by RF standards.

The *solution* is to provide low-noise high-gain stages ahead of the ADC. (It is true that on a stand-alone basis ADCs have relatively high noise figures compared to other RF parts such as LNAs or mixers. In the system the ADC should be preceded with low-noise gain blocks.)