Data Converter Chips

Key:

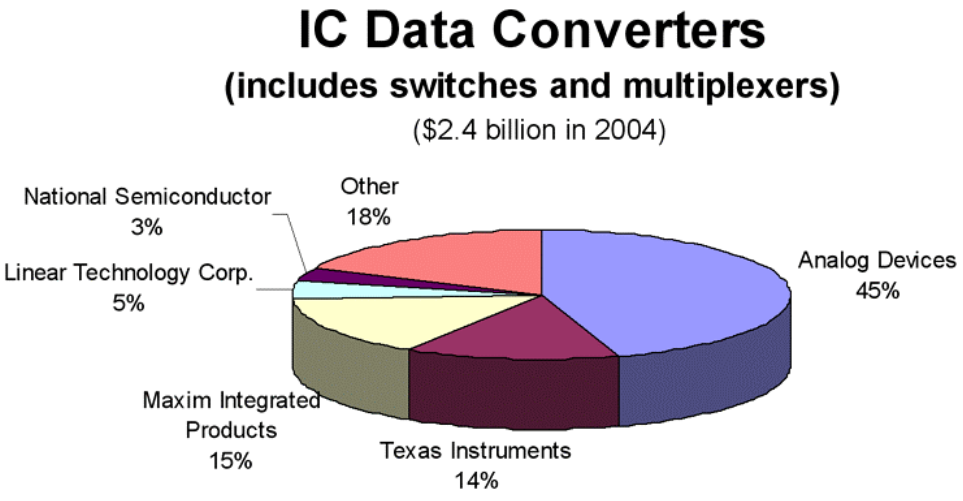
SpecSearch® (searchable catalogs) available in this product category.

Data converter chips transform data (information) from one format to another, such from analog to digital.

Analog-to-Digital Converter Chips (ADC)	**(30 suppliers)** - Analog-to-digital converter chips (ADC) transform information from analog form into digital form.
Codec Chips	**(18 suppliers)** - Codec chips are used to encode and decode (or compress and decompress) various types of data, particularly when the bulk storage is required.
Digital-to-Analog Converters Chips (DAC)	**(30 suppliers)** - Digital-to-analog converters chips (DAC) convert digital signals, representing binary numbers, into proportional analog voltages.

http://cmpmedia.globalspec.com/ProductFinder/Semiconductors_Electronics/Data_Converter_Chips

2005, **April** 13



Source: Gartner Dataquest, April 2005

http://cmpmedia.globalspec.com/LearnMore/Semiconductors/Data_Converter_Chips/Analog_to_Digital_Converter_Chips_ADC

About Analog-to-Digital Converter Chips (ADC)

Analog-to-digital converter chips (ADCs) **transform** information from analog to digital form. ADCs receive analog input, perform calculations on the analog signal, and then digitally encode the output in a format that computerized systems can process. Analog-to-digital converter chips are used in a variety of applications, including **data-acquisition, communications, instrumentation, and signal processing.** To cover a broad range of performance needs, ADCs are available in different resolutions, bandwidths, accuracies, packaging, power requirements, and temperature ranges.

Successive-approximations register (SAR) and flash are two common **architectures** for analog-to-digital converter chips. SAR architecture uses a single comparator and multiple conversion cycles. Flash, or parallel, architecture uses multiple comparators and a single conversion cycle. With flash, ADCs use a set of 2^n-1 comparators to measure an analog signal to a resolution of *n* bits. Consequently, flash ADCs are faster than SAR ADCs, but require a greater number of comparators.

Pipeline architecture overcomes some of the limitations of flash architecture by dividing the conversion task into several consecutive stages. Each stage consists of a sample and hold circuit, an *m*-bit ADC (e.g., a flash converter), and an *m*-bit digital-to-analog converter (DAC). In this way, pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators. However, pipeline analog-to-digital converter chips increase the total conversion time from one cycle to *p* cycles.

Another approach, subranging, combines flash, SAR, and pipeline architectures and breaks *n*-bit conversions into *m*-bit sub-conversions. Like pipeline architecture, subranging consists of several cascading stages, each of which uses a low-resolution analog-to-converter chip to estimate the input and an accurate DAC to convert the output. Subranging also calculates the residue, the difference between the estimated input and the actual output. A gain block is used to amplify and restore the residue to an appropriate level for further estimation by the next stage.

Sigma-delta architecture takes a fundamentally different approach than other ADC architectures. Sigma-delta converters consist of an integrator, a comparator, and a single-bit DAC. The DAC output is subtracted from the input signal, the resulting signal is integrated, and the comparator converts the integrator output voltage to a single-bit digital output (1 or 0). The resulting bit becomes the DAC's input, and the DAC's output is subtracted from the ADC's input signal. With sigma-delta architecture, the digital data from the ADC is a stream of ones and zeros, and the value of the signal is proportional to the density of digital ones from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output.

In terms of **performance**, analog-to-digital converter chips vary according to resolution, sample rate, input voltage range, operating temperature, and a number of other variables. Signal-to-noise (SNR) ratios and signal-to-noise distortion (SINAD) ratios are decibel amounts that represent RMS values for the sine wave f_{IN}. Differential nonliniarity (DNL) errors measure the differences between ideal and measured code transitions for successive ADC codes. DNL errors also measure the difference between ideal and measured output values for successive DAC codes. Integrated non-linearity (INL) is the amount of deviation of the measured transfer function of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) from the ideal transfer function.

General Specifications

Architecture	
Your choices are...	
Flash (Parallel)	The ADC flash architecture uses a set of 2^n-1 comparators to directly measure an analog signal to a resolution of n bits. For a 4-bit flash ADC. For a 4-bit flash ADC, for instance, the analog input is fed into 15 comparators, each of which is biased to compare the input to a discrete transition value. The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators
Pipeline	The ADC pipeline architecture effectively overcomes the limitations of the flash architecture. A pipelined converter divides the conversion task into several consecutive stages. Each of these stages consists of a sample and hold circuit, an *m*-bit ADC (e.g., a flash converter), and an *m*-bit D/A converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The *m*-bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an *m*-bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. Pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of increasing the total conversion time from one cycle to *p* cycles.
Subranging	The subranging architecture is basically a combination of the flash and the successive approximation architectures. It breaks an n-bit conversion into m sub-conversions. Like the pipelined architecture, it consists of several cascaded stages, each of which includes a low-resolution analog-to-digital converter (ADC) to achieve a coarse estimation of the input, an accurate digital-to-analog converter (DAC) to convert the output of the ADC into an analog version of the estimation, a subtractor to get the residue (the difference between the actual output and its estimation), and a gain block to amplify and to restore the residue to an appropriate level for further estimation by the next stage. Basically, a subranging converter is similar to a pipelined converter, but without the sample-and-hold circuit.
SAR	The Successive-Approximations Register (SAR) architecture can be thought of as being at the other end of the spectrum from the flash architecture. While a flash converter uses many comparators to convert in a single cycle, a SAR converter conceptually uses a single comparator over many cycles to make its conversion.
Sigma-Delta	The Sigma-Delta ADC architecture takes a fundamentally different approach from those outlined above. In its most basic form, a sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DACs output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "over sampled" rate. The digital data coming from the ADC is a-stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a

	binary-format output.
Other	Other unlisted, proprietary or specialized converters.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Interface Type	
Your choices are...	
Serial	The output interface is a general serial port.
Parallel	The output interface is a general parallel port.
SPI	The output interface is an SPI (Serial Peripheral Interface) port. SPI was developed by Motorola.
I^2C	Inter-Integrated Circuit (I^2C) bus is a two-wire, low to medium speed, communication bus developed by Philips Semiconductors in the early 1980's.
MICROWIRE™	MICROWIRE™ is a serial protocol created by National Instruments.
Other	Other unlisted, specialized, or proprietary interface type.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Input Type	
Your choices are...	
Single-Ended	Single-ended terminals carry power in one wire and the other wire is grounded.
Differential	Differential terminals carry power in both wires.
Other	Other unlisted or specialized input types.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Number of Inputs	The total number of input channels available in the converter.
Search Logic:	All matching products will have a value greater than or equal to the specified value.

Performance

Resolution	When an analog signal is digitized, it is represented by a finite number of discrete voltage levels. The resolution is the number of discrete levels that are used to represent the signal. To more accurately replicate the analog signal, the resolution must be increased. Resolution is usually defined in bits. Using converters with higher

	resolutions will reduce the quantization error.
Search Logic:	All matching products will have a value greater than or equal to the specified value.
Sample Rate	The rate at which a converter acquires the input signal, digitizes it, and outputs data to the DSP. It is specified in samples per second or Hertz (Hz) and is also referred to as the "throughput rate."
Search Logic:	All matching products will have a value greater than or equal to the specified value.
SNR	Signal-to-noise ratio (SNR) is the RMS value of the sine wave f_{IN} (input sine wave for an ADC, reconstructed output sine wave for a DAC) to the RMS value of the noise of the converter from DC to Nyquist frequency, excluding noise at DC and harmonic distortion content. It is typically expressed in decibels.
Search Logic:	All matching products will have a value greater than or equal to the specified value.
DNL	The Differential Nonliniarity (DNL) error is defined as the difference between the ideal and the measured code transitions for successive codes for an ADC or the difference between the ideal and the measured output value between successive DAC codes.
Search Logic:	All matching products will have a value less than or equal to the specified value.
INL	The Integer Nonliniarity (INL) is the amount of deviation of the measured transfer function of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) from the ideal transfer function (defined as a straight line drawn from zero to full scale). This error is sometimes referred to as static linearity or absolute linearity.
Search Logic:	All matching products will have a value less than or equal to the specified value.
SINAD	Signal-to-noise and distortion ratio (SINAD) is the RMS value of the sine wave f_{IN} (input sine wave for an ADC, reconstructed output sine wave for a DAC) to the RMS value of the noise of the converter from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels.
Search Logic:	All matching products will have a value greater than or equal to the specified value.
SFDR	Spurious Free Dynamic Range (SFDR) is defined as the distance in dB from the fundamental amplitude to the peak spurious component in the output frequency spectrum. The peak spur can be either harmonic or non-harmonic in nature.
Search Logic:	All matching products will have a value greater than or equal to the specified value.
Power Dissipation	The maximum power in watts dissipated by the device.
Search Logic:	All matching products will have a value less than or equal to the specified value.
Input Voltage Range (V_{pp})	The needed input voltage (range) needed to operate the device.
Search Logic:	User may specify either, both, or neither of the limits in a "From - To" range; when both are specified, matching products will cover entire range. Products returned as matches will meet all specified criteria.
Operating Temperature:	This is the full-required range of ambient operating temperature.

Search Logic:	User may specify either, both, or neither of the limits in a "From - To" range; when both are specified, matching products will cover entire range. Products returned as matches will meet all specified criteria.

Reference Access	
Your choices are...	
Internal	The voltage reference is an internal power supply.
External	The voltage reference is supplied by the user.
Other	Other unlisted or proprietary reference access method.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.

Packaging Characteristics

IC Package Type	
Your choices are...	
PBGA	Plastic ball-grid array (PBGA) is the general terminology for the BGA package adopting plastic (epoxy molding compound) as the encapsulation. According to JEDEC standard, PBGA refers to an overall thickness of over 1.7mm.
TBGA	Tape ball-grid array (TBGA) uses a fine, polyimide substrate and provides good thermal performance with high pin counts.
CSP	Chip scale package or chip size package (CSP) has an area that is no more than 20% larger than the built-in die. CSP is compact for second level packaging efficiency and encapsulated for second level reliability. CSP is superior to both direct-chip-attach (DCA) and chip-on-board (COB) technologies. CSP is used in a variety of integrated circuits (IC), including radio frequency ICs (RFIC), memory ICs, and communication ICs.
UCSP	Ultra chip scale package (UCSP).
FLGA	Fine-pitch land-grid array (FLGA) is extremely compact and lightweight, making it suitable for miniature disc drives and digital cameras.
QFP	Quad flat packages (QFP) contain a large number of fine, flexible, gull wing shaped leads. Lead width can be as small as 0.16 mm. Lead pitch is 0.4 mm. QFPs provide good second-level reliability and are used in processors, controllers, ASICs, DSPs, gate arrays, logic, memory ICs, PC chipsets, and other applications.
LFQP	Low quad flat package (LFQP).
TQFP	Thin quad flat package (TQFP).
SOP	Small outline package (SOP).

SOIC	Small outline integrated circuit (SOIC).
TSOP Type I	Thin small outline package (TSOP), Type I is a DRAM package that uses gull wing shaped leads on both sides. TSOP DRAM mounts directly on the surface of the printed circuit board. The advantage of the TSOP package is that it is one-third the thickness of an SOJ package. TSOP components are commonly used in small outline DIMM and credit card memory applications.
TSOP Type II	Thin small outline package (TSOP), Type II is DRAM package that uses gull wing shaped leads on both sides. TSOP DRAM mounts directly on the surface of the printed circuit board. The advantage of the TSOP package is that it is one-third the thickness of an SOJ package. TSOP components are commonly used in small outline DIMM and credit card memory applications.
SSOP	Shrink small outline package (SSOP).
TSSOP	Thin shrink small outline L-leaded package (TSSOP).
VSSOP	Very thin shrink small outline package (VSSOP).
TVSOP	Thin very small outline package (TVSOP).
SOJ	Small outline J-lead (SOJ) is a common form of surface-mount DRAM packaging. It is a rectangular package with J-shaped leads on the two long sides of the device.
HSOF	Small outline flat-leaded package with heat sink (HSOF).
PLCC	Plastic leaded chip carrier (PLCC).
LCCC	Leadless ceramic chip carrier (LCCC).
DIP	Dual in-line package (DIP) is a type of DRAM component packaging. DIPs can be installed either in sockets or permanently soldered into holes extending into the surface of the printed circuit board.
CDIP	Ceramic dual in-line package (CDIP) consists of two pieces of dry pressed ceramic surrounding a "DIP formed" lead frame. The ceramic / LF / ceramic system is held together hermetically by frit glass reflowed at temperatures between 400° - 460° centigrade.
PDIP	Plastic dual in-line package (PDIP) is widely used for low cost, hand-insertion applications including consumer products, automotive devices, logic, memory ICs, micro-controllers, logic and power ICs, video controllers commercial electronics and telecommunications.
SIP	Single in-line package (SIP).
SDIP	Shrink dual in-line package (SDIP).
SZIP	Shrink zigzag in-line package (SZIP).
Other	Other unlisted, specialized, or proprietary packages.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Production Status	

Your choices are...	
Full Production	The device is being manufactured.
Discontinued	The device is no longer available from the manufacturer. The device may still be found in the supply chain.
In Development	The device is in the stages of development.
New Product	The device is new to the market as announced by the manufacturer.
Other	Other unlisted production status.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Screening Level	
Your choices are...	
Commercial	The temperature range supported, and the mechanical and electrical specifications of the device are suitable for commercial applications.
Industrial	The temperature range supported, and the mechanical and electrical specifications of the device are suitable for general industrial applications, such s aeronautical, automotive, medical, and others.
Military	The temperature range supported, and the mechanical and electrical specifications of the device satisfy military standards (MIL-SPEC).
Other	Other unlisted screening levels.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Packing Method	
Your choices are...	
Tape Reel	Method of packing components in a tape system and reeling specified lengths or quantities into a reel for shipping, handling, and configuring for use in industry-standard automated board-assembly equipment.
Tray	The components to be shipped are contained in a try. Normally the tray is designed for components that have leads in four sided (such as QFP or TGFP packages).
Tube	The tube packing method is also known as the stick magazine method. A tube or magazine is used to store and transport electronic components. It is also used to feed components to automatic-placement machines for surface and through-hole board mounting.
Bulk Pack	The devices are distributed as individual parts.
Other	Other unlisted, specialized or proprietary packing method.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving

	all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Pin Count	The number of pins in package.
Search Logic:	User may specify either, both, or neither of the "At Least" and "No More Than" values. Products returned as matches will meet all specified criteria.

Features

Single Supply	The chip can operate with only one supply.
Search Logic:	"Required" and "Must Not Have" criteria limit returned matches as specified. Products with optional attributes will be returned for either choice.
On-Chip ESD Protection	The chip has embedded radiation protection.
Search Logic:	"Required" and "Must Not Have" criteria limit returned matches as specified. Products with optional attributes will be returned for either choice.

http://cmpmedia.globalspec.com/LearnMore/Semiconductors/Data_Converter_Chips/Digital_to_Analog_Converters_Chips_DAC

About Digital-to-Analog Converters Chips (DAC)

Digital-to-analog converter chips (DACs) **transform** information from digital to analog form. They convert signals that have two defined states, on and off, into signals that have a theoretically infinite number of states. For example, modems convert digital computer data that consists of ones and zeroes into audio frequency (AF) tones that can be transmitted over telephone lines. Digital-to-analog converter chips are also used in digital signal processing to improve the intelligibility and fidelity of analog signals. First, analog-to-digital converter chips (ADCs) are used to convert analog signals into digital form. Next, special circuitry is used to improve these signals. Finally, digital-to-analog converter chips are used to transform the digital impulses back into analog form.

There are several **architectures** for digital-to-analog converter chips. Some DACs use a resistive ladder network (R2R) in which each segment consists of two resistors: one with a value of R and one with a value of 2R. Other DACs include a string of resistors, each of which has a value of R. Current steering is an architecture that uses an internal current source to deliver the output current. Sigma-delta architecture takes a fundamentally different approach. In their most basic form, sigma-delta converters consist of an integrator, a comparator, and a single-bit DAC. The output of the digital-to-analog converter is subtracted from the input signal. The resulting signal is integrated, and the output voltage is converted to a single-bit digital output by the comparator. The resulting bit becomes the input to the DAC, and the output is subtracted from the input signal.

Performance specifications for digital-to-analog converter chips include resolution, settling time, differential nonlinearity (DNL), integral nonlinearity (INL), power dissipation, reference access, and special features. Resolution measures the number of discrete levels used to represent a signal and is usually defined in bits. Settling time is the time required for an output to approach a final value within the limits of a defined error band. The DNL error is the difference between the ideal and measured output values for successive DAC codes. The INL error is the amount that a measured transfer function deviates from an ideal transfer function as defined in a straight line drawn from zero to full scale. Power dissipation is the maximum number of watts that the device dissipates. Reference access indicates whether the voltage reference is an internal power supply, or the user supplies the voltage reference. Special features include rail-to-rail outputs, single supply, and on-chip electrostatic discharge (ESD) protection.

Digital-to-analog converter chips are available in a variety of integrated circuit (IC) package types. Basic types include ball grid array (BGA), quad flat package (QFP), single in-line package (SIP), and dual in-line package (DIP). Many packaging variants are available. For example, BGA variants include plastic-ball grid array (PBGA) and tape-ball grid array (TBGA). QFP variants include low-profile quad flat package (LQFP) and thin quad flat package (TQFP). DIPs are available in either ceramic (CDIP) or plastic (PDIP). Other IC package types for digital-to-analog converter chips include small outline package (SOP), thin small outline package (TSOP), and shrink small outline package (SSOP).

General Specifications

Architecture	
Your choices are...	
R-2R	Digital-to-analog converters use a resistive ladder network to produce the transfer function of the DAC. Each segment of the ladder consists on a resistor of value R and a resistor of value 2R.
Resistor String	A DAC that uses string of resistors, each of value R, to produce the conversion.
Current-Steering	A type of DAC architecture that uses an internal current source to deliver the output current.
Sigma-Delta	The Sigma-Delta ADC architecture takes a fundamentally different approach from those outlined above. In its most basic form, a sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DACs output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "over sampled" rate. The digital data coming from the ADC is a-stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output.
Other	Other unlisted, proprietary or specialized converters.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Interface Type	
Your choices are...	
Serial	The output interface is a general serial port.
Parallel	The output interface is a general parallel port.
SPI	The output interface is an SPI (Serial Peripheral Interface) port. SPI was developed by Motorola.
I^2C	Inter-Integrated Circuit (I^2C) bus is a two-wire, low to medium speed, communication bus developed by Philips Semiconductors in the early 1980's.
Microwire	MICROWIRE™ is a serial protocol created by National Instruments.
Other	Other unlisted, specialized, or proprietary interface type.

Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Output Type	
Your choices are...	
Voltage	The DAC produces a voltage as the analog output.
Current	The DAC produces a current as the analog output.
Other	Other unlisted output types.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Number of Outputs	The total number of output channels available in the converter.
Search Logic:	All matching products will have a value greater than or equal to the specified value.

Performance

Resolution	When an analog signal is digitized, it is represented by a finite number of discrete voltage levels. The resolution is the number of discrete levels that are used to represent the signal. To more accurately replicate the analog signal, the resolution must be increased. Resolution is usually defined in bits. Using converters with higher resolutions will reduce the quantization error.
Search Logic:	All matching products will have a value greater than or equal to the specified value.
Settling Time	Settling Time is the time required for the output to approach a final value within the limits of a defined error band, for a step change in the digital input.
Search Logic:	All matching products will have a value less than or equal to the specified value.
DNL	The Differential Nonliniarity (DNL) error is defined as the difference between the ideal and the measured code transitions for successive codes for an ADC or the difference between the ideal and the measured output value between successive DAC codes.
Search Logic:	All matching products will have a value less than or equal to the specified value.
INL	The amount of deviation of the measured transfer function of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) from the ideal transfer function (defined as a straight line drawn from zero to full scale). This error is sometimes referred to as static linearity or absolute linearity.
Search Logic:	All matching products will have a value less than or equal to the specified value.
Power Dissipation	The maximum power in watts dissipated by the device.
Search Logic:	All matching products will have a value less than or equal to the specified value.

Reference Access	
Your choices are...	
Internal	The voltage reference is an internal power supply.
External	The user supplies the voltage reference.
Other	Other unlisted or proprietary reference access method.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Operating Temperature:	This is the full-required range of ambient operating temperature.
Search Logic:	User may specify either, both, or neither of the limits in a "From - To" range; when both are specified, matching products will cover entire range. Products returned as matches will meet all specified criteria.

Packaging Characteristics

IC Package Type	
Your choices are...	
PBGA	Plastic ball-grid array (PBGA) is the general terminology for the BGA package adopting plastic (epoxy molding compound) as the encapsulation. According to JEDEC standard, PBGA refers to an overall thickness of over 1.7mm.
TBGA	Tape ball-grid array (TBGA) uses a fine, polyimide substrate and provides good thermal performance with high pin counts.
CSP	Chip scale package or chip size package (CSP) has an area that is no more than 20% larger than the built-in die. CSP is compact for second level packaging efficiency and encapsulated for second level reliability. CSP is superior to both direct-chip-attach (DCA) and chip-on-board (COB) technologies. CSP is used in a variety of integrated circuits (IC), including radio frequency ICs (RFIC), memory ICs, and communication ICs.
UCSP	Ultra chip scale package (UCSP).
FLGA	Fine-pitch land-grid array (FLGA) is extremely compact and lightweight, making it suitable for miniature disc drives and digital cameras.
QFP	Quad flat packages (QFP) contain a large number of fine, flexible, gull wing shaped leads. Lead width can be as small as 0.16 mm. Lead pitch is 0.4 mm. QFPs provide good second-level reliability and are used in processors, controllers, ASICs, DSPs, gate arrays, logic, memory ICs, PC chipsets, and other applications.
LQFP	Low quad flat package (LQFP).

TQFP	Thin quad flat package (TQFP).
SOP	Small outline package (SOP).
SOIC	Small outline integrated circuit (SOIC).
TSOP Type I	Thin small outline package (TSOP), Type I is a DRAM package that uses gull wing shaped leads on both sides. TSOP DRAM mounts directly on the surface of the printed circuit board. The advantage of the TSOP package is that it is one-third the thickness of an SOJ package. TSOP components are commonly used in small outline DIMM and credit card memory applications.
TSOP Type II	Thin small outline package (TSOP), Type II is a DRAM package that uses gull wing shaped leads on both sides. TSOP DRAM mounts directly on the surface of the printed circuit board. The advantage of the TSOP package is that it is one-third the thickness of an SOJ package. TSOP components are commonly used in small outline DIMM and credit card memory applications.
SSOP	Shrink small outline package (SSOP).
TSSOP	Thin shrink small outline L-leaded package (TSSOP).
VSSOP	Very thin shrink small outline package (VSSOP).
TVSOP	Thin very small outline package (TVSOP).
SOJ	Small outline J-lead (SOJ) is a common form of surface-mount DRAM packaging. It is a rectangular package with J-shaped leads on the two long sides of the device.
HSOF	Small outline flat-leaded package with heat sink (HSOF).
PLCC	Plastic leaded chip carrier (PLCC).
LCCC	Leadless ceramic chip carrier (LCCC).
DIP	Dual in-line package (DIP) is a type of DRAM component packaging. DIPs can be installed either in sockets or permanently soldered into holes extending into the surface of the printed circuit board.
CDIP	Ceramic dual in-line package (CDIP) consists of two pieces of dry pressed ceramic surrounding a "DIP formed" lead frame. The ceramic / LF / ceramic system is held together hermetically by frit glass reflowed at temperatures between 400° - 460° centigrade.
PDIP	Plastic dual in-line package (PDIP) is widely used for low cost, hand-insertion applications including consumer products, automotive devices, logic, memory ICs, micro-controllers, logic and power ICs, video controllers commercial electronics and telecommunications.
SIP	Single in-line package (SIP).
SDIP	Shrink dual in-line package (SDIP).
SZIP	Shrink zigzag in-line package (SZIP).
Other	Other unlisted, specialized, or proprietary IC packages.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all

	attribute options will be returned as matches.
Production Status	
Your choices are...	
Full Production	The device is being manufactured.
Discontinued	The device is no longer available from the manufacturer. The device may still be found in the supply chain.
In Development	The device is in the stages of development.
New Product	The device is new to the market as announced by the manufacturer.
Other	Other unlisted production status.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Screening Level	
Your choices are...	
Commercial	The temperature range supported, and the mechanical and electrical specifications of the device are suitable for commercial applications.
Industrial	The temperature range supported, and the mechanical and electrical specifications of the device are suitable for general industrial applications, such s aeronautical, automotive, medical, and others.
Military	The temperature range supported, and the mechanical and electrical specifications of the device satisfy military standards.
Other	Other unlisted screening levels.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Packing Method	
Your choices are...	
Tape Reel	Method of packing components in a tape system and reeling specified lengths or quantities into a reel for shipping, handling, and configuring for use in industry-standard automated board-assembly equipment.
Tray	The components to be shipped are contained in a try. Normally the tray is designed for components that have leads in four sided (such as QFP or TGFP packages).
Tube	The tube packing method is also known as the stick magazine method. A tube or magazine is used to store and transport electronic components. It is also used to feed components to automatic-placement machines for surface and through-hole board mounting.

Bulk Pack	The devices are distributed as individual parts.
Other	Other unlisted, specialized or proprietary packing method.
Search Logic:	All products with ANY of the selected attributes will be returned as matches. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches.
Pin Count	The number of pins in package.
Search Logic:	User may specify either, both, or neither of the "At Least" and "No More Than" values. Products returned as matches will meet all specified criteria.

Features

Rail-to-Rail Output	The output voltage swing is from the negative to the positive value of the reference voltage.
Search Logic:	"Required" and "Must Not Have" criteria limit returned matches as specified. Products with optional attributes will be returned for either choice.
Single Supply	The chip can operate with only one supply.
Search Logic:	"Required" and "Must Not Have" criteria limit returned matches as specified. Products with optional attributes will be returned for either choice.
On-Chip ESD Protection	The chip has embedded radiation protection.
Search Logic:	"Required" and "Must Not Have" criteria limit returned matches as specified. Products with optional attributes will be returned for either choice.