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ANALOG-DIGITAL CONVERSION

Walt Kester
Editor

ANALOG DEVICES

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FUNDAMENTALS OF SAMPLED DATA SYSTEMS
2.3 DATA CONVERTER AC ERRORS

The effects of aperture and sampling clock jitter on an ideal ADCs SNR can be predicted by the following simple analysis. Assume an input signal given by

$$v(t) = V_O \sin 2\pi ft \qquad \text{Eq. 2.29}$$

The rate of change of this signal is given by:

$$dv/dt = 2\pi fV_O \cos 2\pi ft. \qquad \text{Eq. 2.30}$$

The rms value of dv/dt can be obtained by dividing the amplitude, $2\pi fV_O$, by $\sqrt{2}$:

$$dv/dt|_{rms} = 2\pi fV_O / \sqrt{2}. \qquad \text{Eq. 2.31}$$

Now let Δv_{rms} = the rms voltage error and Δt = the rms aperture jitter t_j, and substitute:

$$\Delta v_{rms} / t_j = 2\pi fV_O / \sqrt{2}. \qquad \text{Eq. 2.32}$$

Solving for Δv_{rms}:

$$\Delta v_{rms} = 2\pi fV_O t_j / \sqrt{2}. \qquad \text{Eq. 2.33}$$

The rms value of the full-scale input sinewave is $V_O/\sqrt{2}$, therefore the rms signal to rms noise ratio is given by

$$SNR = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{\Delta v_{rms}}\right] = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{2\pi fV_O t_j/\sqrt{2}}\right] = 20\log_{10}\left[\frac{1}{2\pi f\, t_j}\right]. \qquad \text{Eq. 2.34}$$

This equation assumes an infinite resolution ADC where aperture jitter is the only factor in determining the SNR. This equation is plotted in Figure 2.80 and shows the serious effects of aperture and sampling clock jitter on SNR, especially at higher input/output frequencies. Therefore, extreme care must be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system.

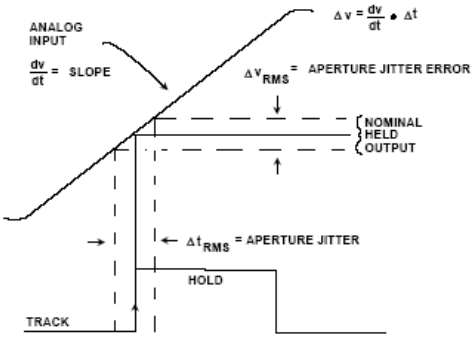

Figure 2.79: Effects of Aperture Jitter and Sampling Clock Jitter

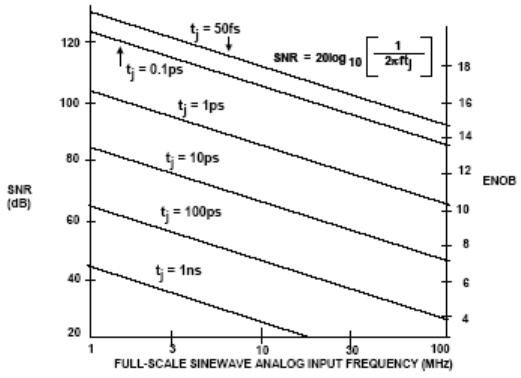

Figure 2.80: Theoretical SNR and ENOB Due to Jitter vs. Fullscale Sinewave Input Frequency

Note: The effects of phase jitter on the external sampling clock (or the analog input for that matter) produce exactly the same type of error.

Clocking high-speed data converters

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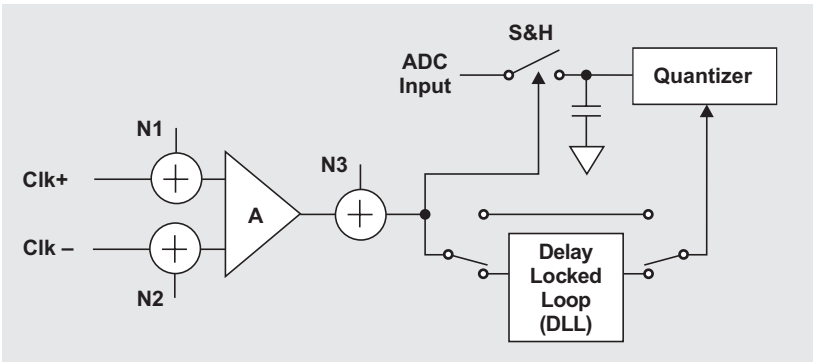
Introduction

In circuit design that involves the use of a high-performance, high-speed analog-to-digital converter (ADC) such as the ADS5500, one of the main careabouts is the clocking scheme. Questions about the type of clock to be used (sinusoidal or square), the voltage levels, or the jitter are common. The purpose of this article is to explain the general theory to support the circuit designer in making the right choices.

Figure 1 shows a simplified model of the clock circuit inside a high-speed ADC like the ADS5500. Although not all ADCs have exactly the same internal blocks in their clock distribution, this diagram can be modified to fit your particular ADC. Since nowadays most of the circuits sold as ADCs include a front sample-and-hold (S&H), for the purpose of this article we will differentiate between them. The circuit that takes an instantaneous analog snapshot of the input signal will be called the S&H; and the ADC itself, which converts the analog value being held by the S&H into quantized digital output, will be called the quantizer. Analyzing what parameters of the internal clock are important for these two circuits will help us understand the main careabouts in our external clock design.

Figure 1. Simplified model of clock circuit in high-speed ADC

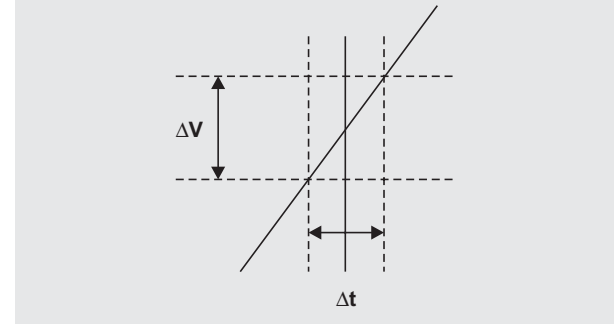


Errors in the sampling instant

The conversion process starts when a clock signal tells the S&H to take the sample. Up to that instant, the internal switch on the S&H circuit has been closed, allowing the voltage across the capacitor to track the input signal (which is why other literature more properly calls this circuit "track and hold"). One of the edges of the input clock then indicates when to open this switch, and the capacitor holds the voltage at that instant in time. This instant is represented in Figure 2 by a vertical solid line. Any error in that instant (Δt) will translate as an error in voltage (ΔV) dependent on the input signal slope. The error in that instant is what we will call jitter.

A mathematical estimation of the best-case signal-to-noise ratio (SNR) (without other noise sources), given a certain amount of jitter, can be extracted from Figure 2. Given a sinusoidal input of amplitude A and frequency f_{IN} (1/T), the uncertainty of the sampled voltage at a given point will be proportional to the slope of the input signal at that instant and to the uncertainty of the sampling instant (jitter, which is the rms value of that variation,

Figure 2. Voltage error relation to sampling jitter



uncorrelated with the input level). The total uncertainty is the addition of all the uncertainties at each point of the sinusoid weighted by the probability of sampling each of the points:

$$\sigma^2_{Jitter} = \frac{1}{T}\int_0^T \left(Slope(\tau)\times Jitter\right)^2 d\tau = \frac{1}{T}\int_0^T \left[\frac{d\left(A\sin\frac{2\pi\tau}{T}\right)}{d\tau} Jitter\right]^2 d\tau$$

$$= \frac{1}{T} Jitter^2 \int_0^T \left(\frac{2\pi A\cos\frac{2\pi\tau}{T}}{T}\right)^2 d\tau = \left\langle a = \frac{2\pi\tau}{T}, \frac{da}{d\tau} = \frac{2\pi}{T}\right\rangle$$

$$= \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\int_0^{2\pi} (\cos^2 a)da = \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\frac{1}{2}(a+\sin a\times\cos a)\Big|_0^{2\pi}$$

$$= \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\pi = \frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2$$

The theoretical limitation of the SNR due to jitter is given by

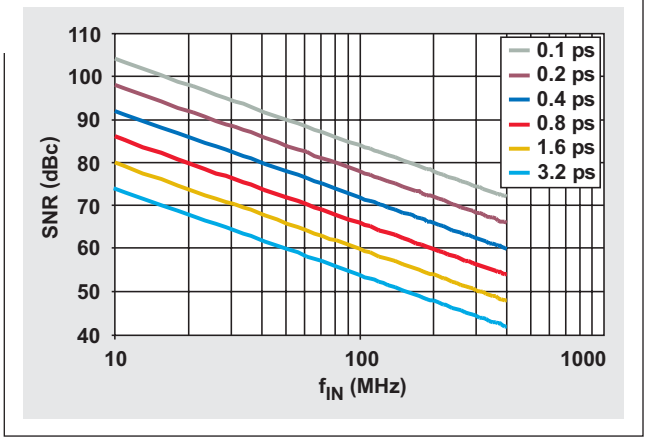
$$SNR\,(dBc) = \frac{S}{N} = 10\log_{10}\left[\frac{\frac{A^2}{2}}{\frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2}\right] = -20\log_{10}(2\pi f_{IN}\,Jitter). \quad \textbf{(1)}$$

Figure 3 shows this limitation as a function of the input frequency.

Observe that increasing or decreasing the input amplitude (A_{IN}) has no effect on the SNR component coming from jitter. In other words, as we decrease the input amplitude, the amount of error due to the jitter also becomes smaller. Nevertheless, there are other sources of error, like thermal noise, that do not get smaller. Assuming all these sources of noise are uncorrelated, the total noise is the addition of a noise term independent of input frequency and a noise term dependent on input frequency (jitter):

$$SNR\,(dBc) = 10\log_{10}\left[\frac{\left(\frac{A}{\sqrt{2}}\right)^2}{Thermal + Quantization + \frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2}\right] \quad \textbf{(2)}$$

Figure 3. Limitation of the SNR due to jitter as a function of input frequency



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Alfio Zanchi,

and Frank (Ching-Yuh) Tsay,

A 16-bit 65-MS/s ADC Core ...

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The SNR limitation from jitter can be calculated via the classic formula

$$\begin{aligned}\mathrm{SNR}_{\mathrm{jitter}} &= 10\cdot\log_{10}\left(\frac{P_{\mathrm{IN}}}{\sigma^2_{V\,\mathrm{jitter}}}\right)\\ &= 10\cdot\log_{10}\left(\frac{P_{\mathrm{IN}}}{\frac{\sigma_T^2}{2}(A_{\mathrm{IN}}\omega_{\mathrm{IN}})^2}\right)\\ &= -20\cdot\log_{10}(2\pi f_{\mathrm{IN}}\sigma_T) \qquad (8)\end{aligned}$$

a mathematical justification of which was published in [17]. Although intuitive, such a derivation is still heuristic. A more rigorous demonstration is found in the probabilistic theorv. and for sake of clarity is reported in the Appendix

Appendix

In the following, we introduce a mathematically rigorous derivation of the popular formula used to determine the SNR limitation introduced by the random occurrence of the sampling clock edge. Given a sinusoidal input of amplitude A_{IN} and angular frequency ω_{IN} ($\omega_{\mathrm{IN}} = 2\pi f_{\mathrm{IN}}$)

$$V_{\mathrm{IN}}(t) = A_{\mathrm{IN}}\sin(\omega_{\mathrm{IN}}t) \qquad (11)$$

the jitter affecting the sampling clock cycle (expressed via the RMS timing error σ_T) induces a theoretical RMS voltage error $\sigma_{V\,\mathrm{jitter}}$ dependent on the input waveform slope, and calculated by means of the formula

$$\sigma_{V\,\mathrm{jitter}} = \sigma_T\cdot\left|\frac{dV_{\mathrm{IN}}(t)}{dt}\right| = \sigma_T\cdot A_{\mathrm{IN}}\omega_{\mathrm{IN}}\cdot|\cos(\omega_{\mathrm{IN}}t)|. \qquad (12)$$

Equation (12) translates into math the intuitive concept that little or no error is introduced by a jittery sampling instant when the input sinusoid is sampled at its peak, but uncertainty in the aperture time causes substantial noise in the sampled voltage when the input sinusoid is close to zero-crossing. Let us now consider the voltage noise stochastic process $n_{V\,\mathrm{jitter}}$ engendered by the uncertainty σ_T affecting the sampling instants of $V_{\mathrm{IN}}(t)$. Its power can be computed as

$$\sigma^2_{V\,\mathrm{jitter}} = \langle n^2_{V\,\mathrm{jitter}}\rangle = \int_{-A_{\mathrm{IN}}}^{+A_{\mathrm{IN}}} n^2_{V\,\mathrm{jitter}}\cdot\mathrm{pdf}(V_{\mathrm{IN}})\,dV_{\mathrm{IN}} \qquad (13)$$

according to the most general definition of variance as *ensemble average*. In (13) the effective noise power is weighted by the probability density function $\mathrm{pdf}(V_{\mathrm{IN}})$, accounting for the probability of the noise having a specific value. The expression is then integrated over the whole range of possible noisy voltages (the input peak-to-peak). The procedure is analogous to the well-known calculation of the quantization noise $\langle n_q^2\rangle = q^2/12$ for a quantization cell of width q with uniform distribution.

For the single-tone tests universally adopted to assess the ADC performance, the weight function is the pdf of a sinusoid. The probability of the input voltage being at level V_{IN} is given by the familiar "bathtub" expression (see for instance [24])

$$\mathrm{pdf}(V_{\mathrm{IN}}) = \frac{1}{A_{\mathrm{IN}}\pi\sqrt{1-\left(\frac{V_{\mathrm{IN}}}{A_{\mathrm{IN}}}\right)^2}}. \qquad (14)$$

The equation for $n_{V\,\mathrm{jitter}}$ as a function of time t is formally identical to (12)

$$\begin{aligned}n_{V\,\mathrm{jitter}}(t) &= n_T(t)\cdot\left|\frac{dV_{\mathrm{IN}}(t)}{dt}\right|\\ &= n_T(t)\cdot A_{\mathrm{IN}}\omega_{\mathrm{IN}}\cdot\cos(\omega_{\mathrm{IN}}t). \qquad (15)\end{aligned}$$

Hence, by combining (13) and (14) it can be written

$$\begin{aligned}&\sigma^2_{V\,\mathrm{jitter}}\\ &= \langle n^2_{V\,\mathrm{jitter}}(t)\rangle = \int_{-A_{\mathrm{IN}}}^{+A_{\mathrm{IN}}}[n_T(t)\cdot A_{\mathrm{IN}}\omega_{\mathrm{IN}}\cdot\cos(\omega_{\mathrm{IN}}t)]^2\\ &\quad\cdot\frac{1}{A_{\mathrm{IN}}\pi\sqrt{1-\left(\frac{V_{\mathrm{IN}}}{A_{\mathrm{IN}}}\right)^2}}\,dV_{\mathrm{IN}}\\ &= \langle n_T^2(t)\rangle\cdot(A_{\mathrm{IN}}\omega_{\mathrm{IN}})^2\cdot\int_{-A_{\mathrm{IN}}}^{+A_{\mathrm{IN}}}\cos^2(\omega_{\mathrm{IN}}t)\\ &\quad\cdot\frac{1}{\pi\sqrt{1-\left(\frac{V_{\mathrm{IN}}}{A_{\mathrm{IN}}}\right)^2}}\frac{dV_{\mathrm{IN}}}{A_{\mathrm{IN}}}. \qquad (16)\end{aligned}$$

The ensemble average of the clock jitter process $n_T(t)$ is σ_T^2, and can be taken out of the integral as long as the clock edge uncertainty is independent from the input amplitude, as is commonly postulated. In reality, to a degree the MOSFET sampling switch will introduce deviations from this idealized behavior. The variable t is now to be expressed in terms of the voltage V_{IN}. From (11), it is

$$\omega_{\mathrm{IN}}t = \arcsin\left(\frac{V_{\mathrm{IN}}}{A_{\mathrm{IN}}}\right). \qquad (17)$$

Therefore, as needed in order to rewrite (16)

$$\cos(\omega_{\mathrm{IN}}t) = \cos\left(\arcsin\left(\frac{V_{\mathrm{IN}}}{A_{\mathrm{IN}}}\right)\right) \qquad (18)$$

where the latter is a measure of the sensitivity of a sample taken from a sinusoidal input, to the aperture jitter affecting the SHA clock edge. Not surprisingly, (14) along with (18) highlight how the input roams the most where the jitter is less of a problem.

Finally, substituting $x = V_{IN}/A_{IN}$ for sake of simplicity, the expression in (16) becomes

$$\sigma^2_{V\,\text{jitter}} = (\sigma_T \cdot A_{IN}\omega_{IN})^2 \cdot \int_{-1}^{+1} \cos^2(\arcsin(x)) \cdot \frac{1}{\pi\sqrt{1-x^2}}\,dx \quad (19)$$

where the second member can be easily calculated with Maple and is indeed equal to $1/2$. Considering that the probe tone power is given by $A^2_{IN}/2$, (8) for the $\text{SNR}_{\text{jitter}}$ is finally derived.

In conclusion, the rigorous statistical calculation justifies the well-known formula linking SNR to the clock jitter in absence of other noise additions, which had been formerly devised in [17] on a more heuristic basis.

[17] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, Feb. 1990.

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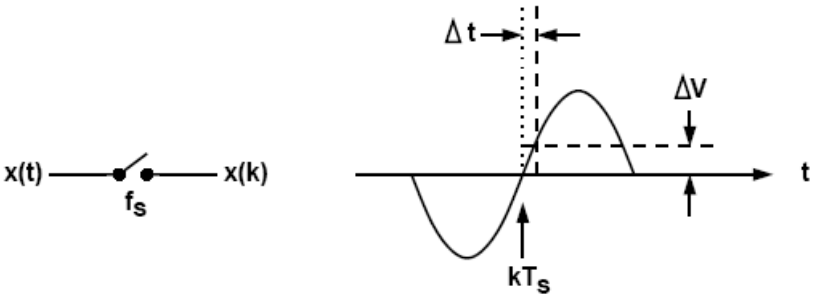
Jieh-Tsorng Wu

Sampling-Time Uncertainty (Aperture Jitter)



$$x(k) = x\,(kT_s + \Delta t) \qquad T_s = \frac{1}{f_s}$$

Let $x(t) = \frac{1}{2}A_{FS}\sin(2\pi f_i t)$ and Δt be a random variable, then

$$x(k) = x\,(kT_s + \Delta t) \approx \frac{1}{2}A_{FS}\sin(2\pi f_i kT_s) + \left.\frac{dx(t)}{dt}\right|_{t=kT_s} \times \Delta t$$

$$\approx \frac{1}{2}A_{FS}\sin(2\pi f_i kT_s) + A_{FS}\pi f_i \cos(2\pi f_i kT_s) \times \Delta t$$

$$\overline{x^2(k)} = \frac{1}{8}A^2_{FS} + \frac{1}{2}A^2_{FS}\pi^2 f_i^2 \times \overline{\Delta t^2} = P_s + P_n$$

The signal-to-noise ratio of $x(k)$ is

$$\text{SNR} = \frac{P_s}{P_n} = \frac{1}{4\pi^2 f_i^2 \cdot \overline{\Delta t^2}} = -20\log(2\pi f_i \cdot \Delta t_{\text{rms}})\ \text{dB}$$

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❺ Little Known Characteristics of Phase Noise

by Paul Smith

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PHASE JITTER IN SAMPLED DATA SYSTEMS

The easiest way to calculate the SNR degradations incurred by phase noise in a sampled data system is to convert phase noise to phase jitter. This is most easily accomplished by recognizing that a time delay is the same as a phase delay at a given frequency. Extending this concept and writing it in terms of noise power yields Equation 1.

$$\sigma_\theta^2 = \omega_{clk}^2 \sigma_t^2,$$

where σ_θ = *phase noise in rms radians*
σ_t = *phase jitter in rms seconds*
ω_{clk} = *clock frequency in radians/sec* (1)

That is, for a given jitter error, a higher frequency signal will have more phase error. The term σ_θ is the total integrated phase noise of the clock[4] and defines the clock SNR by

$$SNR_{clk}(dB) = -10\log\left(\sigma_\theta^2\right) \quad (2)$$

Thus, Equation 1 relates the total integrated phase noise, or clock SNR, to the total jitter in the clock. Phase noise and clock jitter are two different ways to look at the same phenomenon.

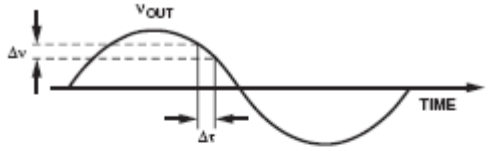

Figure 1.

Traditional sampled data SNR analyses use Figure 1 as an aid to determine how noise on a clock generates an error in the sampled data. From this it is seen that

$$\Delta v(t) = \Delta t \times v'_{out}(t)$$
$$E\left\{\Delta v^2(t)\right\} = E\left\{\Delta t^2 \times v'_{out}{}^2(t)\right\}$$
$$E\left\{\Delta v^2(t)\right\} = E\left\{\Delta t^2\right\} \times E\left\{v'_{out}{}^2(t)\right\},$$

zero mean, independence

Therefore,

$$\sigma_{err}^2 = \sigma_t^2 \times E\left\{v'_{out}{}^2(t)\right\},$$

where σ_t^2 is in $(\text{rms seconds})^2$

From this it is seen that the noise power is a function of the jitter power and the power in the signal derivative.

The SNR of a signal sampled with a jittery clock is defined as

$$SNR_{sig} = \frac{\text{power in signal}}{\text{power in noise}} = \frac{\sigma_{out}^2}{\sigma_{err}^2} = \frac{1}{\sigma_t^2}\frac{E\left\{v_{out}{}^2(t)\right\}}{E\left\{v'_{out}{}^2(t)\right\}} \quad (3)$$

For example, in a single sine wave,

$$v_{out}(t) = A\sin\omega_O t$$
$$v'_{out}(t) = A\,\omega_O\cos\omega_O t$$

Therefore,

$$E\left\{v_{out}{}^2(t)\right\} = \text{power in } v_{out}(t) = \frac{A^2}{2}$$
$$E\left\{v'_{out}{}^2(t)\right\} = \text{power in } v'_{out}(t) = \frac{\omega_O^2 A^2}{2}$$

Using Equation 3,

$$SNR_{sig} = \frac{1}{\sigma_t^2}\frac{\frac{A^2}{2}}{\frac{\omega_O^2 A^2}{2}} = \frac{1}{\sigma_t^2}\frac{1}{\omega_O^2} \quad (4a)$$

$$SNR_{sig} = \frac{1}{4\pi^2 f_O^2 \sigma_t^2}, \text{for a single carrier system.} \quad (4b)$$

This is the standard SNR equation for a single sine wave sampled by a clock with jitter and can be found in many publications[5]. Intuitively what is happening is that higher frequency signals have larger slew rates. This results in larger voltage changes as the sample time changes. It should be remembered that quantization noise and thermal noise must also be added to this to obtain the total noise out of a data converter.

[4]"VCO Phase Noise," Mini-Circuits, Application Note #2.
[5]"Linear Design Seminar," Analog Devices, Inc., Norwood, MA, 1995, pp. 5-20.

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Effect of Jitter on Asynchronous Sampling With Finite Number of Samples

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Usually, the jitter requirements of the frequency synthesizers that provide the sampling clock to the ADC is determined at system level by using the following expression for sinusoidal signals

$$\mathrm{SNR} = 20\log_{10}\left(\frac{1}{2\pi f_{\mathrm{sig}}\cdot\sigma_{\mathrm{tj}}}\right) \tag{1}$$

or its extension valid for any kind of signal [1]

$$\mathrm{SNR} = 10\log_{10}\left(\frac{r_x(0)}{-r_x''(0)\cdot\sigma_{\mathrm{tj}}^2}\right) \tag{2}$$

where x is the analog signal to be sampled (assumed to be wide sense stationary and with zero mean), r_x is its autocorrelation function (the prime denotes the derivative) and σ_{tj} is the long term jitter (as defined in [1]) divided by $\sqrt{2}$. This expression is derived from statistical considerations, assuming the evaluation of the SNR is performed on an infinite number of samples.

[1] N. Da Dalt, M. Harteneck, C. Sandner, and A. Wiesbauer, "On the jitter requirements of the sampling clock for analog to digital converters," *IEEE Trans. Circuits Syst. I*, vol. 49, pp. 1354–1360, Sept. 2002.

A. Sinusoidal Input

As application of the relationship (2), the SNR in case of sinusoidal input is calculated. Assuming $x(t) = A\cdot\sin(\omega t)$, the autocorrelation function is

$$r_x(mT) = \frac{A^2}{2}\cos(\omega mT)$$

and the second derivative is

$$r_x''(mT) = \frac{-\omega^2 A^2}{2}\cos(\omega mT).$$

By substitution in (2), it is easy to find the well-known formula [2] for the aperture jitter SNR in sampling of sinusoidal signals

$$\mathrm{SNR} = 20\cdot\log_{10}\left(\frac{1}{\omega\sigma_{tj}}\right)\ \mathrm{dB}.$$

❼ Jitter is critical in high-performance data converters

- 0.3ps rms can be considered as "bad" for ADS55XX
- ADC applications require 2-3 orders of magnitude better jitter than high-speed digital applications

Jitter noise can exceed quantization noise

- Quantization noise of an N-bit ADC

$$SNR\max_{quantization} = 6.02 * N + 1.76$$

- Jitter noise of an N-bit ADC

$$SNR\max_{jitter} = -20\log(2\pi f \varepsilon)$$

- Find 'quantization noise equivalent' jitter

$$\varepsilon < \frac{1}{2\pi f 10^{0.3N}},$$

$f = input\_frequency$

$\varepsilon = rms\_jitter$

Jitter Tolerance of Nyquist ADCs (ps rms)

Fin	8bit	10bit	12bit	14bit	16bit	18bit	20bit	22bit	24bit
10KHz	64512	16128	4032	1008	252	63	16	4	1
100KHz	6451	1612	403	101	25.2	6.3	1.6	0.4	0.1
1MHz	645	161	40.3	10.1	2.52	0.63	0.16	0.04	0.01
10MHz	64	16.1	4.03	1.01	0.252	0.06	0.01	0.00	0.00
100MHz	6.4	1.61	0.40	0.10	0.025	0.006	0.00	0.00	0.00

[T. Kuyel, 2005]