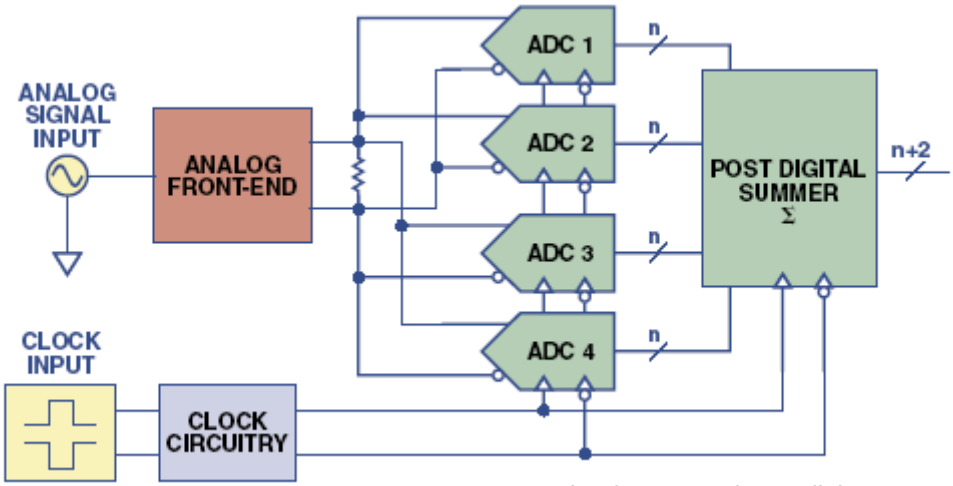
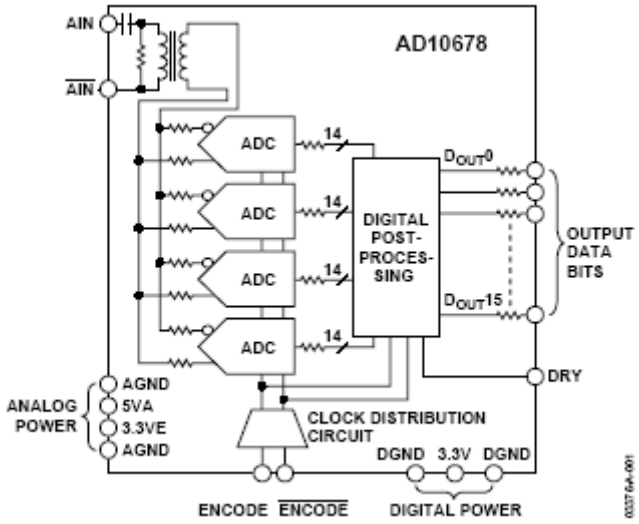
1. *Signal averaging* - for increased **resolution** without loss of speed:

The signals add directly, while noise from the individual ADCs - assumed to be uncorrelated - sums as the RSS (*root-sum-square*), so summing *improves* the **overall SNR**



Summing four ADCs in parallel

AD10678 Specifications	
Res (Bits)	16bit
Thruput Rate	80MSPS
# of ADC Inputs	1
Supply V	Multi (+3.3, +5)
Pwr Diss (max)	8W
Interface	Par
Ain Range	2.15 V p-p
SNR (dB)	80.5dB

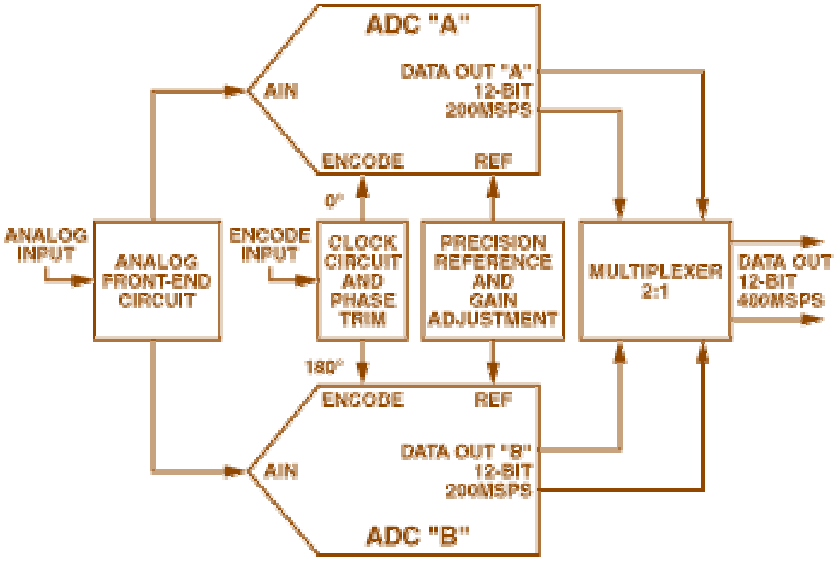


The AD10678 integrates *four* AD6645s, a clock distribution system, and a complex programmable logic device (CPLD) that has been configured to provide a high-speed *addition* algorithm

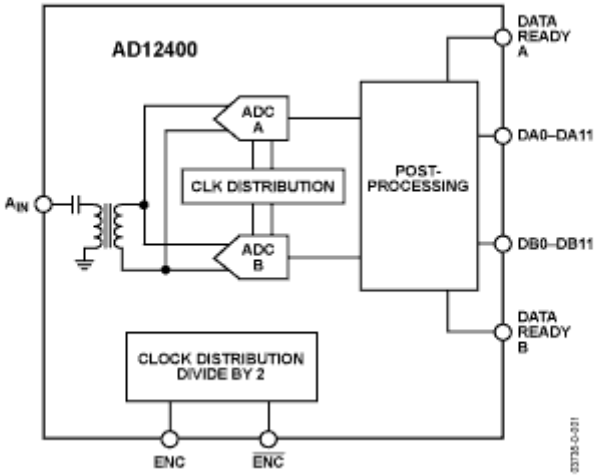
The AD6645 14-bit, 80-MSPS ADC specifies an *effective number of bits* (ENOB) of 12

2. *Time interleaving* - to increase **sampling rates** without loss of resolution:

By properly phasing each ADC's clock signal, the maximum **sample rate** of any standard integrated-circuit ADC type can be **multiplied** by the *number* of ADCs in the system.



AD12400 Specifications	
Res (Bits)	12bit
Thruput Rate	400MSPS
# of ADC Inputs	1
Supply V	Multi (+3.8, +3.3, +1.5)
Pwr Diss (max)	8.5W
Interface	Par
Ain Range	3.2 V p-p
SNR (dB)	64.4dB



The AD12400 comprises *two* high-speed AD9430s, and leverages time *interleaving* and AFB (advanced post-processing technique - *Advanced Filter Bank*) to attain a high level of performance

The AD9430 12-bit, 210-MSPS ADC specifies an *effective number of bits* (ENOB) of 10.6