

# Understanding State of the Art in ADCs

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## ***What are the driving markets?***

There are many dimensions of performance to ADC technology. Some of these are listed in table 1 below. These are common metrics for which ADCs may be selected and have obvious value for certain areas of interest.

<b>Dimension of Performance</b>	<b>Value</b>
SNR	Sensitivity to small signals
SFDR, Harmonics and Intermodulation	Rejection of undesired interferers
Power	Portability or low cost of supplies
Bandwidth	Fewer radios to capture intended signal range
Sample rate	Capture of fast transients or large bandwidths
Cost	Low Cost Radios

Table 1: Sampling of Dimensions of Performance

## **Multiple Dimensions**

Until the late 1980's, military requirements tended to drive data converter markets. Military needs were driven by radar, communications applications and EMP<sup>1</sup> detection. Often these converters were pushed in a single dimension of performance such as spurious free dynamic range (SFDR) or sample rate. Occasionally, two dimensions may have been maximized, but rarely this was the case in multiple dimensions of performance. In fact, many of these dimensions were un-important and were often sacrificed for the needed performance specification. For example, in an effort to provide the highest possible signal to noise ratio (SNR), converter power was allowed to increase to reduce overall device noise. This in turn required larger devices (discrete or on chip) and therefore the cost increased as well.

In today's market, customers and especially the commercial market expect multiple dimensions of converter performance meaning not just one or two parameters maximized, but in many cases, up to four or five. Therefore, parameters such as power consumption, SNR, SFDR, input bandwidth and cost must all be optimized. High speed converters once reserved only for military and perhaps high end test equipment are now finding applications in industrial and consumer products. Notable applications include cellular infrastructure [1][2] and a plethora of other wireless and wired applications such as DOCSIS, WiFi, WiMAX and high end consumer commercial broadcast receivers for HD, FM, AM and satellite broadcasts. The broad appeal for a well rounded ADC is rooted in the fact that once the signal band of interest is digitized, signal processing can be optimized and tailored for nearly any application using software techniques as found in software defined radio (SDR) or software defined instrumentation. The key is ADC performance that is exceptional along a number of both parallel and orthogonal performance dimensions. Typically, performance expectations for such systems are 'the best of the best' meaning best SNR and SFDR possible at the lowest possible cost in the smallest and lowest power package.

## **Level of Integration**

The integration of the ADC function into consumer equipment has brought something that the military never did, volume. While this is not a financial analysis report, it is very important to understand how the aspect of volume production influences the converter market. Many of today's high performance converters are fabricated on 0.18 micro or smaller silicon processes. The cost of a single revision of silicon on such a process can be as high as one million dollars or more, not including the many man-months of the development team. Therefore, it is easy to see that high volumes are required to provide an adequate return on investment. In order to achieve volume, devices must be targeted to match end applications as closely as possible to achieve the largest number of design-ins possible. Therefore, ADCs in many ways become Applications Specific Integrated Circuits (ASICs). Two examples of competitive devices are shown below.

Integration is along both analog and digital signal paths. While fine-line CMOS has provided an interesting path for integrating much digital content after the ADC, integration also exists further into the analog domain. Many new high speed ADCs integrate either analog or digital content in an effort to tie the device more closely to one application or another. From a communications point of view, these integrations are often generic enough or offer a level of programmability that radio applications are easy to achieve. Unfortunately for general purpose ADC consumers, these devices may often be unusable for stand alone applications.

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<sup>1</sup> EMP or Electro-Magnetic Impulses are caused by nuclear or other high energy weapons.

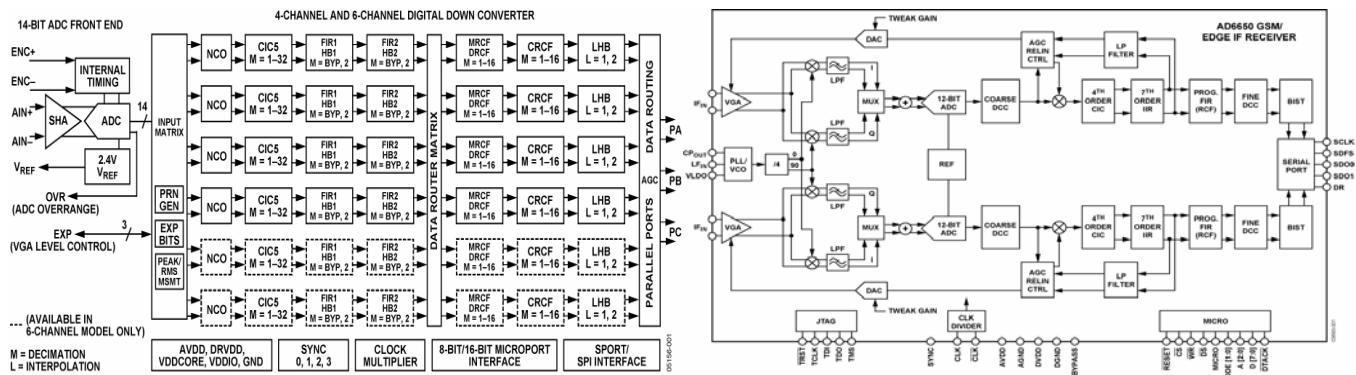


Figure 1: Examples of Integrated High Speed ADC

## Performance

As software defined systems become more common, performance expectations for converters continues to increase, generally remaining one step ahead of actual converter performance. In general, significant upward pressure exists on SNR and SFDR and downward pressure on pricing. To a large degree, these market pressures are working as SNR performance is experiencing performance jumps not entirely predicted by reports by Walden [3] and Le et al. [4] and others as a direct result of customer drive and increasing competitive pressures. Although not without performance penalties, cost for converters is falling as designs are moving from proprietary semiconductor processes to industry standard CMOS processes that are generally much less expensive. Initially, SNR performance dropped back by as much as one-half of a bit during this process transition but recent improvements show signs that performance on standard CMOS processes are back in line with proprietary processes. SFDR is experiencing a slightly different trend. Performance for high end ADCs has stalemated over the last few years and has experienced little forward progress indicating that basic linearity performance has not improving over the last few years. In order to move SFDR performance forward, a displacing technology will be required.

While performance will continue to improve in the varied dimensions, end users can affect the pace that these improvements occur by providing performance feedback to ADC manufacturers. Not a blue sky wish list but a practical and focused list of key performance criterion realizing that tradeoffs must be made in the different dimensions of performance. Only when designers know exactly which specifications to target will they know how to optimize the designs, trading off one performance for another in a meaningful and useful manner.

## What are the requirements?

While there are many dimensions of performance, there are always a few key specifications of interest. These specifications are key to a broad range of applications and offer a view into widely accepted parameters and how they enable certain features as well as how they interact with other parameters.

## Analog Input

### Wider Input Bandwidth

Converter bandwidth is largely determined by the size of the sample capacitors used in the ADC. Bandwidth is inversely proportional to the value of the sample capacitor as shown in equation 1. This is easily observed by considering that the sample process consists of a finite resistance sample switch and a sample capacitance. In this case, it is readily apparent that bandwidth is determined by the combination of the switch resistance (and any external series resistance) and the sample capacitor. Therefore, to maximize input bandwidth, both R and C should be minimized.

$$BW \propto \frac{1}{C}$$

Equation 1: Converter Bandwidth

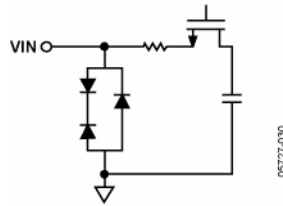


Figure 2: Typical ADC Input Network

Wider input bandwidth allows for better slew rate performance and more accurate tracking of fast slewing analog signals associated with both transient events and high frequency sinewaves. It also allows wide band analog signals to be accurately sampled and is often accompanied by a faster sample rate.

Conversely, wider input bandwidth allows more noise to pass the ADC input stages and be digitized, resulting in lower SNR than would have for a lower bandwidth ADC. This is the reason many high bandwidth ADCs have lower SNR performance than otherwise predicted. If the sampling rate is high enough the input noise will be widely distributed across the Nyquist band and digital filtering can remove excess noise should the desired bandwidth fall within a Nyquist band of the ADC. However, if the sample rate is much less than the analog input center frequency the input noise will be aliased into the Nyquist zone and the noise density can become quite high. Therefore, great care must be taken both in the design and use of wide bandwidth ADCs.

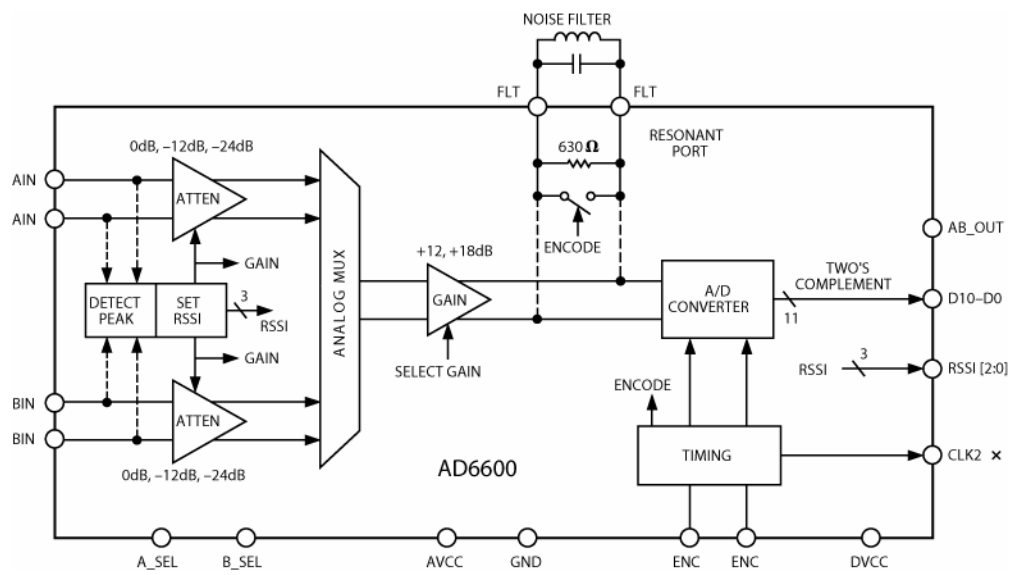


Figure 3: Example of a band-pass ADC for general purpose use.

In reality, wider bandwidths are only necessary for wideband signals such as transient events. High frequency sampling only needs sufficient bandwidth to sample the signals of interest. Since most common signals are band-limited both for performance and regulatory reasons, 'wider' bandwidth is not a necessary requirement of IF under-sampling. Because of this, a class of ADCs called band pass converters allow high frequency signals to be digitized without the excess bandwidths. This results in low distortion sampling and high SNR performance in the signal band of interest. These are typically found as band-pass delta-sigma converters and are often used in highly integrated receiver functions such as those used in WiFi chip-sets. Other examples for more general purpose usage can be seen in products like the AD6600. Its noise improvements are achieved by allowing the internal analog network to be resonated at the desired IF to improve unit SNR and to provide rejection to signals outside the band of interest. Standard converters may also be resonated for improved performance, reducing the drive requirements, improving noise performance and filtering input spurious [5].

### IF Under-Sampling

The IF under-sampling technique has long been sought as a means for reducing the complexity of a receiver design. In fact, sampling as close to the antenna as possible offers the possibility of reducing the size and complexity of the receiver function in a system. Most modern cellular base stations implement IF sampling allowing one or more IF stages to be eliminated from their system reducing both cost and complexity.

While IF under-sampling does reduce overall system cost, there is a performance tradeoff in that IF under-sampling ADCs in the past have generally resulted in lower performance than baseband sampling ADCs. Over the past few years, this requirement has driven

the demand for high performance IF sampling ADCs and are now available that are optimized for both SNR and SFDR for frequencies as high as 450 MHz.

## Wider Bandwidth vs. Higher IF

### Sample Rate

Sample rates are driven by several factors. The largest driver is to have a sample rate that is an integer multiple of common data rates for communication standards. For example, CDMA2000 has a base symbol rate of 1.2288 MHz, WCDMA has a base rate of 3.84 MHz and TD-SCDMA has a base rate of 1.28 MHz. Based on these rates, common sample rates of 78.6, 92.16, 122.88 and 245.76 MSPS are common. As in the past, the ADC technology determines the preferred sample rate and over the past few years, the preference is to run above 80MSPs in most new designs.

Higher sample rates do improve noise performance of ADCs. While the overall integrated noise does not improve, the distribution of the noise over wider bandwidths does offer improvements in noise spectral density (NSD). The lower the noise spectral density, the more sensitive a receiver can be designed. This process is often referred to as processing gain and is nothing more than distributing the same noise over a wider band of frequencies and then digitally filtering out the noise in the frequency bands that are not of interest. Doubling the sample rate can improve the noise spectral density by a factor of 3 dB resulting in a significant improvement in performance of many systems.

However, there are limits to how much sample rates can be increased. Current FPGA<sup>2</sup> and ASIC<sup>3</sup> technology limits CMOS<sup>4</sup> data rates to about 250 MHz, LVDS<sup>5</sup> to approximately 800 MHz and PECL<sup>6</sup> to approximately 1.5 GHz. Other logic schemes such as CML<sup>7</sup> offer the possibility of even higher rates. While some applications have moved to LVDS and PECL, the bulk of applications are implemented in CMOS. This will change in the future, but for now, the mainstream driving applications are still CMOS.

## Better Dynamic Range

### Noise (SNR)

As already established, noise level is directly proportional to input bandwidth (SNR is inversely proportional to bandwidth). The total noise in the system is proportional to equation 2 below. This equation shows that noise is proportional to Boltzmann's Constant and absolute temperature and inversely proportional to the sample capacitor.

$$noise \propto \frac{kT}{C}$$

Equation 2: ADC Noise

As stated in a prior section, noise density decreases with sample rate. As both SNR and sample rate improve, the thermal noise floor continues to reduce. While a long way from device thermal noise, current wideband converters are approaching the noise level of an optimally matched antenna (-174 dBm/Hz) making them easier to use in systems with even modest conversion gain. Current technology is within 20 dB of reaching this threshold and new techniques are being discovered for reducing the noise level through signal processing and better analog design.

In most applications, this level of performance is only achieved when using a low jitter clock source [6] [7]. In recent years, low jitter oscillators, PLL's, DDS' and other devices [8] have become available that can both clean up reference clocks and provide high fan outs to multiple devices in a system. Current ADC technology provides clock jitter as low as about 50 fs creating quite a challenge to system clock designers. Only when system designers provide clock jitter this low can full performance be expected from ADCs, especially when operated at high IF's.

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<sup>2</sup> Field Programmable Gate Array is a logic device that can be programmed for a specific task in the user application rather than during the semiconductor manufacturing process.

<sup>3</sup> Application Specific Integrated Circuit is a customized circuit used for a specific function.

<sup>4</sup> Complementary Metal Oxide Semiconductor is a type of semiconductor.

<sup>5</sup> Low Voltage Differential Signaling is a type of digital logic utilizing low voltage swing and differential signals to reduce interference. LVDS is often used for data path signals.

<sup>6</sup> Positive Emitter Coupled Logic is a type of digital logic utilizing low voltage swing and differentials signal to reduce interference. PECL is often used for low jitter clocking.

<sup>7</sup> Current Mode Logic is a type of digital logic utilizing low voltage swing and differential signals to reduce interference.

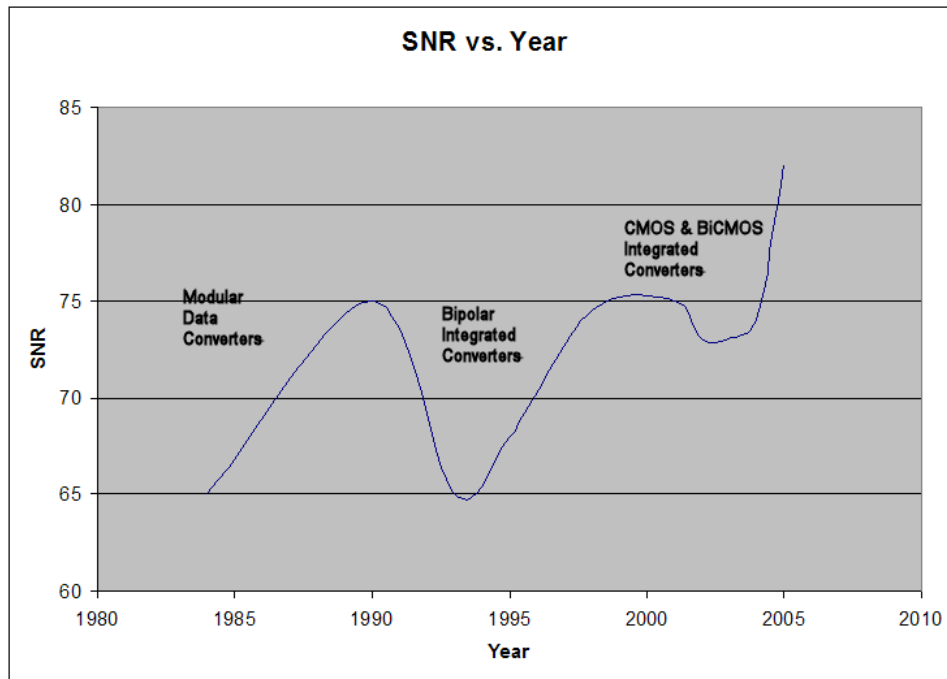


Figure 4. Recent SNR Trends in High Speed Nyquist Converters

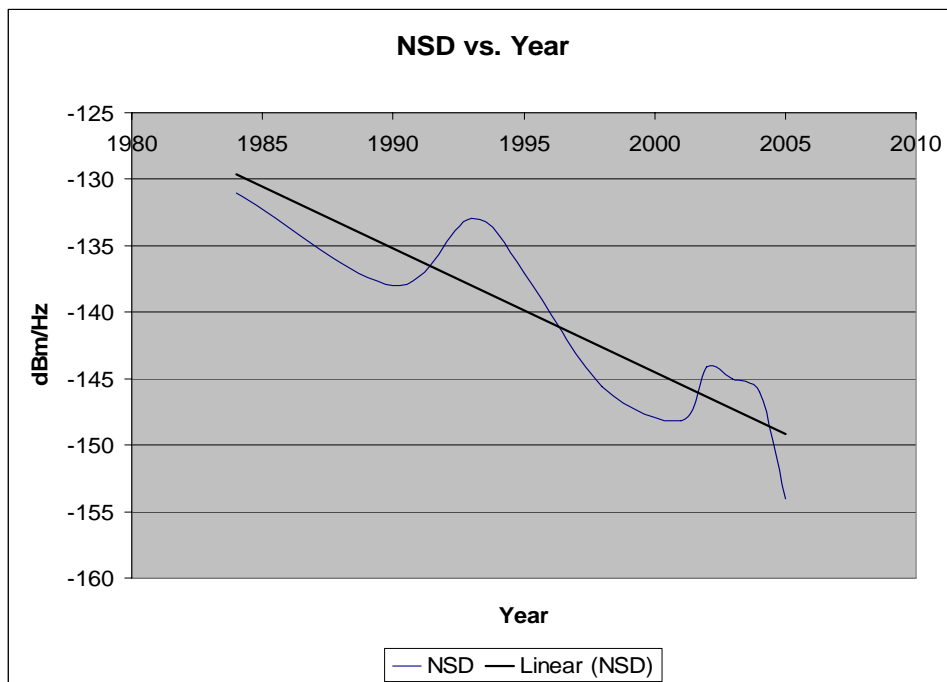


Figure 5. Noise Spectral Density Trends for Production High Speed Nyquist Converters  
(Note the effects of new technologies to the curve and that recovery seems to continue the trend.)

### Spurious (SFDR, Harmonics, IP)

Better spurious performance is achieved by wider bandwidth. A system with a large input bandwidth is less prone to slew rate limitations, allowing the ADC to better track the signal input to the device. As seen in equation 1, bandwidth is proportional to  $1/C$  and since a fast slew rate translates to spurious performance, the same  $1/C$  relationship applies.

$$Spurious \propto BW \propto \frac{1}{C}$$

Equation 3: Spurious performance

Therefore, for optimal spurious performance a wide input bandwidth is desirable. This means the sample capacitance must be as small as possible. However, from equation 2 we know that making the sample capacitance small, the increased input bandwidth allows more noise to enter the front end of the ADC and be spread across the Nyquist spectrum. Thus, SNR and SFDR must always be traded off between one another. Academic literature has continually produced work that explores the key to significantly improved performance. The studies examine how to improve the sampling switch mechanism while optimizing both a reduced sample resistance and smaller capacitor [9].

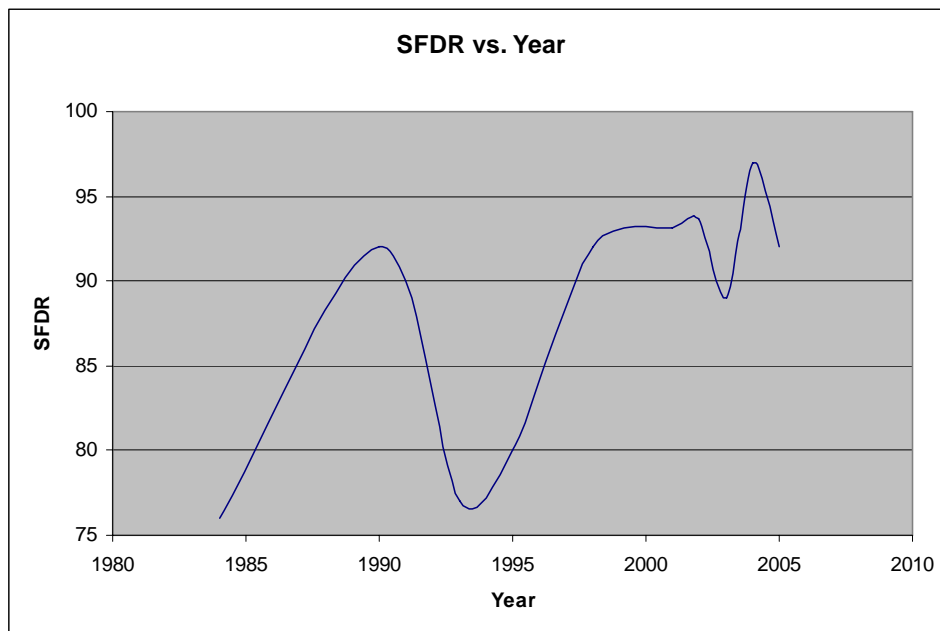


Figure 6. Baseband Spurious Performance Trends for Production High Speed Nyquist Converters

### ADC Performance Table

Given the trends shown above for both SNR and SFDR, how do they stand up against system requirements? The table below shows required performance by air standard for popular wireless standards. These specifications are for wideband multi-carrier performance without the benefit of automatic gain control, similar to what would be required for a software defined receiver capable of processing that standard. As seen, GSM/EDGE in the 900 MHz band is the most challenging and currently not possible with existing converters (current systems utilize single carrier design with narrowband filters and AGC). Referencing figures 4 and 6 clearly shows that for the remaining standards, multi-carrier SDR is entirely possible from an ADC perspective.

Standard	SNR	SFDR	Sample Rate
TD-SCDMA	73 dBFS	83 dBFS	122.88 MHz
CDMA2000	79 dBFS	86 dBFS	92.16 MHz
WCDMA	70 dBFS	81 dBFS	92.16 MHz
WiMAX	~75 dBFS	~90 dBFS	80 MHz
GSM/EDGE (900 MHz multi-carrier)	85 dBFS	110 dBFS	104 MHz

### Common platforms & reuse

Unlike digital designs where Moore's Law [10] is cited, analog and mixed signal designs can not constantly be shrunk to take advantage of smaller geometry processes. There are at least two fundamental process limitations. On digital designs, the verilog code defining the chip can simply be rerun on a compiler for the new process. Therefore, the migration is easy given the ease of design transferability. This is not the case with high performance analog designs. Typically, these analog blocks are not designed in verilog but instead optimized at the transistor level for the specific process to optimize power, noise and linearity. When moved to a new process, the optimization must be completely redone as seen in the displacements in figures 4 and 5 as designers adjust design strategy and techniques for the newest process. In fact, many times, totally new design topologies are required, forcing new designs and architectures. In addition, some processes are simply not compatible with analog signal processing and variations must be made. For example, small geometries have lower breakdown voltages ( $v_T$ 's) and therefore devices must be made larger than the minimum size. If this is required for a significant portion of the device design, using the smaller geometry process loses its appeal for use as an analog or mixed signal process.

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Design reuse is similarly limited to product variants or derivatives on the same process. It is not possible to take one 0.35  $\mu\text{m}$  based design and migrate it to 0.18  $\mu\text{m}$  and expect performance to be the same or better as shown in figures 4 and 5. In general it takes a few product generations for designers to understand the performance curves of a new process and advance the performance curves for high speed ADCs. As stated, using the larger transistors on the finer line process will waste expensive die space and probably will no longer be optimized. Designing product derivatives or close variants are highly possible within the same process. In fact, this is often seen in products where single, dual, quad and octal channels are required. Likewise, reuse is seen in cases where integration with additional analog and digital features is required. At the design core level (fully functional ADCs) products like ADI's AD9228 12-Bit 65MSPS quad ADC are easy to reuse across a large portfolio of both standard products including octals and more application specific products that could include gain, filtering and mixing analog functions. At the circuit level, functions such as output drivers, references and amplifiers are easily reused as long as the processes remain the same.

Unlike memory chips that can constantly be shrunk as newer processes are available, mixed signal ICs never follow the same cost reduction as experienced with digital chips. Once a product is released, its design is fixed and forever tied to that process geometry. Released processes do not experience reduction of cost over time and consequently the cost per die remains fairly constant. A common method to reduce the cost (and price) is to improve product yield and increase volume or to design a new ADC on a new, lower cost process. Unfortunately, as shown in the curves above, this results in a reduction in performance over previous generations. While this does correct in future generations, jumping processes frequently results in reduced performance from one device to the next. The conclusion is therefore that for a system to be reduced in cost from an ADC perspective, new devices must be used since older designs can not be cost reduced. At the same time, going through cost reduction cycles too frequently may result in selecting an ADC with reduced levels of performance.

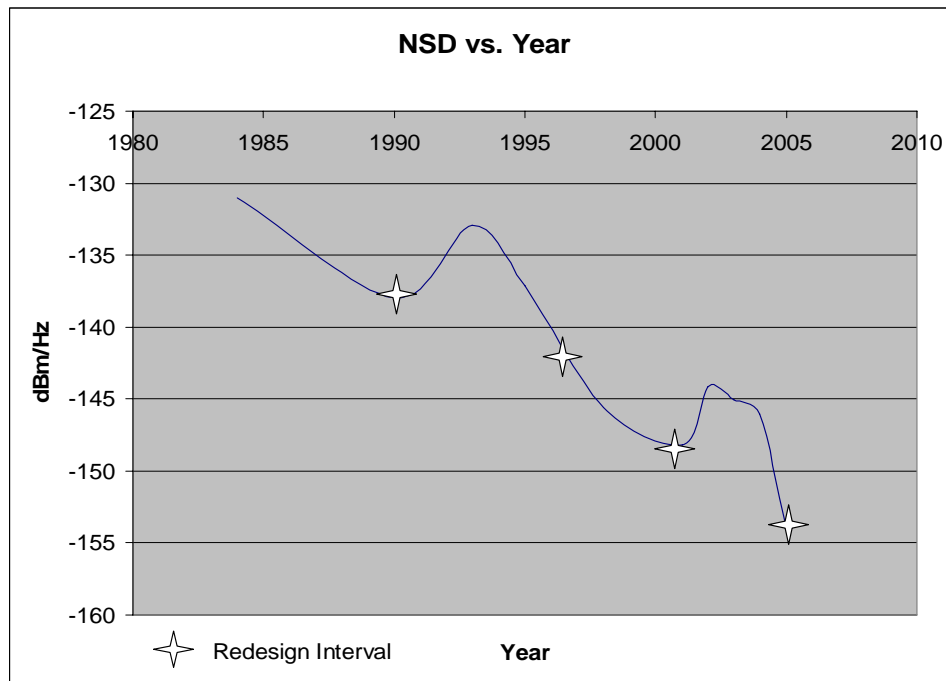


Figure 7. Optimal Redesign Cycle from a historical perspective to give both cost and performance improvements

When devices are migrated to new processes, it is often the desire to make the new device pin and function compatible. Unfortunately, it may behave differently in a number of ways. Not only will dynamic performance be different as outlined above, but analog inputs (range and impedance) and digital output characteristics may be different. More importantly, newer processes typically have smaller breakdown voltages and therefore support lower supplies. While most processes do have the ability to retain supplies of their previous generation, maintaining supplies from two or more generations is becoming increasingly difficult as geometries continue to reduce. These issues make it almost impossible for pin-compatible drop in replacement for the older device without changes to supplies, input matching networks and receiving logic gates.

Pin out families do emerge over time resulting in a continuum of resolution and sample rate in the same package with the same pin out. The results are families of converters with resolutions from 10 to 16 bits with sample rates from about 10 MHz to over 250 MHz can be supported with the same foot print. Several manufacturers offer families of devices fitting this description [11]. This does allow the flexibility of migration between both bit precision and sample speed and over time as pin out families develop, does allow cost reduction from one generation to the next as long as pin outs remains fixed and package technology does not evolve too rapidly. Building a base of pin compatible devices encourages generational development of follow-on device development similar to that of

DACs in the families of devices AD976x, AD975x and AD974x. In addition, having a variety of pin out families provides leverage to purchasing agents in selecting not just functional devices, but allows them to generationally select those devices that bring the greatest value to their end product. From a manufacturing point of view, pin out families allowed for product grade out allowing those products that have the highest performance to be sold as premium devices where as lesser devices can be graded and sold based on their level of performance, thereby offering the best value and highest yields possible.

With the introduction of .35 um CMOS converters, the inclusion of digital features to the core ADC offer many interesting functions beyond the standard output data format. New feature sets include shuffling, dithering, output test patterns, built in self test and a plethora of other user features [12]. However, accessing these features can be problematic. Many new high speed converters now offer SPI interfacing to access the rich features sets once reserved for slow conversion ADCs. Because these features are digital, they can now be easily transported from one design to the next, even across process changes because of their generation in Verilog or other digital language. Over time, many of these new features will emerge as 'standard' features of high performance ADCs and will exist for many generations, even through process shrinks and changes. This standardization of features leads to standardization of design files (for the digital control portion) as well as end application software which often times can not be changed once an OEM's product has been released. In order to preserve the user investment in control software, consistent product memory maps should emerge.

### ***What are the Hardest Limitations?***

A number of limitations exist in data converters. As mentioned above, there is a natural conflict between SNR and SFDR. These are improved by advances in architecture and optimizations in process. While improvements have continually occurred over time, the process is at least partially reset each time a new semiconductor process is employed (see above). Because of this, improvements often tend to be two steps forward and one step backwards. Cost pressures push decisions to switch to newer processes whereas remaining on older processes would indicate that generational improvements in performance are possible but not necessarily a cost reduction.

Additional issues exist with moving to smaller geometries. As the geometry sizes decrease, breakdown voltages are reduced making it harder to design for performance. In terms of SNR where thermal noise may be considered 'finite' for a process or architecture, larger input swings can improve performance. If breakdown voltages constrain signal swing, SNR limitations may result. While this is not a problem for low resolution converters, it is a big limitation for high resolution converters, especially those with large input bandwidths. Similarly, lower breakdown devices offer only reduced overhead between analog signal swings and power supplies, implying poorer linearity from those devices. In summary, smaller geometries with lower breakdown values offer poorer noise and linearity performance.

Interfacing to the analog input is becoming more difficult. For low frequency applications, this is not a big issue but as IF frequencies increase and direct RF sampling becomes a possibility, proper impedance matching to the source becomes more critical. At high frequencies, optimal ADC performance is only achieved when a proper match exists not only because the input is presented with a maximum of signal level but because ADC input behavior in terms of both noise and especially spurious is optimized [5]. Therefore, behavior of the input is very critical to both device designer and end user.

### ***Where are we headed?***

Figures 4 and 5 give a good indication of where Nyquist ADCs are headed. Clearly, SNR is on an improving trend with a clear mind for increased performance. Based on noise spectral density, performance over the last 20 years indicates a solid 1 dBm/Hz per year. As for spurious, this report has provided antidotal evidence showing that SFDR performance has been constant for the last 5 to 10 years in the baseband region. While there is a clear need for fullscale performance in the range of -110 to -120 dBFS, consistent performance of only -95 to -100 dBFS is available in the baseband region today. At the same time great attention has been paid to increasing SFDR performance in the mid and high IF regions with a result that usable IF frequencies as high as 450 MHz are not uncommon for some applications.

In addition to improvements in the analog signal path, improvements in the digital domain can also improve performance. With digital features such as shuffling, dithering [13] and calibration becoming standard features on high speed converters, it is clear that the 'D' is getting bigger in ADC. Each of these digital techniques has the ability to improve the linearity and noise performance of the converter under a variety of conditions. It is clear that improved performance will come from a combined effort of improvements in the analog path as well as digital techniques including calibration, shuffling and dithering.

### ***How do we get there?***

Because of the physics of ADCs, there will always exist a natural opposition between spurious performance and SNR. Therefore, designers are constantly forced to compromise one specification for another. Therefore, it is key for customers to give feedback and guidance to ADC manufacturers. Without clear direction, ADC manufactures will move in the direction they are most drawn to which

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may not be the direction most needed by the customer. Clearly however, a focus needs to be placed on fullscale and near fullscale spurious performance. This will come in time but the issue is continually compounded by process changes that require lower power supplies.

In addition to improvements in process and Nyquist converters as described here, advances in other classes of converters holds potential and may displace these converters in some applications. Old architectures typically thought of as low speed are making an appearance in many applications once reserved for high speed Nyquist converters. Successive Approximation (SAR) ADCs are benefiting from faster and improved processes allowing them to both sample faster and at high input frequencies. Similarly Delta-Sigma ADCs are being used to sample both wider bandwidths at higher IF's using bandpass techniques.

As mentioned before, another key to improved performance is improved clock sources. To achieve rated SNR, especially at high input frequencies, clock jitter must be minimized. Therefore, continued development of low jitter clock sources and a comprehensive understanding of ADC users to the importance of clock sources is a requirement to gaining full performance both now and in the future. Without this, ADC performance will not continue to improve.

In the end, it is not just the ADC designer who is challenged to design a better ADC; the system designer is challenged to blend all of these aspects together. He must choose the right ADC based not only on performance, but cost and other tangible and intangible aspects of converters. He must then apply them in the right manner to achieve optimal performance. This includes layout, input matching, clocking and data collection. Only when these aspects are carefully tended to will the next level of performance be achieved. In order to aid in the development of these systems, manufacturers must provide training and tools, including behavioral modeling [14] to facilitate the next level of performance. Through these interventions, ADC users should be able to make the most of converters.

### **Analog Devices**

Analog Devices is the world leader in data conversion technology. ADI's longstanding leadership in data conversion technology stems from an engineering culture that emphasizes deep understanding of the customer's system challenge, aggressive research and development investing and unmatched mixed-signal design expertise. From application-specific solutions designed to lower system cost to the broadest selection of speed, accuracy, size and power consumption in DACs and ADCs, Analog Devices provides the products, technology and support customers need to successfully bridge between real-world analog signals and the digital world of electronic equipment. ADI's data converters are used widely in consumer electronics, broadband and wireless communications, automotive systems, industrial equipment and medical electronics, as well as a host of other emerging market applications.

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