

# Choosing a high-speed converter

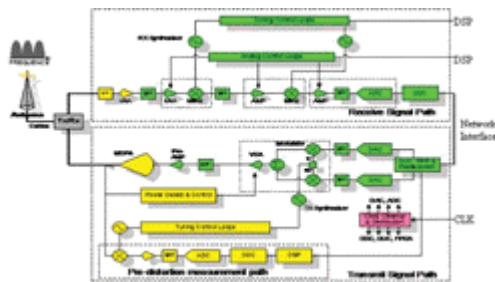
*Designing mixed-signal systems—especially at today's high speeds—requires strict attention to the detailed specifications of converters*

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System developers are challenged by the lower noise, higher speeds, multiple carriers, wider bandwidths, and faster deployment rates required of today's wireless and wired communication systems. *Figure 1* shows high-speed converters providing power amplifier pre-distortion in the measurement signal path, baseband (I/Q) signal detection in the receive signal path, and modulation in the transmit signal path.



**Fig.1. High-speed converters meet many requirements within the communications transmit and receive signal path of today's wireless and wired communication systems.**

A familiarity with converter architectures, reference designs, and modeling tools will allow designers to choose the best converters for their systems. The configuration of converters directly affects a system's ability to detect low-level signals, especially in the presence of interferers. Designers must select converters to meet power consumption, speed, and accuracy requirements—while satisfying size, cost, and time-to-market targets.

Ideally, the predicted performance of components will match their real-world performance closely enough so that redesigns—and costs—are minimized. Detailed simulations and evaluations help tremendously, and configurations can be analyzed prior to actual hardware generation. This minimizes the number of hardware changes, simplifies the converter selection process, and speeds development.

## System level architecture

Tradeoffs of performance and cost are made throughout the design process. Should a super-heterodyne sampling or a direct conversion scheme be used? Many receivers now employ an **IF under-sampling** approach. Here, the IF falls within the second or third Nyquist zone of the A/D converter (ADC). The impact on system performance caused by

operating a converter under such conditions—including power supply variations, temperature extremes, and passive-component tolerances—must be well understood.

The system architecture decision involves many factors, including lessons learned, system analysis, and available reference designs. Previous successes of similar designs may dictate which architecture is chosen. At the system analysis level, one may explore the need to have a gain stage in front of a 12-bit ADC versus implementing a 14-bit ADC, or consider a dual D/A converter (DAC) plus an analog modulator versus a very high speed DAC to generate an IF. Reference designs can demonstrate proven performance of components, but this simply provides a guideline, since actual performance relies on how the components operate under true system conditions.

### **System specifications**

Designers of wireless, wired, point-to-point and high-speed communication systems seek components that will support:

- \* Increased speeds for higher signal bandwidths
- \* Higher resolution for small-signal detection
- \* Better signal-to-noise and spurious rejection
- \* Reduced power consumption

More bandwidth means more information. This results in faster communication and better reaction capabilities—whether to military threat conditions, call transfers, or adaptive equalization. Higher resolution means increased detection of low-level signals. With improved signal-to-noise and spurious rejection, these low-level signals can be more easily detected in the presence of noise, interferers, or blockers.

### **Converter specifications**

The first step in converter selection is to translate standards requirements, such as those for W-CDMA, CDMA-2000, or WiMAX, to **system level** requirements. For example, the 3GPP standard for Wideband CDMA calls for rejection of blockers as high as 87 dB above the desired channel. This sets the signal-to-noise ratio (SNR), gain and noise figure (NF) requirements of the transceiver signal chain converters.

The next step in converter selection involves a comparison of data sheet specifications to system requirements. **Key** system needs, such as input frequencies, output signal processing, phase-locking and integration, must be clearly defined.

The faster and more accurate the selection process, the more likely system time-to-market and costs will be met. High-speed converters offer a range of characteristics to assist designers in optimizing their communications system performance:

- \* **Resolution** (set by number of bits; determines minimum detectable signal)

- \* **Analog Bandwidth** (sets highest analog input or output frequency that can be converted)
- \* **Encode or Clock Rate** (sets the sampling speed of the converter)
- \* **Spurious Free Dynamic Range** (sets sensitivity to interferers for an ADC, or transmit mask for a DAC)
- \* **Noise and Distortion** (can limit dynamic performance of the converter)
- \* **Linearity, Offset, Gain** (sets how accurately the converter output represents the input)
- \* **Power consumption** (can affect the system partitioning and overall system budget)

In addition to data conversion, designers must also consider functions such as **DSP, clock generation, and phase locking**. Converters depend greatly on the characteristics of the input analog signal and the sampling clock.

Higher frequencies and bandwidths correspond to faster switching rates and higher noise. Multi-channel systems may require multiple converters within the same **package** to minimize space, especially for indoor transceiver units like picocells. Portable hand-held systems, with battery power sources, support specific supply voltages and must maintain low **power** consumption.

Most converter data sheets specify standard operating conditions such as input frequency, sampling rate, supply voltages, and temperature. Keep in mind that each converter vendor characterizes their components differently. True operating conditions will vary depending upon system requirements. So, designers must consider how these variations will affect the converter's linearity, dynamic range, noise, and distortion.

### **Converter performance**

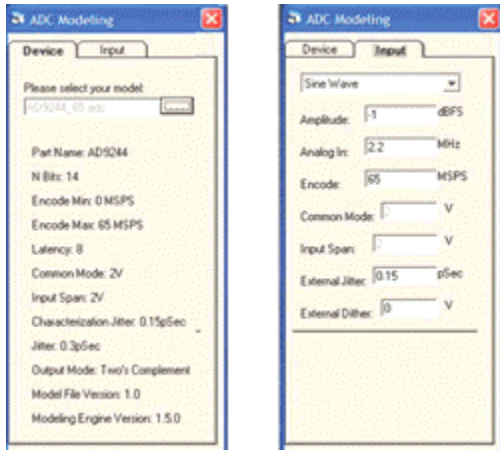
One way to see how a converter will operate is to run it in an **evaluation board**. This requires hardware configuration, test, and modifications to operating conditions while data is taken. If the converter performs poorly, the designer must restart the evaluation process with another part. In addition, designers often wish to evaluate performance with selected clock and/or PLL circuitry. Acquisition and configuration of this hardware adds to the converter evaluation time. This process can take weeks.

A faster converter selection process involves first using **simulation tools** to view the converter's performance. This requires accurate converter models that can be adapted to actual system operating conditions. The designer will then have more confidence in choosing a converter before any hardware is built.

## Converter model and evaluation tool

Many simulation tools exist at the system level. For example, Analog Devices' *ADIsimADC* tool is a behavior modeling example which uses test data, noise and distortion polynomials, and transfer functions to show how an analog-to-digital converter will perform under user-defined operating conditions.

The *ADIsimADC* package provides the front-end for a dynamic link library (.dll) program that can be called from higher-level system simulations. *Figure 2* shows an example of converter parameters.



**Fig. 2. With simulation tools designers can quickly evaluate the performance of converters under real-world conditions.**

Data are generated using detailed characteristics of ADI converters that are included in the many device models. **Ideal ADC models are also included for comparison.**

With simulation tools, designers can quickly evaluate the performance of converters under real-world conditions. Selection of products becomes faster and easier and design confidence is improved. As hardware is procured, lab data and simulation data can be combined to view overall system performance.



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