Picosecond Pulse Labs

Real-Time Sampling Downconverter Front Ends for Digital Radar and Wide-Band Signaling

A sampling down-converter is used to extend the RF bandwidth, and improve the static and dynamic non-linearities of an ADC at the heart of a real-time digital receiver. While static non-linearities are easily correctable using real-time or post-acquisition processing, frequency dependent, dynamic non-linearities are particularly troublesome, as they cause dynamic range (as measured by "Effective Number of Bits" (ENOB), to degrade with RF frequency as well as RF signal level. In a digital IF system, it is usually the Track & Hold Amplifier (THA), ahead of the digitizer, that is the critical element in controlling dynamic non-linearity. Careful attention to the various sources of dynamic non-linearity is required to preserve the system dynamic range and accuracy up to, and well beyond Nyquist.

This paper will show how a sampling downconverter matched to a THA can perform both the downconversion, and the hold function. The linearity of the sampling front-end dominates the overall system linearity by rendering the dynamic non-linearity of the THA effectively static, and therefore correctable.

This combination provides simultaneously, a DC-100 GHz RF BW, DC-13 GHz IF BW, and up to 10 Effective Bits noise and linearity (corrected) at full 2Vp-p input amplitude, at sample rates, potentially exceeding 10 GS/sec.

I. Introduction

The "Holy Grail" of the "Software Defined Radio" concept, is an Analog-to-Digital Converter (ADC) attached to an antenna. In practice, a downconverter and/or Sample- or Track & Hold device is required ahead of the ADC. Sometimes these two functions (downconversion and hold) are combined.

A Track & Hold amplifier (THA), or Sample & Hold (SHA) ahead of the digitizer is invariably required to hold the sampled signal constant during the analog-to-digital conversion process. Even single-rank flash converters perform better dynamically, with a hold function preceding them.

The job of the downconverter is to bring a portion of the RF spectrum into one of the Nyquist bands of the ADC. The THA or SHA can also be used for the downconversion process if it has an analog bandwidth greatly exceeding the Nyquist bandwidth. This is used in the process of "sub-sampling" where the higher order Nyquist bands are accessible, much like harmonic downconversion mixers. Unfortunately, due to dynamic non-linearities in the THA (predominantly slew-rate limitation and dynamic switching aperture modulation by the input signal), linearity and dynamic range decrease significantly for large signals at frequencies approaching the large-signal 3dB bandwidth of the THA.

It is well known that it is primarily the linear and non-linear contributions of the front-end subsystems in a digital radar or communications receiver, that determine the noise and linearity, respectively, of the full system.

Just as the (linear) antenna and low-noise amplifier (LNA) ahead of the downconverter primarily determine the noise figure of the system, the nonlinear frequency conversion/sampling function (downconverter and Track/Hold), primarily determine the dynamic range of the overall system.

Static non-linearity is only amplitude dependent, and therefore easily correctable with digital signal processing (DSP). Dynamic, or frequency dependent, non-linearity is more difficult to correct, in general. It causes dynamic range (as measured by "Effective Number of Bits" (ENOB) in a digital system), to degrade with RF and IF frequency as well as signal level. Dynamic non-linearity causes frequency dependent phase and amplitude distortion. In a digital IF system, it is usually the Track/Hold ahead of the ADC that is the dominant source of dynamic distortion, and therefore critical element in controlling dynamic distortion. Careful attention to the various sources of dynamic distortion is required to preserve the accuracy up to Nyquist. Sub sampling downconverters, operating in the higher Nyquist bands, are even more susceptible to dynamic distortion owing to the higher RF and IF frequencies involved.

A fast-switching, sampling downconverter ahead of the THA amplifier can greatly ease the dynamic linearity requirements of the THA, as well as providing the system with RF bandwidth well beyond the first few Nyquist bands.

This paper describes a sampling downconverter matched to an external THA/ADC that performs both the downconversion, and hold function. This combination provides simultaneously, a DC-100 GHz RF BW. DC-13 GHz IF BW, and 10 Effective Bits noise and corrected linearity at full 2Vp-p input amplitude, at sample rates exceeding 10 GS/sec.

The described architecture is directly applicable to real-time digital radar and UWB communications receivers. When combined with similar technology to perform baseband upconversion [1], an Rx-Tx for UWB, and a radar signature test waveform source can be realized.

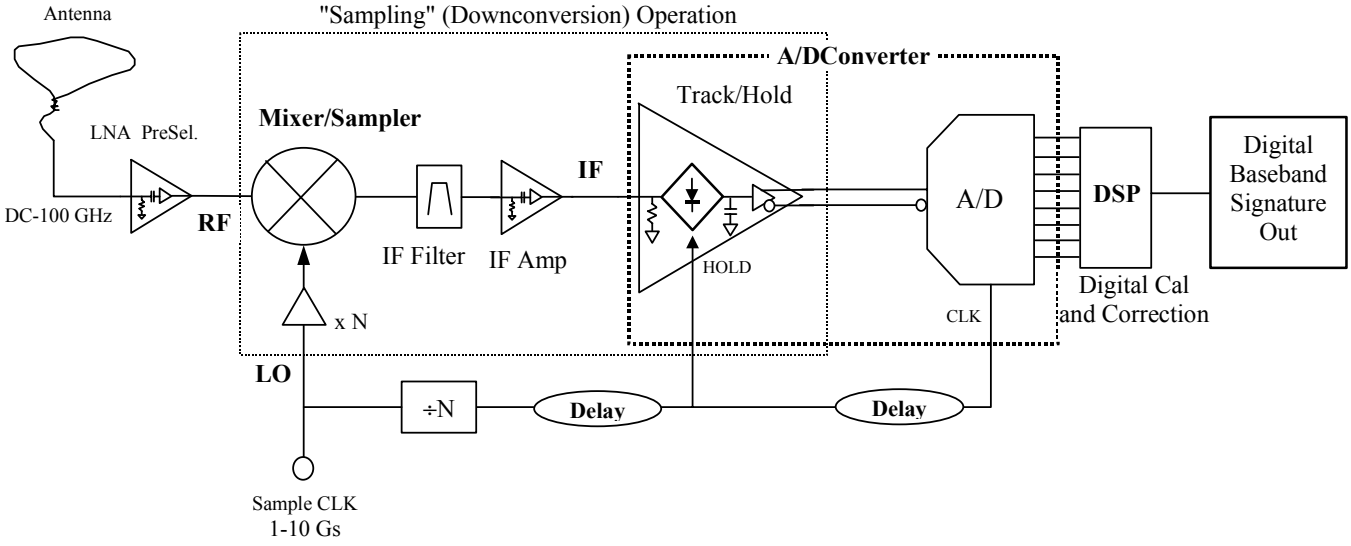


Fig.1 Digital Downconversion Receiver

II. Digital Receiver Architecture

The block diagram in Fig.1, is a generic, single-channel, digital radar receiver front end, consisting of a bandpass antenna system, a low-noise amplifier (LNA), a mixer (downconverter), with IF filter/amp, Track/Hold Amp (THA), Digitizer (ADC), and Digital Signal Processing (DSP). The THA may be part of the ADC, or a separate device technology. The ADC can be a single device, or it could be part of an N-interleaved architecture, which increases the sample rate by N over the individual A/D conversion rate. State of the art today (2004), is 20 GS/sec with 8 bits of resolution. This is available commercially in real-time digital oscilloscopes, using either 12 X 1.66 GS/s, 16 X 1.25 GS/s, or 80 X 250 Ms/sec interleaved digitizers. This potential 10 GHz real-time, instantaneous, Nyquist, *information* bandwidth is limited currently, by the THAs in the systems to around 7 GHz, for small signals. For large signals, i.e. those that use the full range of the ADC, digital correction of the static linearity errors can keep the ENOB above 7 bits. For large signals at full bandwidth, the situation is much worse. Dynamic nonlinearity in the THA and interleave timing error reduce the dynamic range to less than 5 bits, typically, at full scale input and full frequency.

Another key requirement for "real-time" (sample-by-sample) signal acquisition, is that the "instantaneous (real-time) bandwidth", i.e. the IF bandwidth of the downconverter being greater than the analog bandwidth of the THA, and both must be greater than the Nyquist bandwidth of the ADC. In the time domain, this means that the rise time of the step response, or the FWHM of the IF impulse response, must be comparable to, or faster than the rise time/ impulse response of the THA.

It is also important that the settling time of the downconverter IF impulse response be much less than the sample period. The IF must settle to within an LSB in one sample period to erase any memory of the previous sample. This implies an IF bandwidth substantially greater than the Nyquist bandwidth of the ADC.

Sample-to-sample memory (intersymbol interference), represents a dynamic non-linearity because it causes the complex RF-IF conversion gain to depend on sample rate and IF frequency. This type of ISI is a non-linear version of the ISI that is corrected in communication channels with equalization filters. Non-linear ISI is more difficult to correct digitally

It appears theoretically possible to correct for this type of dynamic distortion using a FIR digital filter with non-linear tap coefficients. This is currently being studied by the author. Nonetheless, given the practical limitations of numerical correction, raw (uncorrected) performance is still important, regardless.

III. Real-Time Sampling Downconversion

A wideband sampling downconversion architecture has been developed that addresses most of the above issues. The guiding hypothesis is that an appropriately designed sampler ahead of a THA relieves the dynamic linearity requirements of the THA, and puts them on the sampler. The sampler is designed to have at least comparable static linearity, but also much better dynamic linearity than the THA, and the sampler performance dominates the system performance.

A unique traveling-wave sampling architecture, using fast GaAs Schottky diodes and Non-Linear Transmission Line (NLTL) pulse compression technology exhibits very low static and dynamic non-linearity, while providing real-time IF bandwidth that is many times the current Nyquist limit of 10 GHz (20 GS/sec), has been developed. RF bandwidth from DC to 100 GHz has been demonstrated with this technology [2].

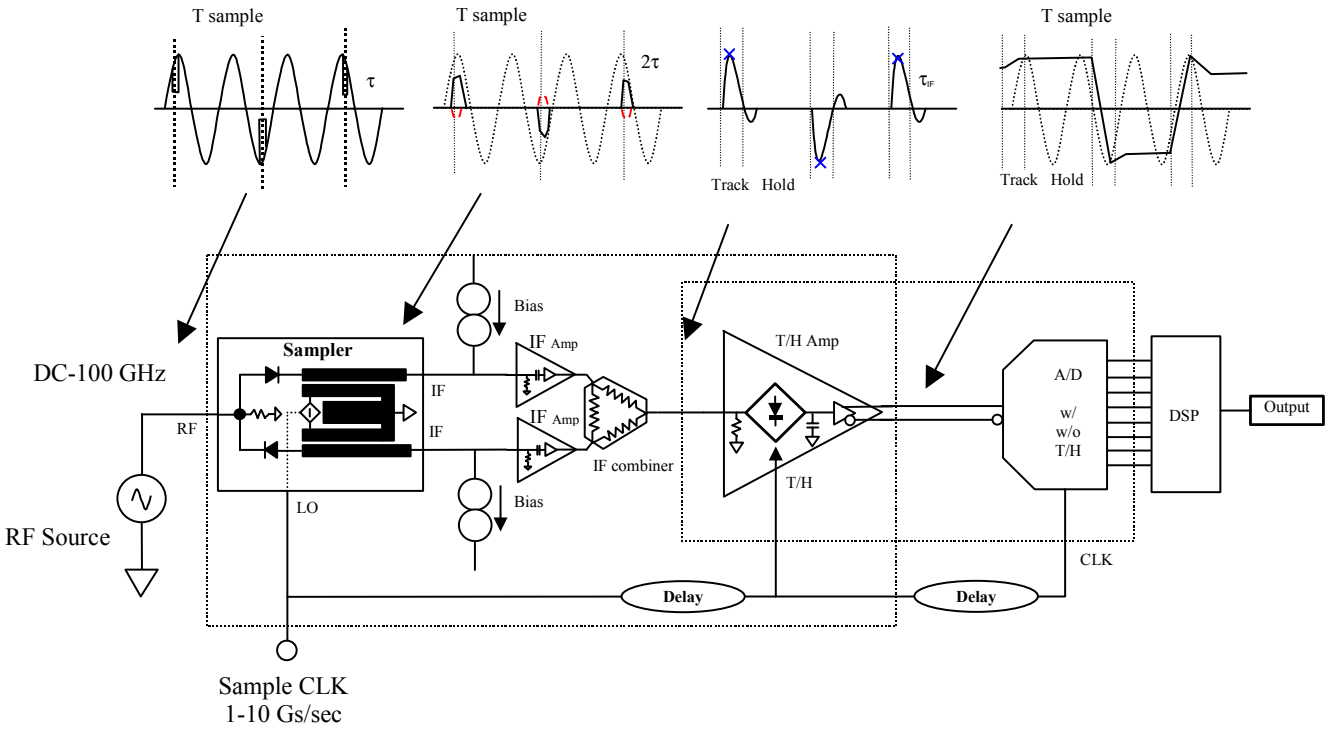


Fig 2 . " Real-time" Sampling Downconversion

Operation of the sampling downconverter in a near-Nyquist, sub-sampled situation, as depicted in Fig 2, is described below.

The LO Sample Clock edges couple to, and commutate a pair of GaAs Schottky mixer diodes which connect the RF port to the IF ports during a short aperture time. The aperture time is controlled set by the electrical length of the LO backshort. Aperture durations of 3-30 pSec are readily achievable with sampling structure dimensions ranging from 0.5-5mm. This corresponds to RF bandwidths of DC to 10-100 GHz.

A charge sample of the RF signal is captured on a transmission line section, and delivered with high pulse fidelity to the IF processing chain. The sampled signal appears as common-mode at the sampler IF ports. The sampled pulses are amplified, shaped (filtered), and combined, to provide an IF output pulse compatible with, and optimized to, the THA response.

The THA is clocked with a delayed version of the sample clock, and timed so as to capture the peaks of the IF sample pulses. The IF pulse peaks are then held by the THA for the duration of the ADC conversion cycle. The ADC is clocked at the end of the ADC conversion cycle to latch the data, and begin the next conversion cycle.

The sampling diodes are reversed biased by the IF combiner network. This reverse bias establishes the full-scale input linear operating range and increases the input dynamic range, by insuring that a full-scale RF signal not commutate the diodes without control of the LO. It also provides a means to DC offset the input linear range, and ensures a matched high-speed DC path to the sampling diodes.

The balanced structure minimizes the LO strobe radiation into the RF. Likewise, the LO signal appears at the sampler IF ports as a differential signal, and is rejected by the combiner.

By tailoring the IF signal processing to provide an "optimal filter" function, matched to the time-domain response of the Track/Hold, the system noise figure is minimized.

Independent samples of the RF input signal are resolved by the THA with nearly zero memory of the previous sample, owing to the high pulse fidelity of the IF chain.

The IF chain, by providing a fixed pulse shape to the THA, significantly reduces the effects of dynamic non-linearity in the THA, by converting its dynamic errors to correctable static errors.

The THA may be incorporated into the ADC architecture, or it may be a separate device technology from the ADC.

The sampler described above is capable of much faster sample rates than the fastest commercially available ADCs. (to >10 GS/sec). THA's in a high-speed technology like GaAs are capable of much shorter acquisition times than those incorporated into the typical high-speed ADC. An advantage of using separate high-speed THAs is that the interleaving of multiple ADCs (to increase the aggregate sample rate) is simplified. The interleave timing skew sensitivity is greatly relieved, since the sample timing is determined predominantly by the sample clock alone.

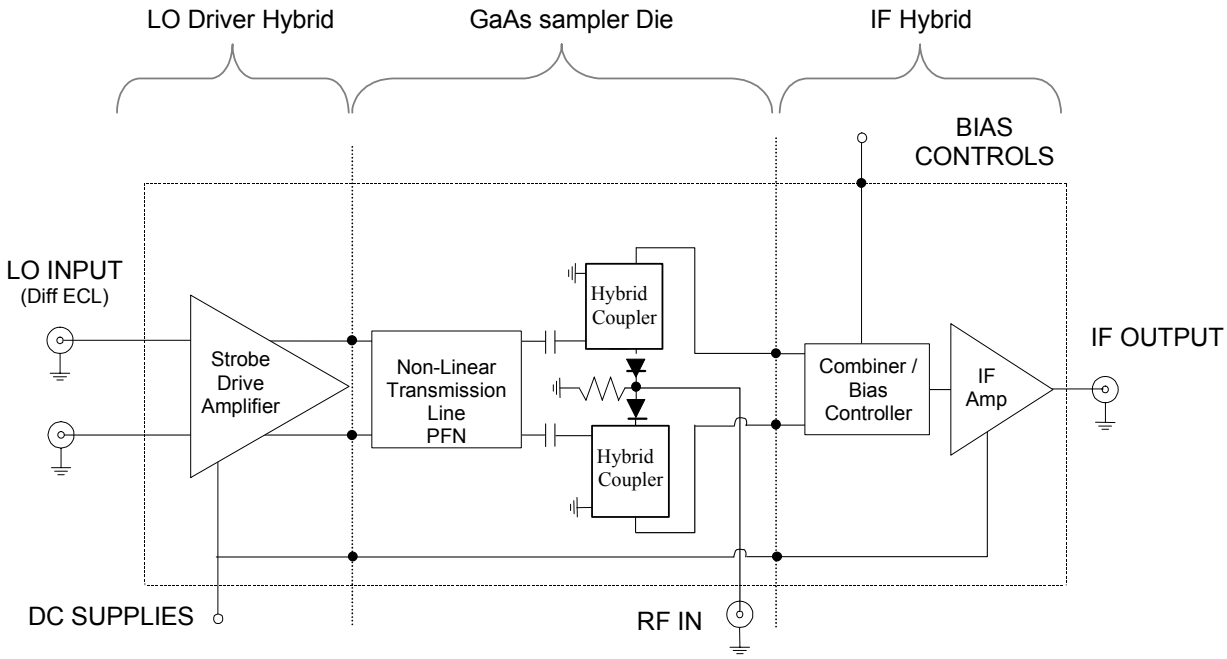


Fig 3 PSPL Wideband IF Sampler Multi-Chip-Module

IV. Sampler Technology

A multi-chip sampler module that supports DC-100GHz RF bandwidth, 10 GS/sec, and instantaneous bandwidths to > 13 GHz is shown in the block diagram in Fig. 3.

The module includes a unique traveling-wave sampling architecture, LO drive, NLTL pulse-forming network, and IF signal processing.

The LO drive hybrid includes the LO amp and balun. It drives the GaAs sampler die which contains a NLTL pulse-forming network (PFN), which in turn commutates the sampling diodes.

The sampling diodes are reverse biased through the IF combiner hybrid. This allows a wide range of control over the trade-off between noise figure, conversion loss, and linear dynamic range

The fast, large amplitude strobe pulses made possible by NLTL technology allow high input 1-dB compression levels, (10-20 dBm), which gives high input third-order intercepts (+25-+35 dBm).

Correctable static linearity errors are predominantly symmetrical, odd-order harmonics. Dynamic linearity errors are small due to very high RF bandwidths, made possible by the speed and low parasitics of the diode switches.

The coaxial RF input port is internally broadband terminated on chip.

V. Conclusion

In conclusion, a unique sampling architecture is applied to a "real time" digital radar/wideband communication receiver that allows downconversion and baseband digitizing of +/-13 GHz of mm-wave RF spectrum. Fast GaAs Schottky diode switches and NLTL pulse-forming technology are key elements for achieving high dynamic range and linearity. A detailed understanding of the residual dynamic non-linearities allows the use of unique DSP algorithms to produce breakthrough ENOB at full scale and full speed.

Acknowledgement

The author wish to acknowledge the able assistance and support of John Ebner, Agoston Agoston and Robert Norton of the PSPL Beaverton Fab and Design Group, and Joe Koebel, Program Manager at PSPL, Boulder.

References

[1] S. Pepper, "Wideband (real-rime) mm-wave sampling pulse modulator for digital radar and UWB signaling", *EuMC 2004* session, EuRAD06: UWB Techniques, Oct.15, 2004

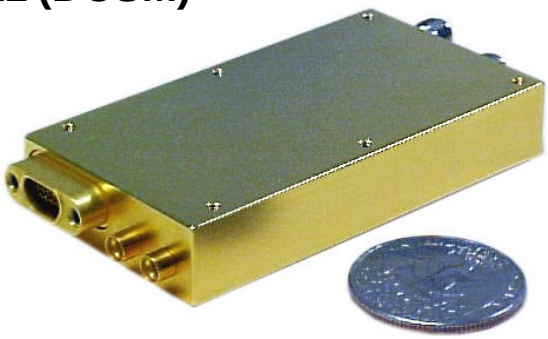
[2] http://www.picosecond.com

MODEL 7600 DOWN CONVERSION SAMPLER MODULE

PRE-RELEASE PRODUCT DATA SHEET

PSPL DOWN CONVERSION SAMPLER MODULE (DCSM)

- **Optimized for Digital Receiver Applications**
- **25 GHz RF Bandwidth**
- **Up to 2.0 GS/s Sampling Rate**
- **Harmonic levels better than -50dBc**



This is a pre-release product data sheet that captures the performance of the 7600 Down Conversion Sampler Module (DCSM). The sampler module configuration characterized here includes a two stage IF amplifier. Results show that the Picosecond Pulse Labs Down Conversion Sampler Module has consistent SFDR performance across the RF bandwidth and at sample rates of up to 2.0 GS/s. The Down Conversion Sampler Module is being optimized for digital receiver applications where it is critical to maintain exceptional linearity performance.

7600 DCSM - Preliminary Electrical Specification					
Parameter	**Min**	**Typical**	**Max**	**Units**	**Comments**
RF Bandwidth		25		GHz	DC to >25GHz
Sampling Rate	DC		2.0	GS/s	
Harmonic Distortion [1] At 0dBm RF Input			-50	dBc	Refer to compiled data on page 3
Input Referred Noise [1]		3.5		mV_{RMS}	Single Shot
Aperture Jitter		TBD	250	fs_{RMS}	with respect strobe input (limited by measurement system)
Max RF Input			+10	dBm	
LO Strobe Input (single ended):					
Slew Rate	6			mV/ps	400mV square wave recommended (ECL)
Impedance		50		ohm	AC coupled
IF Output					Single Ended, Analog
Conversion Gain [1]		-6		dB	Less than 10 GHz
Bandwidth [1]			1.8	GHz	
Strobe-to-IF throughput Delay [1]		TBD		ns	
Power Dissipation [1]		4.5	5.5	W	
Operating Case Temperature	-40		80	C	Recommended range for optimal performance
Storage Temperature Range	-55		125	C	

[1] Performance parameter is subject to change with variations made to the IF amplifier subsystem. This configuration includes a two stage IF amplifier.

DCSM TEST DATA SUMMARY

Figures 1 and 2 contain representative test data of the typical SFDR performance for a digital receiver using a 7600 DCSM.

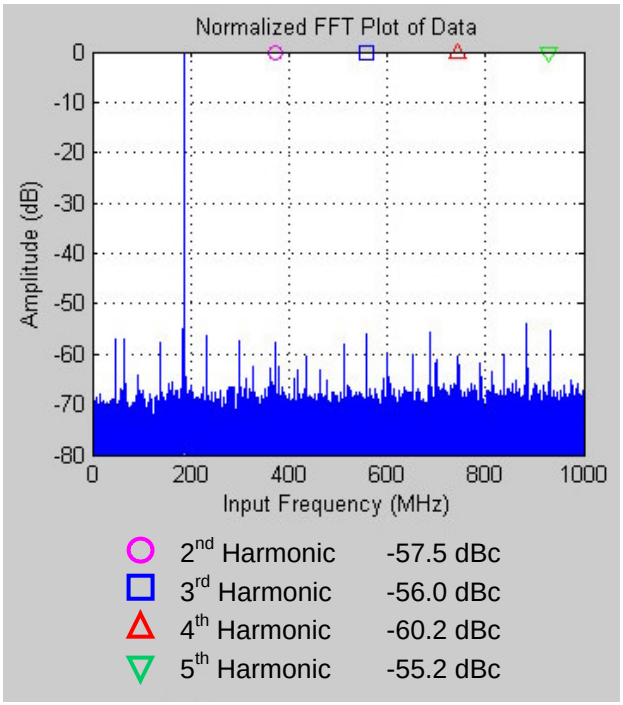


Figure 1: SFDR for 14GHz RF Input (0dBm)

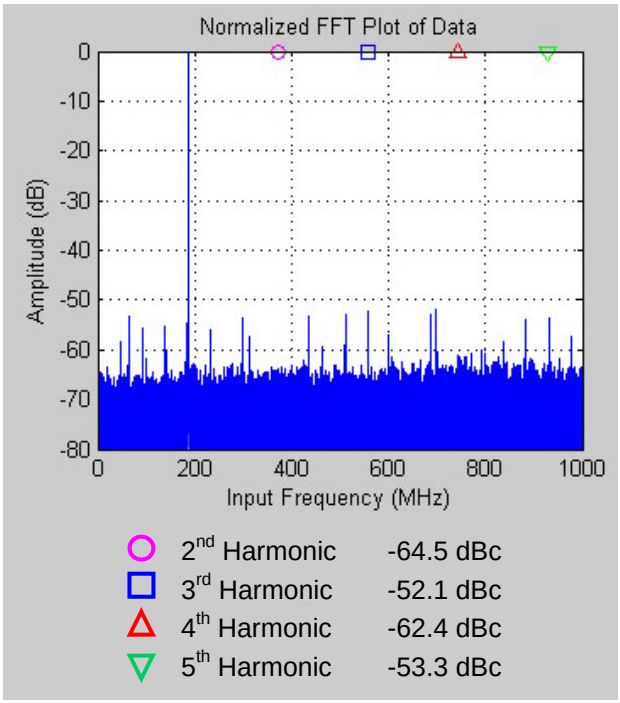


Figure 2: SFDR for 24GHz RF Input (0dBm)

Figure 3 shows how the SFDR of the 7600 DCSM varies as a function of both RF Input frequency and the IF bandwidth of the device under test.

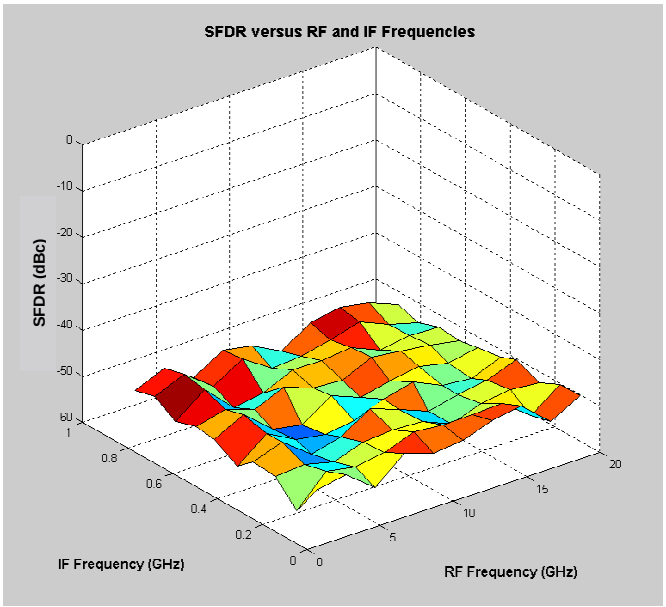


Figure 3: SFDR vs. RF Frequency (0dBm) and IF Bandwidth

DEFINITION OF DCSM TEST SYSTEM

The Picosecond Pulse Labs 7600 series of Down Conversion Sampling Modules (DCSM) leverages patented Non-Linear Transmission Line (NLTL) technologies and proprietary high-voltage diode construction techniques to achieve consistent linearity performance over a broad DC to 25 GHz RF bandwidth and at sampling rates of 10 Ms/s to greater than 2 Gs/s.

The test system used to evaluate the 7600 DCSM is designed to primarily demonstrate the SFDR (spurious free dynamic range) of the device. The test system is VME based, although the 7600 DCSM is a product that can be incorporated into virtually any platform.

As shown in Figure 4, the test system consists of a VME chassis, a high frequency RF synthesizer; and a laptop PC (for performing digital data FFT operations, data analysis and sending system commands).

The VME chassis contains 3 boards:

1. **Clock Board** provides the LO drive signal for the DCSM and the corresponding timing signal for the ADC trigger points. Test conditions are all performed at a clock rate of 2GHz (2Gs/s).
2. **Processor Board** contains an ATMEL 10bit, 2 Gs/s ADC (PN: TS83102G0B) and a microprocessor for data acquisition.
3. **Down Conversion Board** contains the 7600 DCSM with appropriate IF amplifiers.

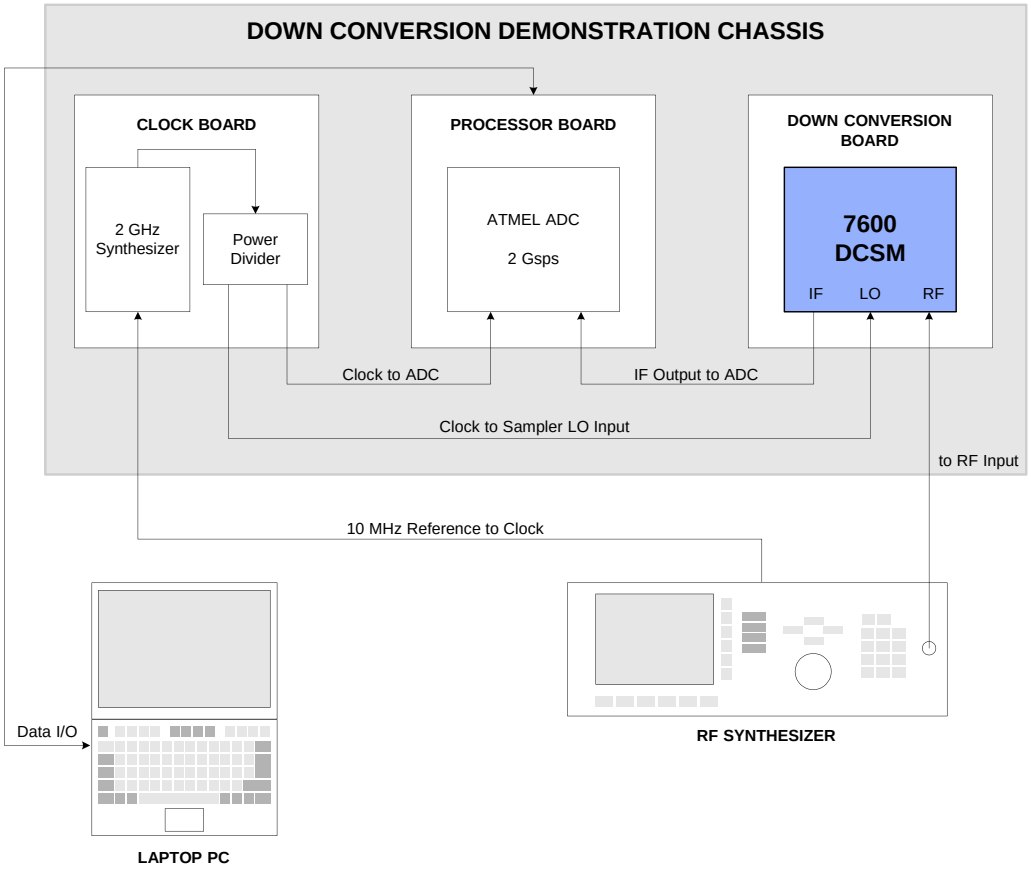


Figure 4: 7600 DCSM Test System Configuration

Features

- **Up to 2 Gsps Sampling Rate**
- **Power Consumption: 4.6 W**
- **500 mVpp Differential 100 Ω or Single-ended 50 Ω (±2 %) Analog Inputs**
- **Differential 100 Ω or Single-ended 50 Ω Clock Inputs**
- **ECL or LVDS Output Compatibility**
- **50 Ω Differential Outputs with Common Mode not Dependent on Temperature**
- **ADC Gain Adjust**
- **Sampling Delay Adjust**
- **Offset Control Capability**
- **Data Ready Output with Asynchronous Reset**
- **Out-of-range Output Bit**
- **Selectable Decimation by 32 Functions**
- **Gray or Binary Selectable Output Data; NRZ Output Mode**
- **Pattern Generator Output (for Acquisition System Monitoring)**
- **Radiation Tolerance Oriented Design (More Than 100 Krad (Si) Expected)**
- **CBGA 152 Cavity Down Hermetic Package**
- **CBGA Package Evaluation Board TSEV83102G0BGL**
- **Companion Device: DMUX 8-/10-bit 1:4/1:8 2 Gsps TS81102G0**

Performance

- 3.3 GHz Full Power Input Bandwidth (-3 dB)
- Gain Flatness: ± 0.2 dB (from DC up to 1.5 GHz)
- Low Input VSWR: 1.2 Max from DC to 2.5 GHz
- SFDR = -59 dBc; 7.6 Effective Bits at F_S = 1.4 Gsps, F_{IN} = 700 MHz [-1 dBFS]
- SFDR = -53 dBc; 7.1 Effective Bits at Fs = 1.4 Gsps, F_{IN} = 1950 MHz [-1 dBFS]
- SFDR = -54 dBc; 6.5 Effective Bits at F_S = 2 Gsps, F_{IN} = 2 GHz [-1 dBFS]
- Low Bit Error Rate (10^{-12}) at 2 Gsps

Application

- Direct RF Down Conversion
- Wide Band Satellite Receiver
- High-speed Instrumentation
- High-speed Acquisition Systems
- High-energy Physics
- Automatic Test Equipment
- Radar

Screening

- Temperature Range for Packaged Device:
  - "C" grade: 0° C < Tc; Tj < 90° C
  - "V" grade: -20° C < Tc; Tj < 110° C
- Standard Die Flow (upon Request)

Description

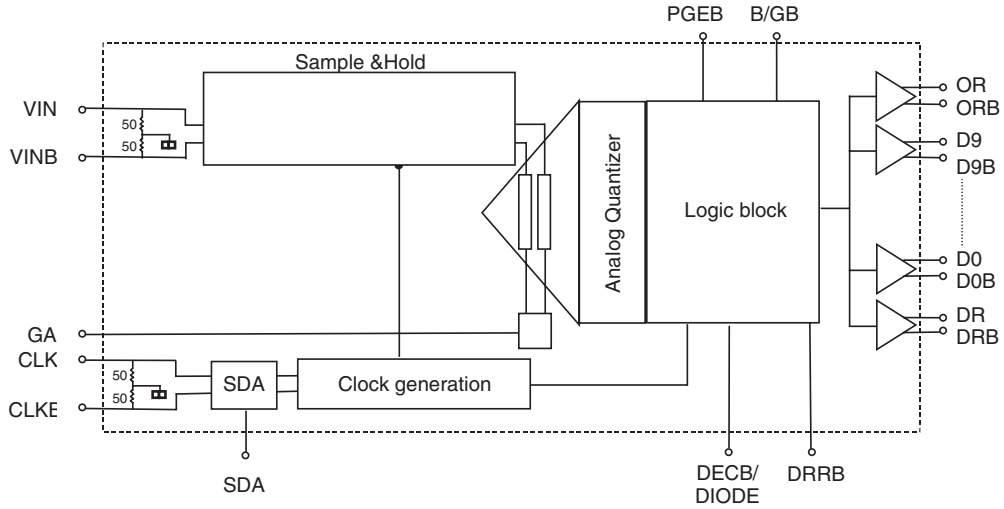
The TS83102G0B is a monolithic 10-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 2 Gsps. It uses an innovative architecture, including an on-chip Sample and Hold (S/H). The 3.3 GHz full power input bandwidth and band flatness performances enable the digitizing of high IF and large bandwidth signals.

10-bit 2 Gsps ADC

TS83102G0B

2101D–BDC–06/04

Figure 1. Simplified Block Diagram



Functional Description

The TS83102G0B is a 10-bit 2 Gsps ADC. The device includes a front-end master/slave Track and Hold stage (Sample and Hold), followed by an analog encoding stage (Analog Quantizer), which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuit and resynchronization stage, followed by 50 Ω differential output buffers.

The TS83102G0B works in a fully differential mode from analog inputs to digital outputs. A differential Data Ready output (DR/DRB) is available to indicate when the outputs are valid and an Asynchronous Data Ready Reset ensures that the first digitized data corresponds to the first acquisition.

The control pin B/GB (A11 of the CBGA package) is provided to select either a binary or gray data output format. The gain control pin GA (R9 of the CBGA package) is provided to adjust the ADC gain transfer function.

A Sampling Delay Adjust function (SDA) may be used to ease the interleaving of ADCs.

A pattern generator is integrated on the chip for debug or acquisition setup. This function is activated through the PGEB pin (A9 of the CBGA package).

An Out-of-range bit (OR/ORB) indicates when the input overrides 0.5 Vpp.

A selectable decimation by 32 functions is also available for enhanced testability coverage (A10 of the CBGA package), along with the die junction temperature monitoring function.

The TS83102G0B uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allows enhanced radiation tolerance (over 100 kRad (Si) total dose expected tolerance).

Typical Reconstructed Signals and Signal Spectrum

The ADC input signal is sampled at a full sampling rate, but the output data is 8 or 16 times decimated so as to relax the acquisition system data rate. As a consequence, the calculation software sees an effective frequency divided by 8 or 16, compared to the ADC clock frequency used (Fs). The spectrum is thus displayed from DC to Fs/2 divided by the decimation factor.

Decimation only folds all spectral components between DC and Fs/2 divided by the decimation factor but does not change their amplitude.

This does not have any impact on the FFT spectral characteristics because of the ergodicity of the samples (time average = statistic average). The input frequency is chosen to respect the coherence of the acquisition.

Figure 17. Fs = 1.4 Gsps and Fin = 702 MHz, -1 dBFS; Decimation Factor = 16, 32 kpoints FFT

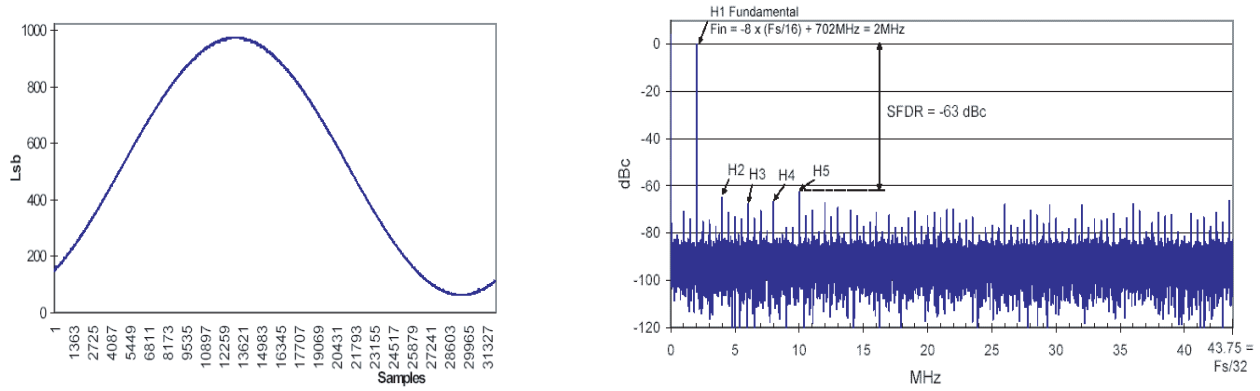


Figure 18. Fs = 1.4 Gsps and Fin = 1399 MHz, -1 dBFS; Decimation Factor = 16, 32 kpoints FFT

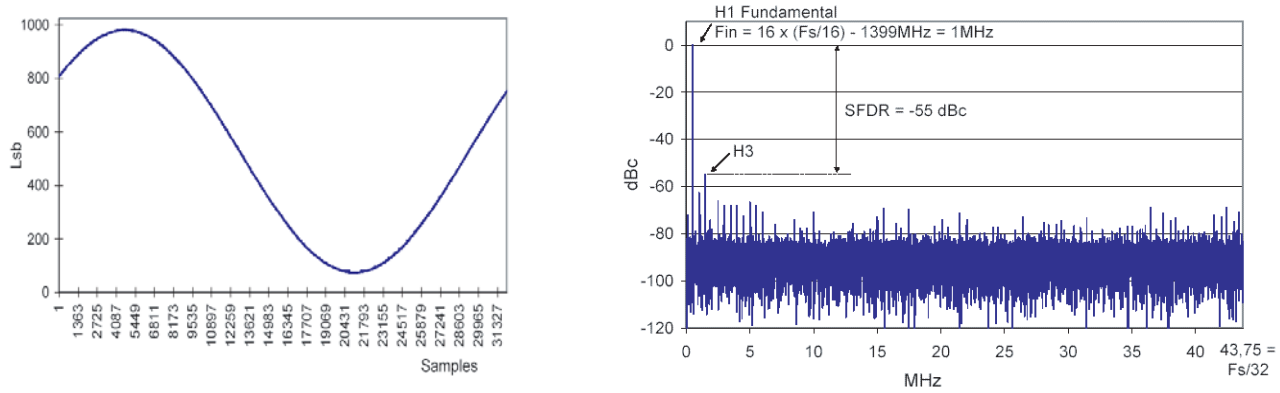


Figure 19. Fs = 1.7 Gsps and Fin = 898 MHz, -1 dBFS; Decimation Factor = 16, 32 kpoints FFT

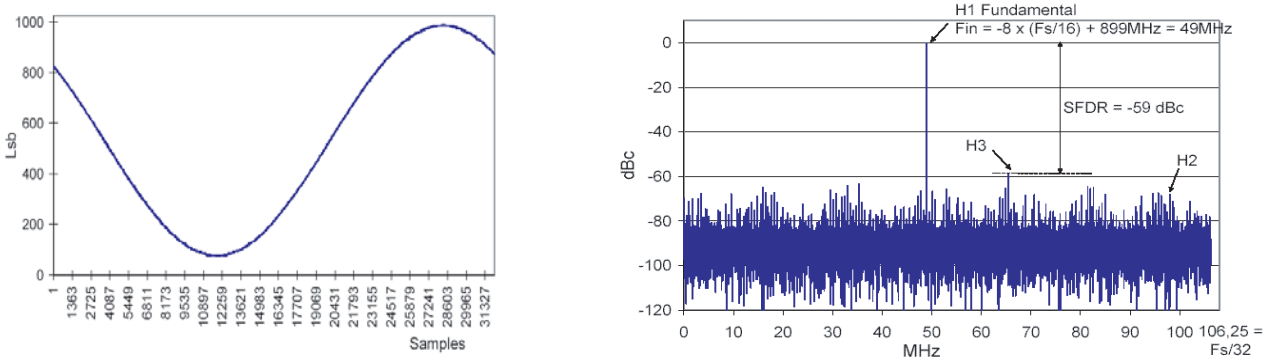


Figure 20. Fs = 1.7 Gsps and Fin = 1699 MHz, -1 dBFS; Decimation Factor = 8, 32 kpoints FFT

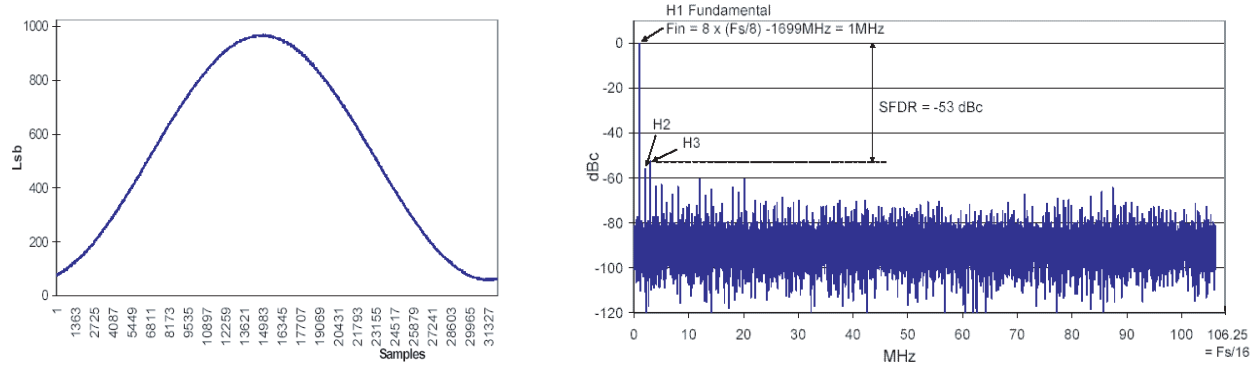
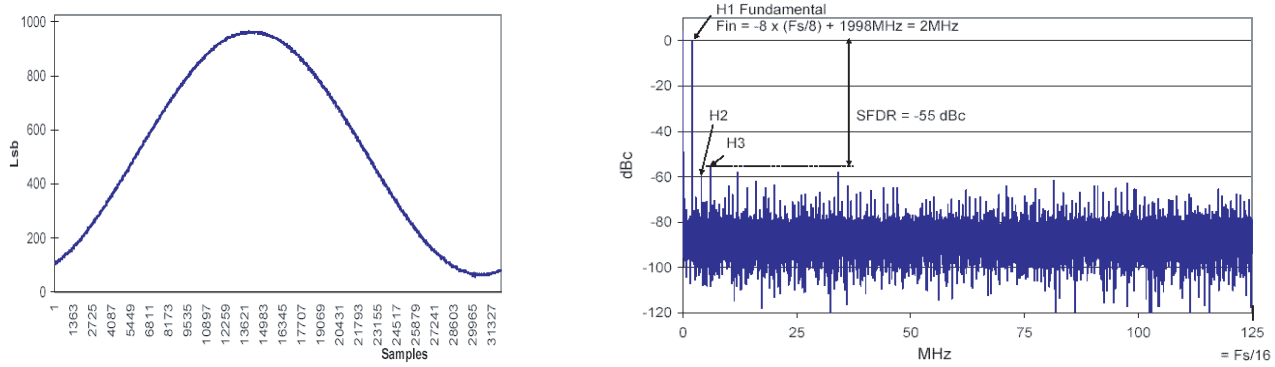
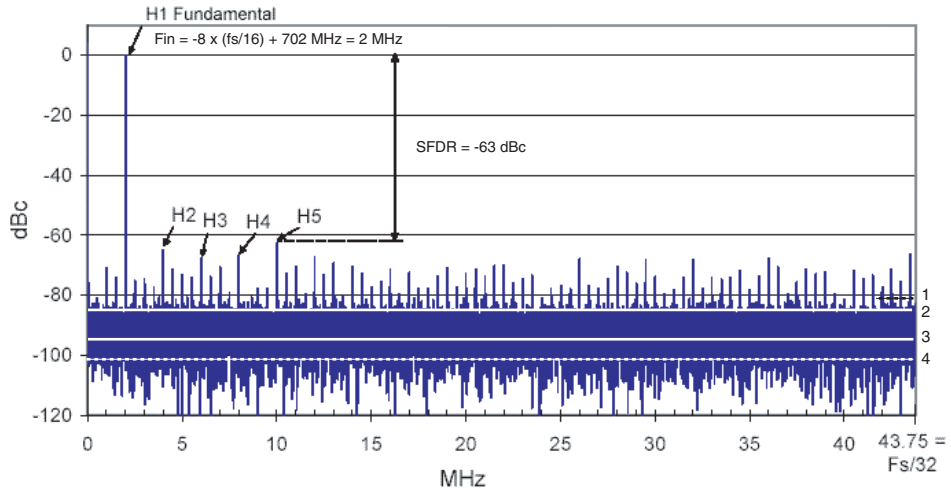


Figure 21. Fs = 2 Gsps and Fin = 1998 MHz, -1 dBFS; Decimation Factor = 8, 32 kpoints FFT



Considerations on ENOB: Linearity and Noise Contribution

Figure 33. Example of a 16-kpoint FFT Computation at Fs = 1.4 Gsps, Fin = 702 MHz, -1dBFS, T_J = 80°C; Bin Spacing = (Fs/2) / 16384 = 2.67 kHz



This is a 16384 points FFT. It is 16 times decimated since a DEMUX 1:8 is used to relax the acquisition system data rate, and data is captured on the rising edge of the data ready signal.

The spectrum is computed over the first Nyquist zone from DC to Fs/2 divided by the decimation factor, which equals Fs/32 = 43.75 MHz.

Legend:

1. Ideal 10-bit quantization noise spectral density, peak value = -84 dB
2. Average SNR noise floor: 47 dB + 10 log ($N_{FFTpoint}$/2) = 86 dB including thermal noise
3. Average SNR noise floor: 57 dB + 10 log ($N_{FFTpoint}$/2) = 96 dB without thermal noise
4. Ideal 10-bit averaged SNR noise floor 6.02 x (N = 10) + 1.76 + 10 log ($N_{FFTpoint}$/2) = 101 dB

Note: The thermal noise floor is expressed in dBm/Hz (at T = 300 K, B = 1 Hz): 10 log (kTB/1 mW) = -174 dBm/Hz or -139.75 dBm/2.67 kHz. THD is calculated over the 25 first harmonics.

With ADC input referred thermal noise:

- ENOB = 7.6 bits
- SINAD = 47 dB
- THD = -55.7 dB (over 25 harmonics)
- SFDR = -62.6 dBc
- SNR = 47.3 dB

Without ADC input referred thermal noise:

- ENOB = 9.2 bits
- SINAD = 57 dB
- THD = -55.7 dB (over 25 harmonics)
- SFDR = -62.6 dBc
- SNR = 57.3 dB

Conclusion:

Though the ENOB is 7.6 bits (in this example at 1.4 Gsps Nyquist conditions), the ADC features a 10-bit linearity regarding the 60 dB typical SFDR performance.

However, it has to be pointed out that the ENOB is actually limited by the ADC's input referred thermal noise, which dominates the rms quantization noise. For certain applications (using a spread spectrum) the signal may be recovered below the thermal noise floor (by cross correlation since it is white noise).

Therefore, the thermal noise can be extracted from the ENOB: the ENOB without a referred input thermal noise is 9.2 instead of 7.6 in this example, only limited by the quantization noise and clock induced jitter.