

Received October 7, 2019, accepted October 22, 2019, date of publication October 25, 2019, date of current version November 7, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2949701

Theory of Quantization-Interleaving ADC and Its Application in High-Resolution Oscilloscope

JIAN GAO¹, PENG YE^{1,2}, HAO ZENG¹, ZHIXIANG PAN¹,
YU ZHAO¹, HAO LI¹, AND JIE MENG¹

¹School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China

²Department of Research and Development, Uni-Trend Technology (China) Company Ltd., Dongguan 523000, China

Corresponding author: Hao Zeng (zenghao@uestc.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61701077, Grant 61501087, and Grant 61801092, and in part by the Dongguan Introduction Program of Leading Innovative and Entrepreneurial Talents.

ABSTRACT The pursuit of high sampling rates and high bandwidth is a long-term theme for oscilloscopes. Recently, accurate test requirements and advanced technology have driven high-resolution oscilloscopes to be a new appeal in both research and industry. Previous high resolution acquisition methods either obtain more bits by reducing the sampling rate or work with many restrictions. In this paper, we propose a novel architecture where parallel ADC is used in quantization interleaving ADC (QIADC) manner, to achieve more bits of resolution. Both the on-chip implementation and the off-chip implementation are presented in a straightforward manner. Although the proposed schemes are different, they have exactly the same effect on resolution enhancement. Based on the basic theory of quantization-sampling model, the principle of QIADC is explained in statistical domain. Furthermore, we derive an explicit expression of enhanced bit. To achieve the goal of both high sampling rate and resolution, a dual channel QIADC oscilloscope prototype is designed and the effectiveness of the proposed method is demonstrated. Experimental results show that i) Smaller signals can be identified and the dynamic range of the system is significantly improved by 5.7dB; ii) The effective number of bits (ENOB) has an improvement of 0.5-bit at multiple frequency points in the 1 GHz band; iii) A higher precision waveform capture is provided through arbitrary waveform test. Finally, the utilization and power overhead of proposed QIADC is also analyzed in this paper.

INDEX TERMS Data acquisition, quantization, statistics analysis, oscilloscope, resolution enhancement.

I. INTRODUCTION

With the persistent development of modern telecommunication systems, aerospace equipment and radar transceivers, the capture of complex signals in these systems has become a major challenge. Digital storage oscilloscope (DSO), which is a core instrument that ensures the observation and analysis of complex signals, has been widely employed in faults diagnosing during design and capture anomalies [1]–[5]. On the other hand, sampling rate and bandwidth are the key competencies of DSO, because these two indicators are important attractions for users. So the studies on these the above indicators will last long-term in the field of measurement and instrumentation.

The significance of the measurement lies in the feedback to the real situation. In some specific cases, such as recording

The associate editor coordinating the review of this manuscript and approving it for publication was Cihun-Siyong Gong.

high-resolution radar signals or high-energy physics experiments [5], the oscilloscope resolution is very important since waveform capture with more resolution means more accurate description of the signal. But due to limitation of processing ability, traditional DSO has 8-bit resolution typically. Recently, the progress of computer computing and storage capability has driven the birth of high-definition oscilloscope. Therefore, the research of high-precision or high-resolution DSO has become a fresh point of practical applications [6], [7].

In this paper, our goal is to design a high-resolution oscilloscope with ultra-fast sample rate. So, those classical methods that use speed to exchange resolution, such as sigma-delta modulators ($\Sigma - \Delta$) [8], [9], digital-based averaging techniques [10]–[12] and FIR or IIR filters [13]–[15] are neglected in this paper. To achieve our goal, we investigate the resolution-enhanced solutions for high speed acquisition systems that break through the resolution of single ADC and

achieve resolution improvement through parallel acquisition architecture. We will first review the mainstream architectures with high bandwidth, high sample rate and high resolution acquisition purposes, and analyze the pros and cons of these methods.

A typical method used to realize the required high-speed technique involves the time-interleaved ADC (TIADC), which uses multiple ADCs with same sampling rate to acquire the same signal at different time instant. A significant advantage of this parallelism is the relaxation of the time speed on each channel. Therefore, the design of each channel is easier. However, any small channel mismatch between sub-ADCs will cause gain and phase error that results in significant performance degradation. Therefore, error estimation and calibration methods have been proposed to suppress the spurious components and restore the dynamic performance of sub-ADCs. Specifically, the mixed signal compensation [16]–[18] and blind signal calibration techniques [19], [20] have been extensively studied. Besides, digital bandwidth interleaving (DBI) and asynchronous time interleaving (ATI) techniques enlarge the sampling rate and digital bandwidth by frequency interleaving as reported in [21]–[23], but the challenge is the frequency response equalization problem for filter banks [24].

If the aforementioned techniques are methods to expand the acquisition performance in horizontal dimension, a parallel sampling technique referred to time-synchronized ADC (TSADC) [25], [26] is to pursue performance improvement in vertical dimension. And a hybrid acquisition architecture utilizing both the horizontal and vertical expansion is also found in [27]. With the advantages of enhancing dynamic range and effective number of bits (ENOB), TSADC has been reported in [25]–[28]. A typical report in [25] first proved that the uncorrelated noise can be reduced in TSADC; further in [26], the combined impact of signals, harmonics and noise and their correlation has been investigated in depth. However, TSADC still has theoretical limitations in terms of the nature of resolution enhancement and its applicable constraints. In [29], the author indicated the applicable premise requires standard deviation of noise large than the least significant bit (LSB) of ADC.

As a step towards our ultimate goal, this paper studies theoretical issues of the quantization process of ADC and parallel ADC. We will propose a novel resolution-enhanced method referred to quantization-interleaved ADC (QIADC). Under the background of quantization-sampling theorem which has been proposed by Widrow *et al.* in [30], we derive an explicit formula for the enhanced effects of the proposed architecture from a statistical point of view. Furthermore, we take the design of a dual channel prototype as an example, and the implementation of QIADC is set up to show the resolution improvement from three experiments. Finally, the power consumption is also analyzed. The results show that the cost of resources and power consumption is very small compared to the contribution in resolution of this method.

The contributions of our work therefore can be concluded as: i) A resolution-enhanced architecture is proposed and two QIADC schemes are given. ii) Using quantization-sampling model, the core quantization theorem based on QIADC is given and proven. The theory of the proposed QIADC also further extends this model. iii) An oscilloscope prototype of a dual channel QIADC is implemented, we verify both the feasibility and correctness of QIADC. To this end, an oscilloscope with both ultra-fast sample rate and high resolution is designed when the performance of a single device is limited.

The rest of this paper is organized as follows: Section II reviews the quantization theory from a statistical perspective, which is the fundamental of QIADC model; Section III focuses on the proposed QIADC architecture and explains the principle of improvement; Next, a high resolution oscilloscope prototype based on dual channel QI structure is designed, details of the implementation are introduced in Section IV; In Section V, experiments are conducted to demonstrate the effectiveness of QIADC; Finally, a brief conclusion of this paper is given in Section VI.

II. REVIEW OF QUANTIZATION THEORY

In this section, a brief review of the quantizing-sampling theorem will be demonstrated. In the time or frequency domain, quantization is a nonlinear problem that is difficult to analyze by using linear theory. However, from a statistical view, the analysis of quantization process is an easy problem. As first proposed in [30], non-linear quantization theory is analogous to the analysis of signal sampling theorem. Therefore, we first review the fundamental theory of quantization and its statistical model.

A. DEFINITION AND DENOTATION

If we observe the baseline of the oscilloscope in a period as ensemble samples, each baseline at different times is a random noise signal. The histogram result of the amplitude at certain time is a random variable, shown in Fig. 1 (a).

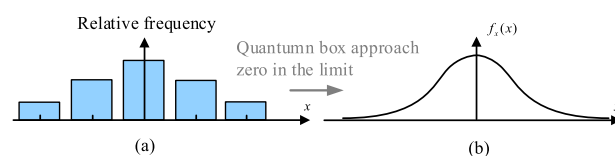


FIGURE 1. Derivation of a histogram: (a) histogram of x that indicates the relative frequency of the samples falling within the given quantum box; (b) when limit the bar width of histogram to zero, the PDF of x is continuous.

The relative frequency of each bar equals the probability of event occurring within a given quantum box. When the width of quantum box approaches infinitely small, the histogram becomes a continuous function $f(x)$ in the limit state, sketched in Fig. 1 (b). Therefore, the probability density function (PDF) of signal $x(t)$ is denoted as $f(x)$. Note that, the area covered by $f(x)$ is unit.

When each sample quantized by a quantizer, the actual amplitude is rounded to a fixed set of values, which are

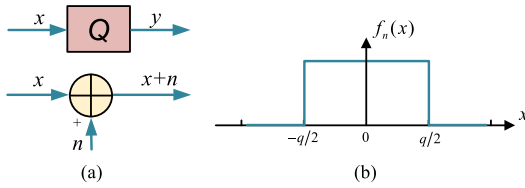


FIGURE 2. Equivalent model of quantization: (a) simplified model of the quantizer; (b) PDF of quantization noise.

usually encoded as words of finite length. Thus, the quantization process causes accuracy loss unavoidably. Quantization loss or quantization noise can be modled as an additive noise to the original signal [30], shown in Fig. 2 (a). The impact of a quantizer is modeled by an additive, independent noise, uniformly distributed in $[-q/2, q/2]$, where q is LSB. Therefore, its pdf $f_n(x)$ has a uniform distribution, sketched in Fig. 2(b).

It is well known that, when two independent random variables are added, the PDF of the summation results is a convolution of the PDFs of the two independent random variables. Therefore, we calculate the convolution of $f_x(x)$ and $f_n(x)$, and obtain the real PDF of the quantized signal. The convolved PDF is written by

$$\begin{aligned}
 f_{\hat{x}}(x) &= f_x(x) * f_n(x) \\
 &= \int_{-\infty}^{\infty} f_x(\alpha) f_n(x - \alpha) d\alpha \\
 &= \int_{x-q/2}^{x+q/2} f_x(\alpha) \cdot \frac{1}{q} d\alpha.
 \end{aligned} \tag{1}$$

where $*$ is convolution operator.

B. STATISTICAL MODEL OF QUANTIZATION

Based on the concepts of original PDF, quantization noise PDF and convolved PDF, we introduce an important model of quantization-sampling.

The quantizer discrete the continuous voltages to a set of quantized values, always expressed as sample code. Thus, if the signal is in the scale of reference voltage of N -bit ADC, the effect of quantizer is a sampling impulse train that uniformly distributed on the horizontal axis with interval of $q = 2^{-N}$, shown in Fig. 3 (d), which is represented by

$$p(x) = q \sum_{m=-\infty}^{\infty} \delta(x - mq). \tag{2}$$

The multiplication operation between impulse and convolved PDF yields an impulse train of varying weights

$$\begin{aligned}
 f_y(x) &= f_{\hat{x}}(x) \cdot p(x) \\
 &= \int_{x-q/2}^{x+q/2} f_x(\tau) \frac{1}{q} d\tau \cdot \sum_{m=-\infty}^{\infty} q \cdot \delta(x - mq) \\
 &= \sum_{m=-\infty}^{\infty} w_m \cdot \delta(x - mq),
 \end{aligned} \tag{3}$$

where weight of the m th pulse is $w_m = \int_{mq-q/2}^{mq+q/2} f(\alpha) d\alpha$.

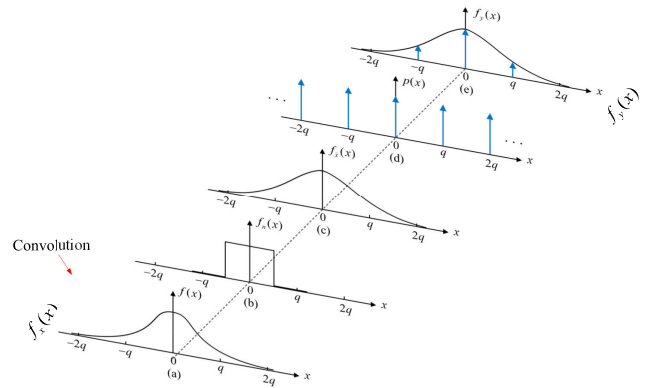


FIGURE 3. Formulation of quantization process in PDF domain (a) PDF of original input x ; (b) PDF of quantization noise n ; (c) Convolved PDF of $f_x(x)$ and $f_n(x)$; (d) A uniformly distributed impulse train; (e) Product of $f_{f_x(x) * f_n(x)}$ and $p(x)$ which is the PDF of quantized signal y .

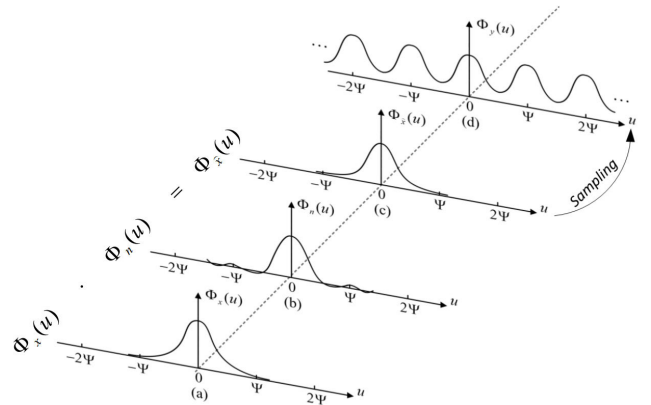


FIGURE 4. Formulation of quantization process in CF domain (a) CF of original input x ; (b) Sinc function, CF of quantization noise n ; (c) Product of $\Phi_x(u)$ and $\Phi_n(u)$; (d) CF of quantized signal y , periodic repetition of (c) with period of Ψ .

Fig. 3 shows the process of quantization. It can be found that the quantizer is a sampler in the statistics domain, which is analogous to the sampler of signal in time domain.

C. CHARACTERISTIC FUNCTION

The characteristic function (CF) that is the Fourier transform of PDF can be defined as

$$\Phi_x(u) = \int_{-\infty}^{\infty} f_x(x) e^{jux} dx. \tag{4}$$

The input CF is sketched in Fig. 4 (a). In general, a Gaussian distribution has a same envelope in transform domain. Accordingly, the CF of quantization noise is calculated as

$$\begin{aligned}
 \Phi_n(u) &= \int_{-\infty}^{\infty} f_n(x) e^{jux} dx \\
 &= \int_{-q/2}^{q/2} \frac{1}{q} e^{jux} dx \\
 &= \text{sinc}\left(\frac{qu}{2}\right),
 \end{aligned} \tag{5}$$

where $\text{sinc}(u) = \sin(u)/u$. In Fig. 4 (b), a sinc function is pictured and this corresponds to the PDF of Fig. 4 (b). On the reference of convolution property, the convolution of PDFs yields the product of the CFs. Therefore, the convolved PDF can be represented by $\Phi_{\hat{x}}(u) = \Phi_x(u) \cdot \Phi_n(u)$, shown in Fig. 4(c).

Using eq. (4), we derive the CF of impulse train as a new train of impulses in CF domain, that is

$$\Phi_p(u) = \Psi \sum_{k=-\infty}^{\infty} \delta(u - k\Psi). \quad (6)$$

where, period interval of quantization frequency is $\Psi = 2\pi/q$. Again using the convolution property, the sampling in PDF domain provides the convolution of $\Phi_{\hat{x}}(u)$ and $\Phi_p(u)$ in CF domain. Fig. 4 (d) illustrates $\Phi_{\hat{x}}(u)$ produces periodically repetition, which holds

$$\begin{aligned} \Phi_y(u) &= \Phi_{\hat{x}}(u) * \Phi_p(u) \\ &= \Psi \sum_{k=-\infty}^{\infty} \Phi_x(u - k\Psi) \cdot \text{sinc} \left[\frac{q \cdot (u - k\Psi)}{2} \right]. \end{aligned} \quad (7)$$

Next, we discuss the relationship between sampling model in time domain and quantization model in statistics domain. The sampled signal holds the periodic spectrum. Instead of repeated with period of $\Omega = 2\pi/T$ in time domain, $\Phi_{\hat{x}}(u)$ is repeated with a period of quantization frequency $\Psi = 2\pi/q$. This reveals similarity of sampling theorem. The difference of two theories is the basic symbolic expression of the sampling period T and the LSB q . This is because that the domain of analysis is different.

III. QUANTIZATION INTERLEAVING ARCHITECTURE

In this section, a novel QIADC is proposed to achieve higher quantization resolution. We first demonstrate two types of general scheme which are typical implementations. Then use a two channel structure as an example to explain the principle based on the previous quantization-sampling theorem. Finally, we propose the core contribution of this architecture.

A. TWO TYPE OF QIADC STRUCTURE

Traditional oscilloscope directly sends the signal to ADC for sampling and quantization. This leads the resolution of acquisition same as individual ADC. We now extend it to parallel $M > 1$ channels and more bits can be obtained through the structure referred to QIADC.

Fig. 5 depicts the overall scheme of the proposed structure. The proposed QIADC structure consists of M separate individual channels which use an ADC with same resolution of N -bit and same sampling rate. The ADCs driven by a same clock source are normally working simultaneously. Signal flow is shown with the arrow in this diagram, where the input signal is sampled at the Nyquist frequency. First, the analog input goes into a power splitter driver that divides the input x into M identical sub signals.

Different from traditional direct sampling, the first operation is adding different offset value inside ADC before the

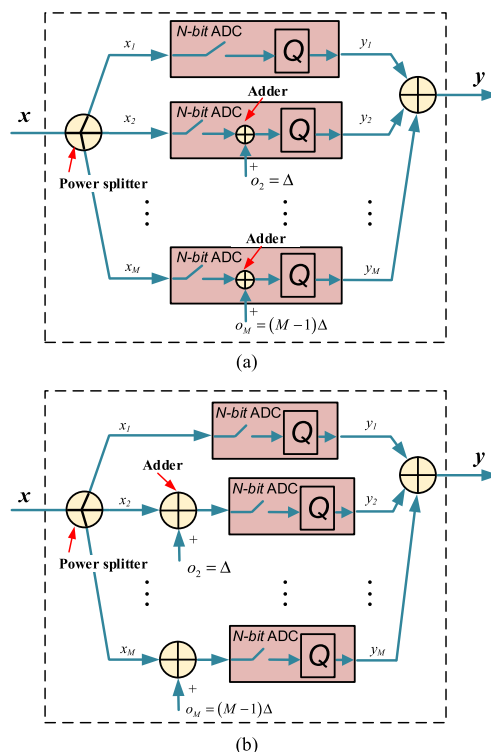


FIGURE 5. Structure of QIADC (a)Form I, the offset is added inside ADC, changing the conversion function of each quantizer. (b) Form II, the offset is added outside ADC, biased signal is quantized by the M quantizers with same conversion function.

signal is sent to quantizer, shown in Fig. 5 (a). For the m th channel input, the fractional offset is $o_m = (m - 1)\Delta$, where $m \in [1, M]$ and Δ is the $1/M$ fractional of q , i.e., $\Delta = q/M$. The added offset shifts the characteristics of each quantizer by o_m . When the signals of M channels are quantized, high-speed data of multiple channels are added to obtain one result. This is the second operation in this architecture. The output of the architecture enhances data resolution, and the number of enhancement bits is directly related to the number of channels.

The type of adding offset inside ADC is called form I. In form I, the offset is added to the quantizer, which changes the conversion function of each quantizer. However, for some board-level designs, the internal operation of the ADC is difficult to achieve and the accuracy is poor. So form II is proposed to solve this problem. In Form II, the offset is added to signal before sent to ADC, and M ADCs quantize biased signal. The difference is the addition offset outside ADC, but it actually remains the same improvement in quantization. The explicit improvement will be explained in next subsection.

B. A TWO CHANNEL EXAMPLE

The principle of the proposed architecture can be explained by a two channel QIADC using the quantization-sampling model. This theory also provides further insight of quantization-sampling model.

Let an arbitrary convolved PDF of input signal $f_{\hat{x}}(x)$ as shown in Fig. 6 (a). The quantizer of the first channel samples

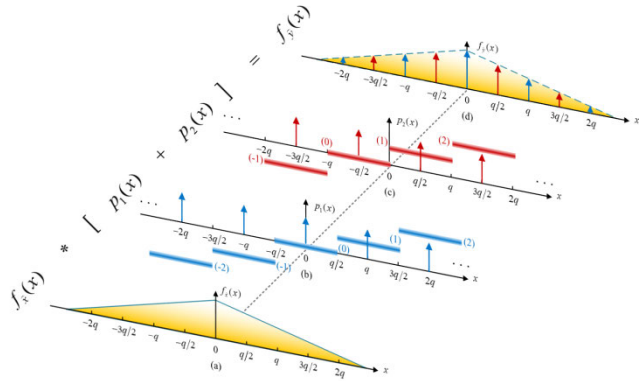


FIGURE 6. Formulation of the QIADC in PDF domain (a) PDF of input, convolution of original signal and quantization noise; (b) Impulse train of original quantizer; (c) Impulse train of shifted quantizer; (d) Sum of the PDF of two quantizers, the envelope is same as (a).

the PDF with impulse train of $p_1(x)$. Each code band projects onto the x -axis and generates an impulse that locates at the center of a code strip. General mid-tread quantizer has $(2^N - 1)$ code bands that quantizes x in $(-q/2, q/2)$ into code zero, quantizes x in $(q/2, 3q/2)$ into code one and so on, as shown in Fig. 6 (b). The union of all code bands covers the entire reference voltage range. Therefore, one quantizer corresponds to an impulse train.

Fig. 6 (c) shows the second biased impulse train. Next we will discuss how this train is produced. For form I structure, this conversion function is changed due to the additional offset inside ADC. Thus, the x in $(0, q)$ is quantized into code one, x in $(q, 2q)$ is quantized into code two and so on, shown in Fig. 6 (c). Hence, the impulse train in the second channel is shifted by $q/2$, given by $p_2(x) = p_1(x - q/2)$.

For form II structure, since no offset is added to the ADC, the conversion function of the second quantizer is the same as the first one. However, the offset of $\Delta = q/2$ is added to the input signal, leading to the final result of the quantization changed. Different from x in $(-q/2, q/2)$ corresponds to code zero, two quantized results are produced in this code band. With added Δ , x in $(-q/2, 0)$ still has the quantized result of zero. But x in $(0, q/2)$ is quantized into code one. This is because the actual quantized x is $(0 + q/2, q/2 + q/2) = (q/2, q)$ which is corresponding to the result of one. Result of next code band also changes and so on. Fig. 6 (c) shows this result. From the above discussion, form II is analogous to form I essentially. The impulse train of biased quantizer is also a shift of $p_1(x)$, which gives $p_2(x) = p_1(x - q/2)$.

Next, $f_{\hat{x}}(x)$ is sampled by separately, which gives

$$f_{y1}(x) = f_{\hat{x}}(x) \cdot p_1(x), \quad (8)$$

$$f_{y2}(x) = f_{\hat{x}}(x) \cdot p_2(x), \quad (9)$$

Summing the eq. (8) and eq. (9), a new impulse train is generated, written as

$$\begin{aligned} f_{\hat{y}}(x) &= f_{y1}(x) + f_{y2}(x) \\ &= f_{\hat{x}}(x) \cdot [p_1(x) + p_2(x)] \\ &= f_{\hat{x}}(x) \cdot p(x). \end{aligned} \quad (10)$$

where, new impulse train is $p(x) = q \sum_{m=-\infty}^{\infty} \delta(x - m\frac{q}{2})$. This quantization result is analogous to the a $(N+1)$ -bit quantizer, whose LSB is just half of N -bit quantizer.

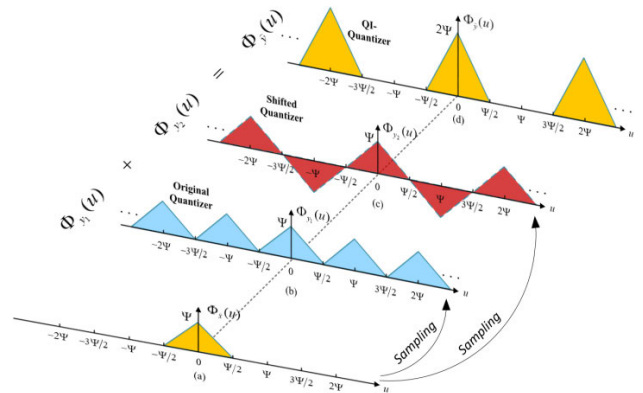


FIGURE 7. Formulation of the QIADC in CF domain (a) CF of input; (b) CF of original quantizer; (c) CF of shifted quantizer, odd spectrums are reversed; (d) Sum of the CF of two quantizers, the height and period of new CF is twice of (b).

In transfer domain, the CF of input can be written as $\Phi_{\hat{x}}(u)$, shown in Fig. 7 (a). After sampling by the impulse train, whose CF $\Phi_p(u)$ is given in eq. (6), the spectrum of $\Phi_{\hat{x}}(u)$ is repeated with period of Ψ . Fig. 7 (b) illustrates the output of original quantizer, represented by $\Phi_{y1}(u)$.

For the shifted quantizer with offset $\Delta = q/2$, the CF of shifted impulse train can learn from the property time shifting of Fourier transform which is given by [31] and written as

$$\begin{aligned} \Phi_{p2}(u) &= e^{-juq/2} \left[\Psi \sum_{k=-\infty}^{\infty} \delta(u - k\Psi) \right] \\ &= \Psi \sum_{k=-\infty}^{\infty} \delta(u - k\Psi) \cdot e^{-juq/2} \Big|_{u=k\Psi} \\ &= e^{-jk\pi} \cdot \Psi \sum_{k=-\infty}^{\infty} \delta(u - k\Psi), \end{aligned} \quad (11)$$

where, the exponential term has value of $e^{-jk\pi} = (-1)^k$. When k is even, $\Phi_{p2}(u)$ is same with original quantizer. Whereas when k is odd, it has a reversal envelope of $\Phi_{p1}(u)$. This yields the CF of $\Phi_{y2}(u)$ part rotation, as shown in Fig. 7(c). In Fig. 7(d), making the summation of original quantizer and shifted quantizer, we get the output of a two channel QIADC, expressed as

$$\begin{aligned} \Phi_{\hat{y}}(u) &= \Phi_{y1}(u) + \Phi_{y2}(u) \\ &= 2\Psi \sum_{l=-\infty}^{\infty} \hat{\Phi}_{\hat{x}}(u - 2k\Psi). \end{aligned} \quad (12)$$

Since $(N+1)$ -bit quantizer has a half LSB of N -bit quantizer, its quantization radian frequency is double of the N -bit quantizer, that gives $\Psi_{N+1} = 2\Psi_N$. Therefore, the output of

a $(N+1)$ -bit quantizer yields

$$\begin{aligned} \Phi_{\hat{y}_{N+1}}(u) &= \Psi_{N+1} \sum_{k=-\infty}^{\infty} \hat{\Phi}_x(u - k\Psi_{N+1}) \\ &= 2\Psi_N \sum_{k=-\infty}^{\infty} \hat{\Phi}_x(u - 2k\Psi_N). \end{aligned} \quad (13)$$

Compare eq. (12) and eq. (13) to conclude that a two channel N -bit QIADC is analogous to $(N + 1)$ -bit ADC.

C. ENHANCEMENT OF RESOLUTION

For a more general situation, we extend it to the case of a fixed number $M > 1$ channels, the essential improvement of resolution is proposed in this part.

1) QUANTIZING THEOREM

✧ To achieve the improvement of QIADC, the CF of x is band-limited, so this requires

$$\Phi_x(u) = 0 \quad \text{for } |u| > \frac{\Psi}{2m} = \frac{\pi}{qm}. \quad (14)$$

✧ The achievable bit of improvement of M channel QIADC is

$$b = \log_2 M. \quad (15)$$

To recover the whole input information from M channel QIADC, the CF should avoid aliasing, which requires a constraint of eq. (14). Besides, to achieve the theoretical enhancement, channel mismatches or non-ideal errors are inevitable. It is required all the errors, such as slight offset, gain, time skew, bandwidth mismatch, and nonlinearity error, have been calibrated and controlled at first. Under these two assumptions, the resolution can be improved as (15).

2) PROOF OF Eq. (15)

The increased performance is independent of the original number of bits but is strongly related to the number of channels.

Let the resolution of original quantizer is N -bit. For the m th channel impulse train. The m th channel impulse train $p_m(x)$ is shifted by o_m in horizon axis compared with the first channel $p_1(x)$. Therefore, we directly obtain the CF of the m th channel impulse train

$$\begin{aligned} \Phi_{p_m}(u) &= e^{-ju(mq/M)} \cdot \left[\Psi_N \cdot \sum_{k=-\infty}^{\infty} \delta(u - k\Psi_N) \right] \\ &= \Psi_N \cdot \sum_{k=-\infty}^{\infty} \delta(u - k\Psi_N) \cdot e^{-ju(mq/M)} \Big|_{u=k\Psi} \\ &= \Psi_N \cdot \sum_{k=-\infty}^{\infty} \delta(u - k\Psi_N) \cdot e^{-jk\Psi_N(mq/M)}, \end{aligned} \quad (16)$$

where, $\Phi_{p_m}(u)$ has a period of Ψ_N . After the linear summation of M channels, the CF of QIADC system output

arrives at

$$\begin{aligned} \Phi_{\hat{y}}(u) &= \Phi_{\hat{x}}(u) \cdot \sum_{m=1}^M \Phi_{p_m}(u) \\ &= \Phi_{\hat{x}}(u) \cdot \sum_{m=1}^M \left[\Psi_N \sum_{k=-\infty}^{\infty} \delta(u - k\Psi_N) \cdot e^{-jk\Psi_N(mq/M)} \right] \\ &= \Phi_{\hat{x}}(u) \cdot \sum_{k=-\infty}^{\infty} \alpha(k) \cdot \delta(u - k\Psi_N), \end{aligned} \quad (17)$$

where, the internal sum is $\alpha(k) = \Psi_N \sum_{m=1}^M e^{-jk\Psi_N(mq/M)}$. Notice that $\alpha(k)$ in eq. (10) can be computed as follows:

$$\begin{aligned} \alpha(k) &= \Psi_N \sum_{m=1}^M e^{-jk(2\pi/q) \cdot (mq/M)} \\ &= \Psi_N \sum_{m=1}^M e^{-jm2\pi k/M} \\ &= \begin{cases} M \cdot \Psi_N, & k = lM \\ 0, & k \neq lM. \end{cases} \end{aligned} \quad (18)$$

The basis for this result is the fact that the summation over one period of a periodic complex exponential is zero. However, when $k = lM$, where $l \in Z$, complex exponential has a real value. Substituting the eq. (18) to eq. (17), the final output can be further derived by

$$\Phi_{\hat{y}}(u) = \Phi_{\hat{x}}(u) \cdot M\Psi_N \sum_{l=-\infty}^{\infty} \delta(u - lM\Psi_N). \quad (19)$$

On the other hand, $(N + b)$ -bit quantizer has a period of quantization frequency $\Psi_{N+b} = 2^b\Psi_N$, which means M channel QIADC system is analogous to the $(N + b)$ -bit ADC. So the eq. (15) is proven. ■

D. ENOB ANALYSIS

Besides the enhancement of real bit, i.e., ADC resolution, the ENOB is also improved in QIADC. ENOB is a key metric of evaluating the application performance. According to the definition in IEEE Std 1241 [33], this indicator is defined by equation $ENOB = N - \log_2(\sigma/q_{rms})$, where σ and q_{rms} is respectively the root-mean-square (rms) of all uncorrelated noise and quantization noise. There are kinds of factors to influence σ , such as temperature, circuit quality, frequency of the input, etc.. An important feature is as σ increases, ENOB will reduce. Averaging is an effective method to reduce uncorrelated noise which causes the significantly improvement of ENOB. When using averaging technique, the gain of bit can be written by

$$G_{ENOB} = \log_2(\sigma'/\sigma). \quad (20)$$

where σ' is the noise rms of output data.

Since that the standard deviation of the sum of M statistically independent random variables only increases by

\sqrt{M} for averaging method. Therefore, the gain of ENOB is $G_{ENOB} = 1/2 \cdot \log_2 M$ after averaging operation. However, the improvement of averaging only works when quantization noise is lower than thermal noise, which means that, G_{ENOB} is limited by level of uncorrelated noise. This can be explained by a simulation in Fig.8. In this simulation, the standard deviation of thermal noise gradually increases from 0, and the step size is 0.1LSB. Through the ENOBs comparisons of single ADC, 2 channel TSADC and 2 channel QIADC, the relationship between noise and ENOB are depicted in this figure. TSADC is a typical parallel averaging method.

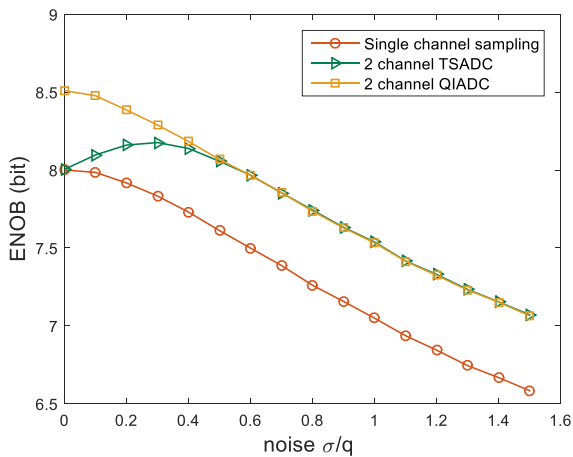


FIGURE 8. An comparison ENOB v.s. level of uncorrelated noise. The ENOBs are calculated from a same signal that is respectively sampled by single ADC, 2 channel TSADC and 2 channel QIADC.

Obviously, for ideal condition of $\sigma/q = 0$, TSADC has no contribution to ENOB. When $\sigma/q > 0.5$, the gain of TSADC is 0.5 bit. The simulation results are consistent with the theoretical value $G_{ENOB|M=2} = 0.5$ bit. This shows the premise of TSADC is nearly 0.5 times of LSB. However, the excess bits of QIADC is not limited by noise level. As σ increases from ideal condition to normal condition, the improvement stays 0.5 bit. Though for a good ADC with extreme low thermal noise, the improvement of 0.5 bit is also obtained for a dual channel QIADC. This simulation concludes that QI sampling has the same ENOB improvement of averaging when σ is large. Besides, the boost is not constrained by noise level.

IV. APPLICATION OF QUANTIZATION INTERLEAVING

The proposed architecture has been implemented in an oscilloscope with one acquisition channel, which has sampling rate of 5GSPS and resolution of 11-bit. The 11-bit resolution is achieved through dual channel QIADC structure. If the prototype is not configured in QIADC manner, the input signal is sampled by a single ADC. Each ADC has 5GSPS sampling rate and 10-bit resolution.

The core circuit diagram is illustrated in Fig. 9. From the signal generator, the input signal passes through three circuit boards. 1) The first is conditioning board, composed of low-pass (LP) filter, single-ended to differential circuit and a power splitting network, which is designed for voltage

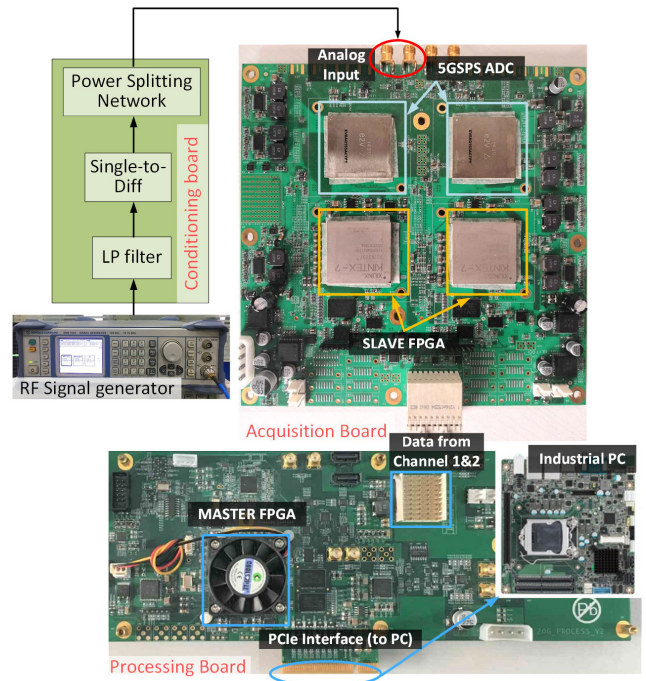


FIGURE 9. An implementation diagram of dual channel QIADC structure, including a conditioning board, an acquisition board, and a processing board.

adjustment to adapt ADC. 2) Next is acquisition board, which includes two ADCs and two SLAVE field programmable gate arrays (FPGAs). This board is used for basic signal digitization, acquisition in different mode and hardware decimation. Selected FPGA (XC7K325T, Xilinx, Inc., Kintex-7 series) receives the parallel data streams from the two ADCs that meet the specific protocol and control data acquisition process. The ADC configuration is done by software before normal operation. 3) The last is processing board which is consists of a synthetical FPGA (XC7K325T, Xilinx, Inc., Kintex-7 series) and a configurable clock generator. High-quality sampling clock signal is generated in this module and frequency conversion is finished through phase-locked loop. This FPGA reconstructs the high speed data and stores the sampled data in the first-in first-out (FIFO) buffer (Normal acquisition mode) or the third-generation double data rate (DDR3) memory (Mass storage acquisition mode). Finally, the sampled data are sent to industrial PC for display and advanced analysis through peripheral component interface express (PCI-e) interface.

The proposed QI technology runs through the entire system. As aforementioned analysis, form II is analogous to form I essentially. In this design, in order to adapt to this platform, the front-end is implemented in type I manner. Operation of adding offset is done by configuring the offset control register inside ADC. Then, the implementation of summation process lands in the MASTER FPGA.

The selected ADC (EV10AQ190A, E2V, Inc., Quadruple series) has an offset register to compensate for the offset bias, which can be regarded as the interface of internal

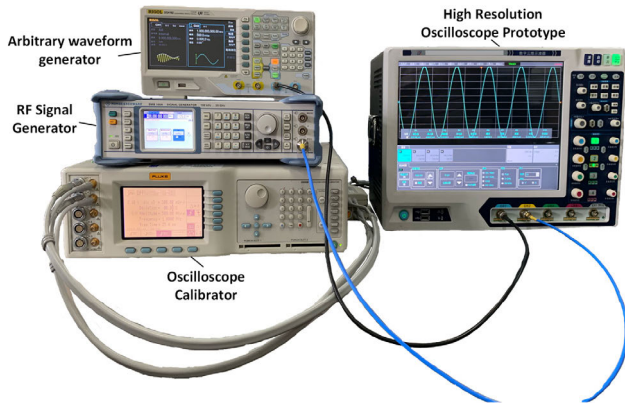


FIGURE 10. The test platform of prototype evaluation.

offset adjustment. According to the datasheet of ADC [32], we find the variation offset range is $\sim \pm 20\text{LSB}$ and the total configuration step size is 1024. So, the digital control word (DCW) can be calculated by the following equation

$$o_m = o_0 - \frac{m}{M} \cdot \frac{1024}{40}. \quad (21)$$

Therefore, the update value of two offset registers to be sent are calculated, illustrated in Table. 1.

TABLE 1. The update DCW of offset registers, $M = 2$.

| Channel | Relative | Decimal | DCW value |
|---------|----------|---------|-------------------------|
| 0 | 0 | 512 | 0x200 (Default Setting) |
| 1 | 13 | 499 | 0x1F3 |

V. EVALUATION

In this section, we evaluate QIADC from the aspects of static test without signal, dynamic test in terms of ENOB analysis and arbitrary waveform. First, the smallest signal that can be recognized is significantly improved. Second, the standard ENOB evaluation of acquisition system has been carried out, which demonstrates the effectiveness of improvement of dynamic parameters. Finally, we show that our method delivers more accuracy in real signals capture. These experiments are based on the self-organizing test platform.

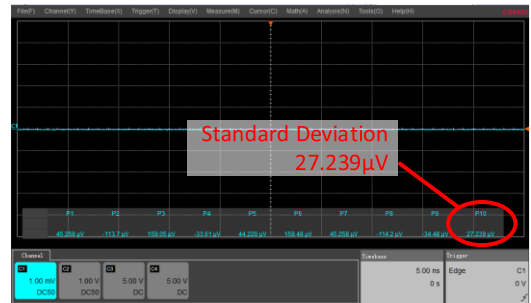
A. EXPERIMENT SETUP

The experiment is based on the test platform which includes the oscilloscope prototype, oscilloscope calibrator, signal generator and arbitrary waveform generator (AWG) shown in Fig. 10. The instrument that is under test is the designed high resolution oscilloscope prototype. Software developed on visual studio 2017 runs on Windows 7 operating system, which supports the configuration operated through the panel or peripherals flexibly. The prototype will be first calibrated by the oscilloscope calibrator (FLUKE, 9500B) automatically and accurately. The input signals of experiment are provided by two types of signal generator. One is RF signal generator (Rohde & Schwarz, SMB 100A) which supplies

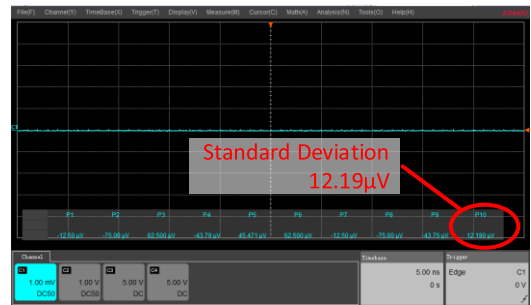
high frequency sinusoidal signals from 100kHz to 20GHz to the prototype. The other instrument on the top of SMB 100A is arbitrary waveform generator (RIGOL, DG4162). It generates many kinds of complicated signals for the time-domain waveform test.

B. BASELINES

In the first experiment, we tested the standard deviation of baseline noise, denote as σ , without any input signal. This is an effective evaluation of the small signal which reflects the static performance of an oscilloscope.



(a)



(b)

FIGURE 11. Baseline test without any input signal. (a) The top plot shows the baseline without QI technique. (b) The bottom plot shows the waveform after employing QI technique with $M = 2$. The marker shows the standard deviation of baseline noise.

Fig. 11 visually shows the baseline noise @ 1mV/div. In the measurement table on the screen, the column of ‘P10’ gives the result of σ , which is calculated by N samples

$$\sigma^2 = mse = \frac{1}{N} \sum_{n=1}^N (y_n - \bar{y})^2, \quad (22)$$

where, \bar{y} is the mean of total samples. From Table 2, it shows that the σ of 12.19 μV and 27.24 μV with and without QIADC in the two figures of Fig. 11 (a)&(b). Table 2 records the measured standard deviation of baseline noise at different vertical scales. From the small signal range @ 1mV/div to large signal range @ 1V/div, the test is carried with the sampling rate of 5GSPS. By comparing Table 2, the minimum value and typical value of σ decreases after applying QIADC method. This indicates that the smaller signal can be recognized in the system. From the table, it shows that the smallest signal is defined in the prototype with rms of 11.03 μV .

TABLE 2. Measured baseline noise @5GSPS.

| Vertical scale | Tradition | | QI sampling | |
|----------------|---------------|---------------|---------------|---------------|
| | Min. | Typ. | Min. | Typ. |
| 1mV/div | 21.4 μ V | 27.24 μ V | 11.03 μ V | 12.19 μ V |
| 10mV/div | 220.5 μ V | 247.5 μ V | 124.5 μ V | 131 μ V |
| 100mV/div | 2.19 mV | 2.34 mV | 1.21 mV | 1.30 mV |
| 1V/div | 21.68 mV | 23.91 mV | 12.19 mV | 13.51 mV |

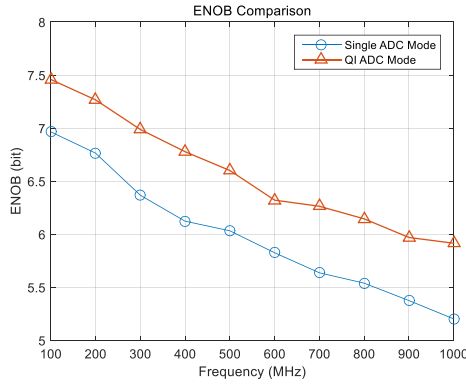


FIGURE 12. ENOB curves in different acquisition modes. The input frequency has an input range from 100MHz to 1GHz.

The result of this experiment demonstrates an improvement in terms of static noise performance. This mostly contributes to the reduction of quantization noise of QIADC. Besides, since the noise from two channels are independent, σ of uncorrelated noise is also reduced after the summation of sampled data. In addition, this result also contributes to the system dynamic range. With the same largest signal, the dynamic range of system improves

$$20 \cdot \lg \left(\frac{21.4\mu\text{V}}{11.03\mu\text{V}} \right) = 5.7568 \text{ dB.} \quad (23)$$

C. DYNAMIC PERFORMANCE

Next, the dynamic performance of system is verified by testing the ENOB at different frequencies. First, the SMB100A generates a set of sinusoidal waves from 100MHz to 1GHz as analog input with frequency interval of one hundred megahertz. Then, the digitized output data is sent to the industrial PC for ENOB analysis. The ENOB can be calculated in frequency domain by SINAD test method proposed in IEEE Std 1241 [33]. After the calculation of SINAD, the value is transferred to ENOB by the relationship of (71) in [33]. Repeat this calculation process and plot a curve of ENOB as a function of frequency, shown in Fig. 12.

From the horizontal point of view, it can be seen that ENOB decreases when frequency increases. The main reason for the drop is that even if the original signal amplitude is same, the jitter noise power on the sampling clock increases as the frequency increases. Distortions and nonlinearity spurs are also positively correlated with frequency of input. By the vertical comparison, it can be seen that the best ENOB performance that appears in QIADC mode is 7.5-bit@100MHz,

which is 0.5-bit higher than traditional single channel mode. And this enhancement keeps same in the whole 1GHz band.

Through this experiment, it can be concluded that compared with the traditional sampling method, the real performance is significantly improved in the system with QI method. But the result also shows that this method has little contribution to jitter noise cancellation, which is a typical source of correlated noise.

D. WAVEFORM

The third experiment depicts the time domain waveform. In this experiment, we chose typical square and sinc signal that generated from AWG as test signals. Fig. 13 illustrates the different views of captured waveform with and without QI technique. For better observation, the signal is partially amplified in the zoomed window.

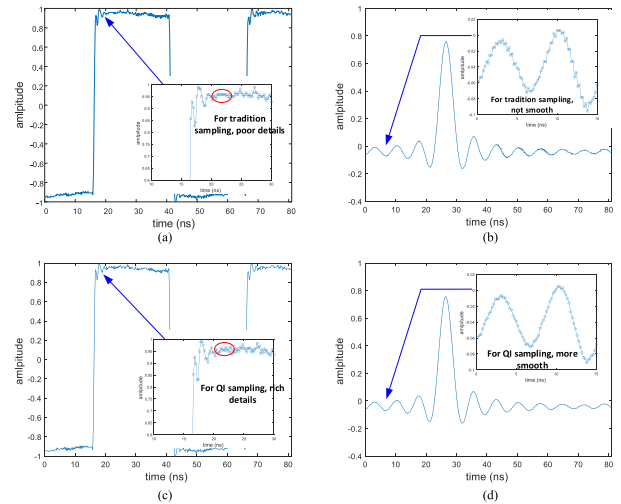


FIGURE 13. Time-domain waveforms of by (a) 20MHz square signal captured without QI technique; (b) 10M sinc signal captured without QI technique; (c) 20MHz square signal captured with QI technique; (d) 10M sinc signal captured with QI technique. The partially enlarged view of the waveform is displayed in the embedded window in the figure.

Fig. 13 (a) illustrates the square waveform captured by tradition sampling method. It can be seen that for slow-changing parts, the details of ripple are poor. The focus part of flat signal shows that waveform changes cannot be recognized due to insufficient resolution. However, from Fig. 13(c), when applying QI sampling technique, the ripple can be observed clearly and the details of ripple are rich. The result reflects the nature of high resolution that is a more accurate description of waveform.

Fig. 13 (b)&(d) show the view of sinc signal and its tail acquired with tradition method and QI method. In the zoom view, it can be found that instead of the saw tooth on the signal captured by tradition method, the waveform is more smooth when sampled by the QI technique, shown in Fig. 13 (d). From this experiment, it can be concluded that except for the advantage of high definition, the QI sampling also contributes to waveform smoothing and noise cancellation.

E. CONSUMPTION ANALYSIS

Previous results show good behavior in terms of small signal, ENOB and waveform. However, the improvement comes at the cost of extra resource requirements.

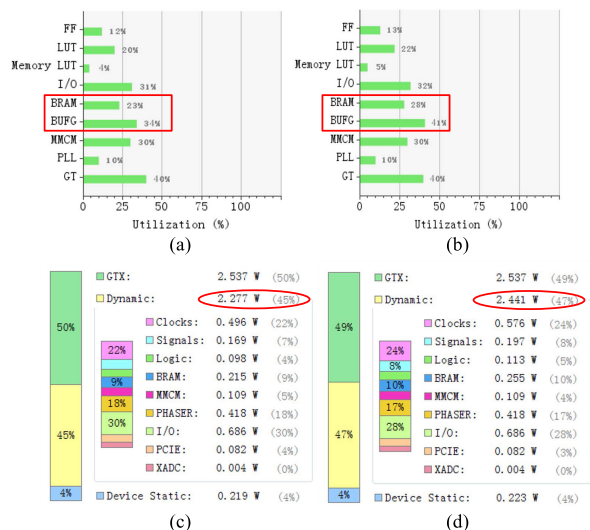


FIGURE 14. Utilization of Logic resources and power consumption comparison (a) Utilization without QI technique (b) Utilization with dual QI technique (c) On-chip power without QI technique (d) On-chip power with dual QI technique.

The parallel architecture first requires one more ADC. This causes an increase in the cost of the basic device, which also results in twice power and area of the circuit. In addition, Fig. 14 shows the utilization of on chip resources and the power consumption of MASTER FPGA. The percentage result shows that more BRAM and BUFG resources are used since the parallel ADC method requires the processing chip to transfer and cache high-speed data from two ADC channels instead of single channel. Besides, due to more D flip-flops are used, dynamic power increases from 2.277W to 2.441W. Increased power consumption only accounts for 6% of total power consumption but the improvement of baseline noise and ENOB presented in experiment B&C is significantly higher than a single channel. Although the consumption increases, from this figure, it shows great efficiency in terms of logic resources and its power.

VI. CONCLUSION

We have proposed a parallel acquisition architecture to improve vertical resolution for the ultra-fast applications. Through interleaved sampling in vertical axis, we obtain more bits of resolution in the acquisition system.

In this work, we first introduced the quantization theory from a statistical perspective to build the foundation theory of QIADC. Besides, a precise analysis of improvement was proposed and proven by a statistical quantization-sampling model for the first time. Next, we have designed a high resolution oscilloscope prototype based on dual channel QI structure. Experiments are carried to demonstrate the real

effectiveness of QIADC from three aspects of baseline test, dynamic test and arbitrary waveform test. Compared with traditional methods, the experimental results have shown higher dynamic range and ENOB with QIADC technique. Except for applied to the instrument integrated with acquisition system, the proposed technique also provides a new angle in high resolution integrated circuit design.

REFERENCES

- [1] A. Albert, S. Funk, H. Katagiri, T. Kawashima, M. Murphy, A. Okumura, R. Quaglian, L. Sapozhnikov, A. Shigenak, H. Tajima, L. Tibaldo, J. Vandembroucke, G. Varner, and T. Wuh, "TARGET 5: A new multi-channel digitizer with triggering capabilities for gamma-ray atmospheric Cherenkov telescopes," *Astroparticle Phys.*, vol. 92, pp. 49–61, Jun. 2017.
- [2] B. Brannon, "Some recent developments in the art of receiver technology: A selected history on receiver innovations over the last 100 years," *Analog Dialogue*, vol. 52, pp. 1–6, Aug. 2018.
- [3] Z. M. Parker, T. J. Pasielka, G. A. Parker, and D. A. Leib, "Immune- and nonimmune-compartment-specific interferon responses are critical determinants of herpes simplex virus-induced generalized infections and acute liver failure," *J. Virol.*, vol. 90, no. 23, pp. 10789–10799, 2016.
- [4] J. N. Rogers, C. E. Parrish, L. G. Ward, and D. M. Burdick, "Improving salt marsh digital elevation model accuracy with full-waveform lidar and non-parametric predictive modeling," *Estuarine Coastal Shelf Sci.*, vol. 202, pp. 193–211, Mar. 2018.
- [5] E. C. Pollacco, G. F. Grinyer, F. Abu-Nimeh, T. Ahn, S. Anvar, and A. Arokiaraj, "GET: A generic electronics system for TPCs and nuclear physics instrumentation," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 887, pp. 81–93, Apr. 2018.
- [6] *DEBUG in HIGH DEFINITION: HDO9000 Oscilloscope Datasheet*, Teledynelecroy, Chestnut Ridge, NY, USA, 2017.
- [7] P. J. Pupalaiakis and T. Lecroy, "Understanding vertical resolution in oscilloscopes," DesignCon, Santa Clara, CA, USA, Tech. Rep., 2017. [Online]. Available: https://www.researchgate.net/publication/313384271_DesignCon_2017_Understanding_Vertical_Resolution_in_Oscilloscopes
- [8] J. C. Candy and O. J. Benjamin, "The structure of quantization noise from sigma-delta modulation," *IEEE Trans. Commun.*, vol. COM-29, no. 9, pp. 1316–1323, Sep. 1981.
- [9] H. Inose, Y. Yasuda, and J. Murakami, "A telemetry system by code modulation- $\Delta - \Sigma$ modulation," *IRE Trans. Space Electron. Telemetry*, vol. SET-8, no. 3, pp. 204–209, Sep. 1962.
- [10] C. Bishop, "Effects of averaging to reject unwanted signals in digital sampling oscilloscopes," in *Proc. IEEE AUTOTESTCON*, Sep. 2010, pp. 1–4.
- [11] Y. Lembeje, J. P. Keradec, and G. Cauffet, "Improvement in the linearity of fast digital oscilloscopes used in averaging mode," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 6, pp. 922–928, Dec. 1994.
- [12] C. Fager and K. Andersson, "Improvement of oscilloscope based RF measurements by statistical averaging techniques," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, Jun. 2006, pp. 1460–1463.
- [13] A. Baccigalupi, M. D'Arco, A. Liccardo, and R. S. L. Moriello, "Compressive sampling-based strategy for enhancing ADCs resolution," *Measurement*, vol. 56, pp. 95–103, Oct. 2014.
- [14] L. Angrisani, M. D'Arco, G. Ianniello, and M. Vadursi, "An efficient pre-processing scheme to enhance resolution in band-pass signals acquisition," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 11, pp. 2932–2940, Nov. 2012.
- [15] L. Angrisani, M. D'Arco, G. Ianniello, and M. Vadursi, "Novel built-in solution for data acquisition system resolution enhancement," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf.*, May 2011, pp. 1–5.
- [16] K. Yang, S. Tian, P. Ye, P. Zhang, and Y. Zheng, "A statistic-based calibration method for TIADC system," *Math. Problems Eng.*, vol. 2015, no. 6, 2015, Art. no. 689869.
- [17] L. D. Han, D. M. Nguyen, C. Jabbour, T. Graba, P. Desgreys, and O. Jamin, "All-digital calibration of timing skew for TIADCs using the polyphase decomposition," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, pp. 99–103, Jan. 2016.
- [18] K. Yang, J. Shi, S. Tian, W. Huang, and P. Ye, "Timing skew calibration method for TIADC-based 20 GSPS digital storage oscilloscope," *J. Circuits Syst. Comput.*, vol. 25, no. 2, 2016, Art. no. 1650007.
- [19] Y. Qiu, Y.-J. Liu, J. Zhou, G. Zhang, D. Chen, and N. Du, "All-digital blind background calibration technique for any channel time-interleaved ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2503–2514, Aug. 2018.

- [20] J. Gao, P. Ye, H. Zeng, J. Song, W. Wei, and K. Yang, "An adaptive calibration technique of timing skew mismatch in time-interleaved analog-to-digital converters," *Rev. Sci. Instrum.*, vol. 90, no. 2, 2019, Art. no. 025102.
- [21] P. Pupalaiakis, "High bandwidth real time oscilloscope," U.S. Patent 7 519 513 B2, Apr. 14, 2009.
- [22] P. Pupalaiakis and D. C. Graef, "High bandwidth oscilloscope for digitizing an analog signal having a bandwidth greater than the bandwidth of digitizing components of the oscilloscope," U.S. Patent 8 583 390 B2, Nov. 12, 2013.
- [23] D. Knierim and Beaverton, "Test and measurement instrument including asynchronous time-interleaved digitizer using harmonic mixing," EP Patent 2 528 235 A2, Nov. 28, 2012.
- [24] J. Song, S. Tian, and Y.-H. Hu, "Analysis and correction of combined channel mismatch effects in frequency-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 655–668, Feb. 2019.
- [25] E. Seifert and A. Nauda, "Enhancing the dynamic range of analog-to-digital converters by reducing excess noise," in *Proc. IEEE Pacific Rim Conf. Commun., Comput. Signal Process.*, Jun. 1989, pp. 574–576.
- [26] K. C. Lauritzen, S. H. Talisa, and M. Peckerar, "Impact of decorrelation techniques on sampling noise in radio-frequency applications," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 9, pp. 2272–2279, Sep. 2010.
- [27] J. Gao, W. Huang, W. Wei, L. Guo, H. Li, and P. Ye, "Trade-off between sampling rate and resolution: A time-synchronized based multi-resolution structure for ultra-fast acquisition," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2018, pp. 1–5.
- [28] G. Ulbricht, J. Kneißl, C. Kelm, and G. Kilian, "Increasing SDR receiver dynamic range by ADC diversity," *J. Signal Process. Syst.*, vol. 89, no. 1, pp. 191–208, 2017.
- [29] W. Huang, J. Gao, P. Ye, K. Yang, L. Guo, W. Wei, Y. Zhao, Z. Pan, S. Tian, and H. Wang, "General analysis of resolution enhancement on time-synchronized sampling and its multi-resolution solution in 20GSPS acquisition system," *IEEE Access*, vol. 7, pp. 81321–81332, 2019.
- [30] B. Widrow, I. Kollar, and M.-C. Liu, "Statistical theory of quantization," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 2, pp. 353–361, Apr. 1996.
- [31] A. V. Oppenheim and A. S. Willsky, *Signal and System*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.
- [32] *Low Power QUAD 10-Bit 1.25 GSPS ADC Operating Up to 5 GSPS Quadruple Analog to Digital Converter: EV10AQ190A Datasheet*, E2V, Chelmsford, U.K., 2013.
- [33] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converter*, IEEE Standard 1241, IEEE Instrumentation Measurement Society, 2010.



JIAN GAO was born in Hebei, China, in 1993. He received the bachelor's degree from the University of Electronic Science and Technology (UESTC), Chengdu, China, in 2015, where he is currently pursuing the Ph.D. degree. His research interests include mixed-signal processing, filter design, optimization control, high-speed ADCs, digital storage oscilloscopes, and so on.



PENG YE was born in Sichuan, China, in 1973. He received the B.S., M.S., and Ph.D. degrees from the University of Electronic Science and Technology of China (UESTC), in 1995, 2001, and 2010, respectively, where he is currently a Professor. His research interests include high speed data acquisition and signal processing, and digital storage oscilloscope.



HAO ZENG was born in Sichuan, China, in 1979. He received the B.S., M.S., and Ph.D. degrees from the University of Electronic Science and Technology of China (UESTC), China, in 2002, 2005, and 2010, respectively. He is currently a Researcher with UESTC. His research interests include high speed data acquisition and signal processing, RF signal generator, and so on.



ZHIXIANG PAN was born in Anhui, China, in 1993. He received the B.S. degree in measurement technology and instruments from the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2015, where he is currently pursuing the Ph.D. degree. His research interests include the design and theory of wideband signal acquisition and processing, and electronic measurement and instrument.



YU ZHAO was born in Liaoning, China, in 1993. He received the B.S. degree in electric and information engineering from the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, China, in 2015, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include the design and theory of digital, analog, and mixed-signal processing systems, and high speed data acquisition systems.



HAO LI received the B.S. degree from the North University of China. He is currently pursuing the Ph.D. degree with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, China. He has been visiting the Wireless Communication Group, University of British Columbia, Kelowna, BC, Canada, since 2017, sponsored by the China Scholarship Council. His current research interests include 5G cellular networks, resource allocation optimization, massive MIMO, and heterogeneous networks.



JIE MENG was born in Inner Mongolia, in 1992. She received the B.S. degree from the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), in 2015, where she is currently pursuing the Ph.D. degree. Her research interests include wideband signal communication systems, digital signal processing, and high-speed signal acquisition.

...