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Selecting the Optimal Resolution and Conversion Frequency for A/D and D/A Converters

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Abstract *–When a signal is converted by means of a converter circuit as an analog to digital converter (ADC) or a digital to analog converter (DAC) the quantization and sampling effects appeared, which causes a quality decrease of the signal that is usually indicated by the signal to noise ratio (SNR). This SNR lost decreases when the resolution and conversion frequency of the converter is increased. Nevertheless, in this way the cost and the complexity of the circuit are also unnecessarily increased. In this work, a method to select the optimal resolution and the conversion frequency is proposed. This method, which is based on the dynamic characteristic of the converter and the signal, utilizes the desirable resulting signal quality as the constraint. From the signal's SNR and the quantity of it that can be lost the minimum number of bits N is obtained. Then, from N the minimum conversion frequency is calculated. A mathematical analysis and a simulation test of the method are carried out. Results can be directly applied to select the main dynamics characteristics of the ADC, the DAC or, in general, of a DAS.*

Keywords *–Data acquisition, data conversion, digital-analog conversion, signal sampling, signal resolution, white noise, random noise.*

I. INTRODUCTION

When an ADC (Analog to Digital Converter) [1]-[3] or a DAC (Digital to Analog Converter) has to be selected, or even a DAS (Data Acquisition System) [4] [5], the question of how many bits are necessary and how fast the signal must be sampled for the application in question is formulated.

As a first approach, the number of bits needed may be specified taking into account the minimal variation of the input signal to be detected, which is called one code bin or Q. This coefficient is calculated by dividing the Full Scale input Range (FSR) by the number of code transition levels in the discrete transfer function (2^N-1) [6] [7]. This is the most common method used but it is only suitable from a static point of view. Therefore, it is not enough when the lost signal quality must be known; this is the dynamic point of view.

On the one hand, the characteristic defining the signal quality from a dynamic point of view is its SNR. On the other hand the conversion process, sampling and quantization, has two negative effects over the signal's SNR. The sampling effect depends on the frequency f_S and the quantization effect depends on the resolution or the number of bits N.

Therefore the SNR decreases depending on the f_S y N. To aid their selection it is necessary to relate them by means of a rule or an equation which are easy to apply. That is to say what is the SNR of the signal and what its tolerated loss is? Thus, firstly the initial signal's SNR and its quantity sacrificed are related to the minimum N. Secondly the value obtained of N is utilized to calculate the minimum value of f_S. In this way, the dimension and the working frequency of the converter are optimized.

On study this relation it has been found that when the ADC resolution N increased, the SNR of the signal also improved, but only up to a certain N, above which point no more improvement is achieved. Therefore, it is pointless to select an ADC with a better resolution. As for the conversion frequency, it is deduced that to optimize the value of N to obtain a certain signal quality, it is necessary to use a criteria in order to establish a minimum conversion frequency. Therefore the introduced criteria must be taken into account, which is stronger than the Nyquist criteria [7] but guarantees that with no periodic signals the same desirable quality may be achieved. From that analysis, considering that this signal always has some quality loss, albeit it small (for instance 0.1 dB), two equations are obtained.

To validate the previous analysis, using a random noise model, uniformly distributed for the signal and also for the ADC model, simulations have been made.

These results can be directly applied as a criterion to select the dynamic characteristic of an ADC, a DAC or a DAS. Moreover, it can be useful to answer another question. That is, if the SNR of an analog signal is unknown and it is converter to digital format, could that SNR be deduced? Well, if the original characteristic of the signal is known, if the ADC SNR is also known and if the SNR of the converted signal is calculated, then, the SNR of the original signal may be deduced.

In the next section a detailed problem definition and its solution is presented. In section III a simulation example is presented and in section IV experimental results, which utilize a real DAS including an ADC with its conditioning circuit and the interface with the PC, are shown in order to prove the main contributions of this work. Finally, conclusions are summarized in section V.

II. PROPOSED SOLUTION

The problem definition follows the Fig. 1 diagram. The starting data is the SNR of the signal and the maximum accepted SNR loss. From this data the minimum number of bits is obtained. Finally, with this value and with the input signal frequency, the minimum conversion frequency is obtained.

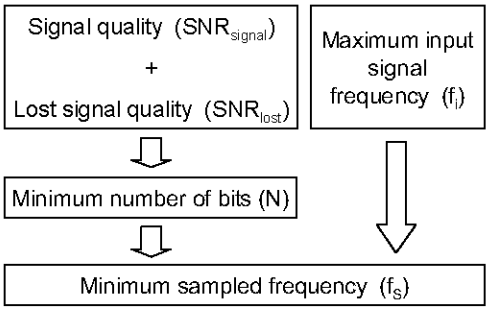

Fig. 1. Input and output information for the problem.

A. Problem analysis

To analyze the problem the diagram depicted in Fig. 2 is followed. The diagram consists of two blocks, B_1 and B_2, which are characterized by their SNR and are connected in serial.

B_1 constitutes the source of the original signal S_1 that is composed by the x information and by the r_1 noise, so the output signal of the B_1 is $S_1=x+r_1$. This signal crosses B_2 and becomes noisier since this block introduces it the r_2 noise. To do the analysis the two following suppositions are made. First, signal information x is maintained through the two blocks. Second, noises r_1 and r_2 are considered as independent random variables. Then, the total noise in the signal at the B_2 block output is equal to the quadrature sum of the two noises $(r_1^2+r_2^2)^{1/2}$ [8] and the output information is x. With these suppositions the final signal is $S=x+(r_1^2+r_2^2)^{1/2}$.

To distinguish how the signal to noise ratio is expressed, if it is in a logarithmic scale (dB) the capital letters are used (SNR) and if it is per unit the lower case letters are used (snr).

Then, the snr of B1 is $snr_1=x/r_1$ and for B2 is given by $snr_2=x/r_2$. When this relation is expressed in a logarithmic scale we have the equations $SNR_1=20\log(x/r_1)$ and $SNR_2=20\log(x/r_2)$ both of them expressed in (dB).

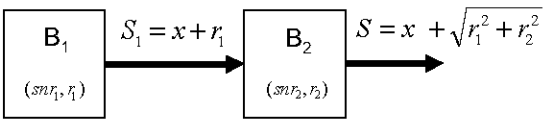

Fig. 2. Diagram of the signal source (B_1) and the process (B_2) handling the signal.

The total signal to noise ratio is given by (1), and taking into account the noise of each block given by (2), the total signal to noise ratio, depending on the signal to noise ratio of each two blocks, is obtained from (3). This equation may be generalized to more blocks by means of (4). Commonly, the signal to noise ratio is expressed in a logarithmic scale according to expression (5) and the acronym SNR is used. In this way, the total SNR of the two blocks is represented by (6). This equation is specified, by the following example depicted in Fig. 1, by (7).

$$snr = \frac{x}{\sqrt{r_1^2 + r_2^2}} \tag{1}$$

$$r_1 = \frac{x}{snr_1} \;;\; r_2 = \frac{x}{snr_2} \tag{2}$$

$$snr = \frac{x}{\sqrt{\frac{x^2}{snr_1^2} + \frac{x^2}{snr_2^2}}} = \frac{snr_1 \cdot snr_2}{\sqrt{snr_1^2 + snr_2^2}} \tag{3}$$

$$snr = \frac{\prod_{m=1}^{2} snr_m}{\sqrt{\sum_{m=1}^{2} snr_m^2}} \tag{4}$$

$$SNR = 20 \cdot \log snr \quad ; \quad snr = 10^{\frac{SNR}{20}} \tag{5}$$

$$SNR = 20 \cdot \log \frac{\prod_{m=1}^{2} 10^{\frac{SNR_m}{20}}}{\sqrt{\sum_{m=1}^{2} 10^{\frac{SNR_m}{20} \cdot 2}}} \tag{6}$$

$$SNR = 20 \cdot \log \frac{10^{\sum_{m=1}^{2} \frac{SNR_m}{20}}}{\sqrt{\sum_{m=1}^{2} 10^{\frac{SNR_m}{10}}}} = 20 \cdot \log \frac{10^{\frac{SNR_1 + SNR_2}{20}}}{\sqrt{10^{\frac{SNR_1}{10}} + 10^{\frac{SNR_2}{10}}}} \tag{7}$$

B. Application to the ADC number of bits selection

The previous analysis may be directly applied to the problem of calculating the minimum number of bits needed to limit the maximum loss in the signal quality. The block B_1 is substituted by a generator representing the process that provides the signal to be converted and B_2 is changed by the ADC (Fig. 3). To simplify, the terminology of Table I is followed.

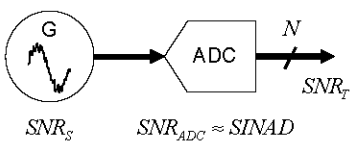

Fig. 3. Diagram of the two blocks connected in serial.

Table I. Terminology.

Term	Definition
N	Number of bits
snr_S	Input signal SNR
snr_{ADC}	ADC SNR
snr_L	SNR lost of the signal
snr_T	Total SNR in the output
SNR_S	Input signal SNR in dB
SNR_{ADC}	ADC SNR in dB
SNR_L	SNR lost of the signal
SNR_T	Total SNR in the output in dB

By substituting in (7) the terms defined in Table I the expression of the total SNR is obtained (8). In this equation the value of the SNR_{ADC} may be substituted by (9). In this way, the SNR_T depending on the SNR_S and N is obtained (10).

$$SNR_T = 20 \cdot \log \frac{10^{\frac{SNR_S + SNR_{ADC}}{20}}}{\sqrt{10^{\frac{SNR_S}{10}} + 10^{\frac{SNR_{ADC}}{10}}}} \quad (8)$$

$$SNR_{ADC} = 6.02 \cdot N + 1.76 \quad (9)$$

$$SNR_T = 20 \cdot \log \frac{10^{\frac{SNR_S + 6.02 \cdot N + 1.76}{20}}}{\sqrt{10^{\frac{SNR_S}{10}} + 10^{\frac{6.02 \cdot N + 1.76}{10}}}} \quad (10)$$

According to (10) Fig. 4 shows how the quality of the sampled signal (indicated by SNR_S) improves when the number of bits (N) of the ADC increases. In this example, the input signal has an SNR (SNR_S) equal to 50 dB. The total SNR (SNR_T) increases significantly up to certain N (around 9-10 bits). After this, even if N is increased, the total SNR does not improve. This performance is important because it may be taken as a rule. Since, ***if an ADC with a SNR with 10 dB above the SNR of the signal is selected, then the signal is minimally worsened*** (about 0.1 dB). Therefore, if an ADC with more bits of resolution is selected, it will be more expensive but the performance achieved will not be better. Moreover, if more bits than those needed are used, not only the cost of the ADC is greater but also the cost of digital parts (the bus width, the memory size, etc.), the power consumption and the conversion time are unnecessarily increased.

From this point of view, it is possible to know what is the SNR of the ADC needed and then to deduce from it the number of bits. But, if what is interesting is to be able to select N from the acceptable loss in the SNR, it will be necessary to adapt the previously presented calculus as follows.

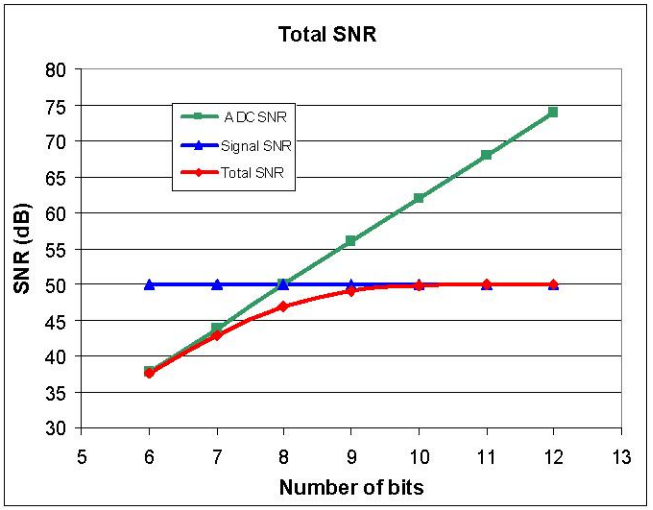

Fig. 4. Total SNR versus the ADC number of bits (N).

The starting point is the loss acceptable in the SNRof the signal. This loss in the SNR is, according to (11), the difference between the signal SNR and the total SNR in the output. By substituting the SNR values (12) and transforming it to a linear scale the equation (13) is obtained. In this equation the value of snr_T is substituted by its value from the general expression obtained in (4). Thus, the value of snr_{ADC} is obtained from (9) and equalized to the expression (14) and then, the expression (15) is achieved. Finally, from (15), N is deduced and with some calculus the general expression for N, which depends on the SNR_S and the value of SNR_L, is obtained.

$$SNR_T = SNR_S - SNR_L \quad (11)$$

$$20 \cdot \log snr_T = 20 \cdot \log snr_S - 20 \cdot \log snr_L \quad (12)$$

$$\log snr_T = \log \frac{snr_S}{snr_L} \quad snr_T = \frac{snr_S}{snr_L} \quad (13)$$

$$\frac{snr_S}{snr_L} = \frac{snr_S \cdot snr_{ADC}}{\sqrt{snr_S^2 + snr_{ADC}^2}} \quad ; \quad snr_{ADC}^2 = \frac{snr_S^2 + snr_{ADC}^2}{snr_L^2}$$

$$snr_{ADC}^2 \cdot \left(1 - \frac{1}{snr_L^2}\right) = \frac{snr_S^2}{snr_L^2}$$

$$snr_{ADC} = \sqrt{\frac{snr_S^2}{snr_L^2 - 1}} \quad (14)$$

$$6.02 \cdot N + 1.76 = 20 \cdot \log \sqrt{\frac{snr_S^2}{snr_L^2 - 1}}$$

$$20 \cdot N \cdot \log 2 + 20 \cdot \log \frac{\sqrt{6}}{2} = 20 \cdot \log \sqrt{\frac{snr_S^2}{snr_L^2 - 1}} \tag{15}$$

$$\log\left(2^N \cdot \frac{\sqrt{6}}{2}\right) = \log \sqrt{\frac{snr_S^2}{snr_L^2 - 1}} \;;\; 2^N = \frac{2}{\sqrt{6}} \cdot \sqrt{\frac{snr_S^2}{snr_L^2 - 1}}$$

$$N = \log_2 \frac{2}{\sqrt{6}} \cdot \sqrt{\frac{snr_S^2}{snr_L^2 - 1}}$$

$$N = \frac{1}{2} \cdot \log_2 \left(\frac{2}{3} \cdot \frac{snr_S^2}{snr_L^2 - 1} \right) =$$

$$= \frac{1}{2} \cdot \left[\log_2 \frac{2}{3} + \log_2 snr_S^2 - \log_2 \left(snr_L^2 - 1 \right) \right]$$

$$N = \frac{1}{2} \cdot \left[\log_2 \frac{2}{3} + \log_2 \left(10^{\frac{SNR_S}{10}} \right) - \log_2 \left(10^{\frac{SNR_L}{10}} - 1 \right) \right] =$$

$$N = \frac{1}{2} \cdot \left[\log_2 \frac{2}{3} + \frac{SNR_S}{10} \cdot \log_2 10 - \log_2 \left(10^{\frac{SNR_L}{10}} - 1 \right) \right] \tag{16}$$

If the SNR of the input signal to be converted and the SNR of the converter system are both known depending on N. Therefore, it will be easy to calculate N from the loss of the signal quality which can be assumed. To do this, it is enough to apply (16). Finally, it is important to point out that in real systems the ENOB (Effective Number of Bits) [8] is used instead of N. Therefore, equation (16) may be changed to (17).

$$ENOB = \frac{1}{2} \cdot \left[\log_2 \frac{2}{3} + \frac{SNR_S}{10} \cdot \log_2 10 - \log_2 \left(10^{\frac{SNR_L}{10}} - 1 \right) \right] \tag{17}$$

Fig. 5 presents the value of N that should be taken when the SNR of the signal and the SNR to loss are known. This figure has three traces corresponding to three different losses of SNR (0.1, 1.0 and 3.0 dB).

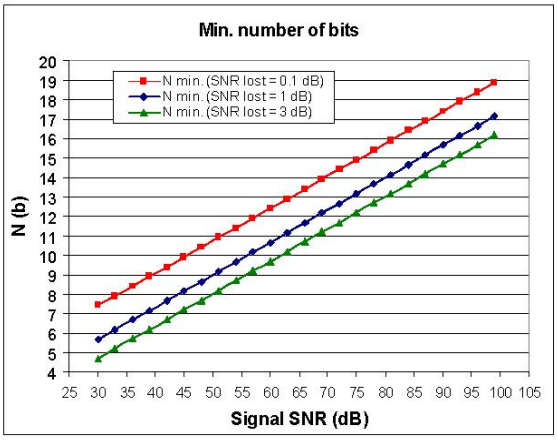

Fig. 5. Minimum number of bits needed versus the SNR lost in a certain input sampled signal with a certain SNR.

After the minimum number of bits has been obtained the optimal conversion frequency must be calculated. This is the frequency at which all code bins have almost one sample and when the signal has the maximum slope only one sample. In this way, the loss of some code, due the amplitude change of the signal between two consecutive samples is greater than the corresponding increment between two consecutive codes (Fig. 6), is avoided. Moreover, obtaining several samples of the signal corresponding to the same code is also avoided (Fig. 7). The optimal frequency corresponds to Fig. 8, in which we can see how, in the portion of the signal with the greatest slope, there is the minimum code bin, in other words only one sample per code bin that guarantees that there is almost one code bin per sample.

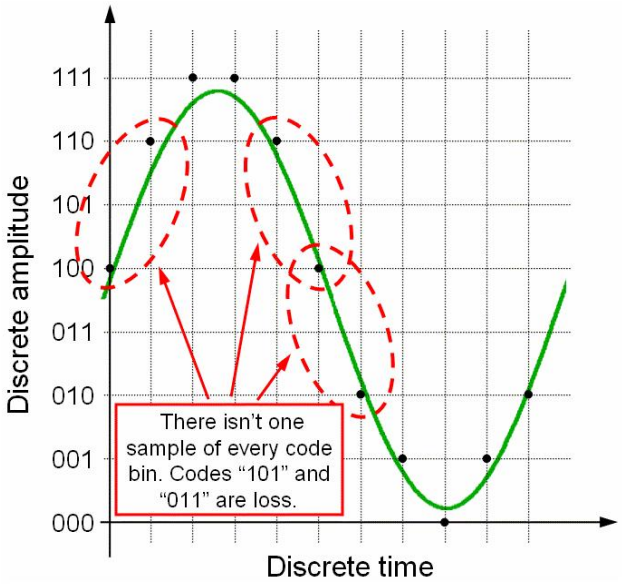

Fig. 6. Signal sampled at a too slow frequency ($f_s = 11 \cdot f_i$).

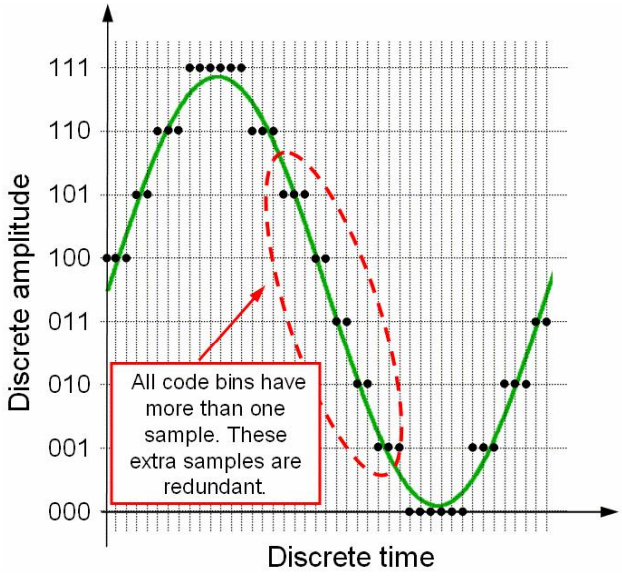

Fig. 7. Signal sampled at a too fast frequency ($f_s = 33 \cdot f_i$).

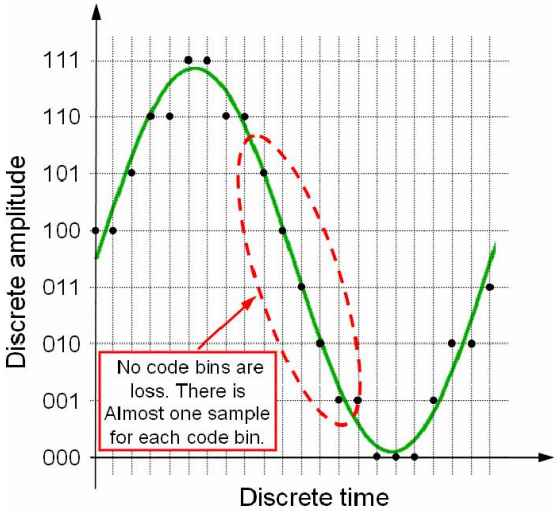

Fig. 8. Signal sampled at the optimal frequency ($f_s = 22 \cdot f_i$).

To obtain that optimum frequency value the maximum slew rate of the signal must be taken into account. If the signal is composed of a set of harmonic components, the component with greater frequency must be considered. Either way, the maximum slew rate must be considered. To do the analysis it is supposed that the signal represented by (18) has the greatest frequency f_i and its amplitude corresponds with A_0=$FSR/2$. Differentiating (18) two times and equalizing it to zero, the point of maximum slope is obtained (20), this is the zero crossing point. Substituting this point in (19) it gives the expression of the greatest slope (21).

$$v(t) = A_0 \cdot \sin(\omega \cdot t) \tag{18}$$

$$\frac{dv(t)}{dt} = A_0 \cdot \omega \cdot \cos(\omega \cdot t) \tag{19}$$

$$\frac{d^2 v(t)}{dt} = A_0 \cdot \omega^2 \cdot \sin(\omega \cdot t) = 0 \quad ; \quad \omega \cdot t = 0, \pi, 2\pi \ldots \tag{20}$$

$$\left.\frac{dv(t)}{dt}\right)_{\max} = A_0 \cdot \omega = A_0 \cdot 2 \cdot \pi \cdot f_i \tag{21}$$

$$f_s \geq \frac{2^{N-1}}{FSR} \cdot \frac{FSR}{2} \cdot 2 \cdot \pi \cdot f_i \tag{22}$$

Now, the slope of the signal is compared to the maximum slope that the sampled process can detect (Fig. 9). This value must be greater than or equal to the expression (21), thus the general equation (22) is obtained, which can be simplified to (23). In the example of Fig. 6 to Fig. 8, the number of bits is 3, and the number of samples per signal period is 11, 33 and 22 respectively.

Applying the equation (23) the relation (24) is obtained. This result demonstrates, as would be expected, that the value of 22 samples per period is the optimum number.

$$f_s \geq \left(2^N - 1\right) \cdot \pi \cdot f_i \tag{23}$$

$$f_s = \left(2^3 - 1\right) \cdot \pi \cdot f_i = 21.98 \cdot f_i \tag{24}$$

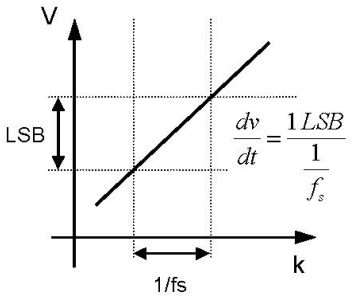

Fig. 9. Maximum slew rate of the signal's voltage.

III. SIMULATION RESULTS

Fig. 10 shows a signal with a SNR of 15 dB that is sampled at a frequency f_i=$51f_s$ by an ADC of 4 bits. The ADC has a SNR equal to 25 dB therefore it has 10 dB more than the signal, according to the presented rule the lost SNR of the signal becomes 0.137 dB, which is an acceptable result because it is near the theoretical value of 0.1 dB.

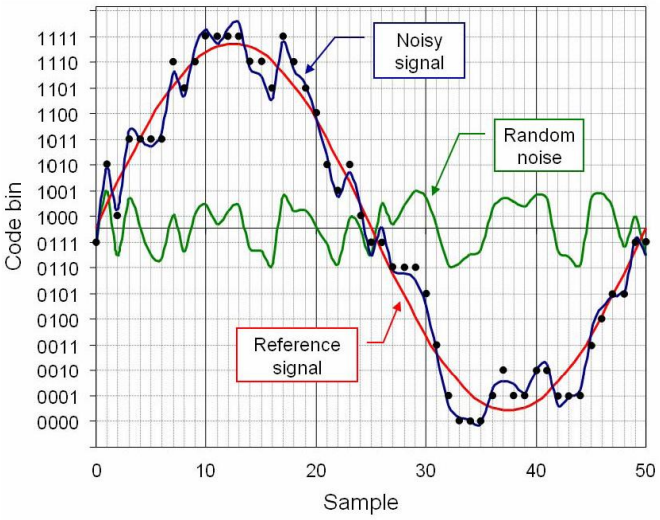

Fig. 10. Example of a noisy sampled signal with 15 dB of SNR.

IV. EXPERIMENTAL RESULTS

In order to prove the simulation results which validate the rules presented in this work, two experiments are presented in this section. To do this an ADC including conditioning and converters circuits is used to acquire the data and then the spread sheet in the PC is utilized to analyze them.

In the first experiment a set of noisy signals formed by a fixed 24 kHz sinusoidal component and by a variable random noise are acquired by the ADC and then analyzed (Fig. 11).

In the second experiment the acquired noise signal is fixed at 25 dB (Fig. 12) and the SNR of the ADC is varied from 20 to 42 dB by connecting the necessary number of bits (from 3 to 8) (Fig. 13). Each time the number of bits is changed the ADC SNR is measured by acquiring the sinusoidal signal but disconnecting the noise. After this, the noise is added to the sinusoidal signal and the result is acquired in order to be analyzed by the spread sheet (Fig. 13).

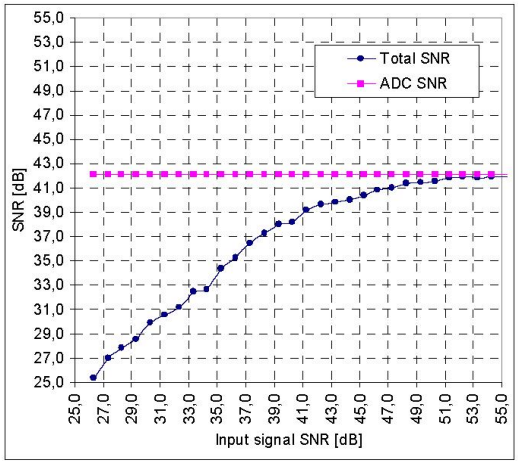

Fig. 11. Result from sampling, with a fixed ADC SNR of 42 dB, signals with different SNR.

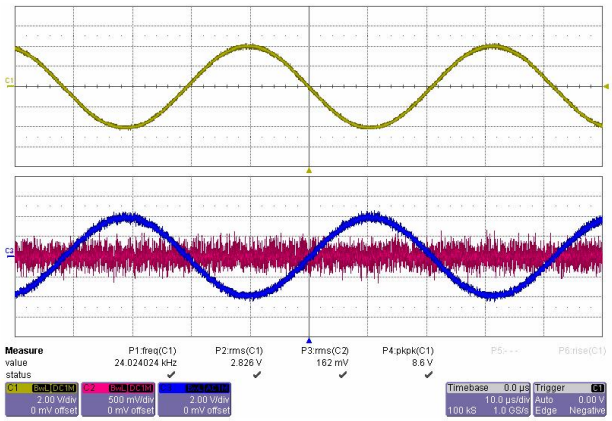

Fig. 12. Oscilloscope screen with the input sinusoidal (C1), the noise to be added (C2) and the output noised sinusoidal of 25 dB of SNR.

In both experiments the sampled rate is maintained at 24 MHz and, according to (23) and taking into account that the maximum number of bits in the experiments is 8 b, the size M of the data record has been established at 1 k samples and so the frequency of the signal to 24 kHz.

Fig. 11 shows that the total SNR does not improve when the input signal SNR is 10 dB over the ADC SNR. Therefore, the ADC performance limits the resulting SNR.

Reciprocally, Fig. 13 shows that when the ADC SNR gets over in 10 dB the input signal SNR, in this case equal to 25 dB (8 Vpp sinusoidal plus 162 mV rms white noise), the final SNR does not improve and thus, sampling the signal with a major resolution is pointless.

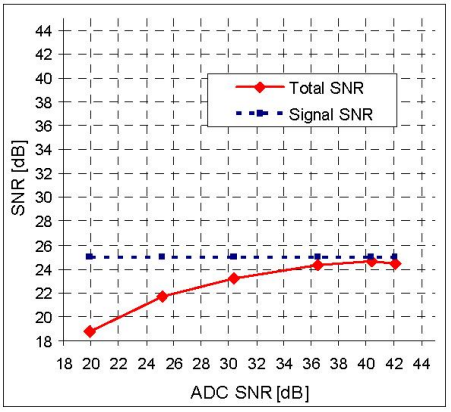

Fig. 13. Result from sampling the 25 dB signal varying the ADC SNR.

V. CONCLUSIONS

When the resolution of an ADC must be selected in an optimal way following rules can be useful:

- Select the ADC with a SINAD of 10 dB above the signal's SNR.
- For a certain maximum SNR to be lost in the conversion process, select an ADC with an ENOB greater than the one given by the expression (17).
- Finally, after selecting the ADC resolution, select the sampled frequency given by expression (21).

These applied results have been initially proved by simulation and after by real experiments.

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