Evaluation Engineering May, 2003

# Are ΣΔ ADCs Greek to You?

**Monotonicity, linearity, and more bits for less money—why wouldn't you use a sigma-delta ADC?**

*by Tom Lecklider, Senior Technical Editor*

If only real-world signals were digital instead of analog. Because they're not, data acquisition systems must amplify, filter, and then digitize analog input signals before manipulating the resulting digital bits in meaningful ways. Regardless of how fast or clever the software routines are, **system performance is set by the characteristics of the analog-to-digital converter (ADC).**

How many types of ADCs can you name in less than a minute? Most test engineers are familiar with **flash** ADCs used in fast digital oscilloscopes. They also understand the noise-rejection capabilities of much slower, **dual-slope** converters used in multimeters and data acquisition systems.

Successive approximation (**SAR**) ADCs fall between these extremes in terms of both speed and resolution. Typically, a sample-and-hold circuit is required with a SAR converter to provide a constant input during the N-step conversion process, where N is the number of bits of resolution.

**Pipelined** converters comprise multiple stages of conversion, each successive stage adding a number of bits of resolution and a delay to the overall digital output. Flash converters often are used within the separate stages of a pipelined circuit with a means of calibration to extend flash converter linearity.

There are many variations within these major categories, all designed to improve speed, accuracy, resolution, or cost. So, if you listed five or six types, you did very well.

## Sigma-Delta ADCs

Did you include a sigma-delta or delta-sigma ADC in your list? *At one time, there was a distinction between the terms, but they are used interchangeably today.* Different companies have standardized on the use of one name or the other to describe their ADCs.

## The Modulator

In its simplest form, the converter comprises a 1-b ADC, an integrator, a 1-b DAC, a means of summing the signal input and feedback from the DAC, and an output filter. The circuitry ahead of the filter is collectively termed the modulator (**Figure 1**).

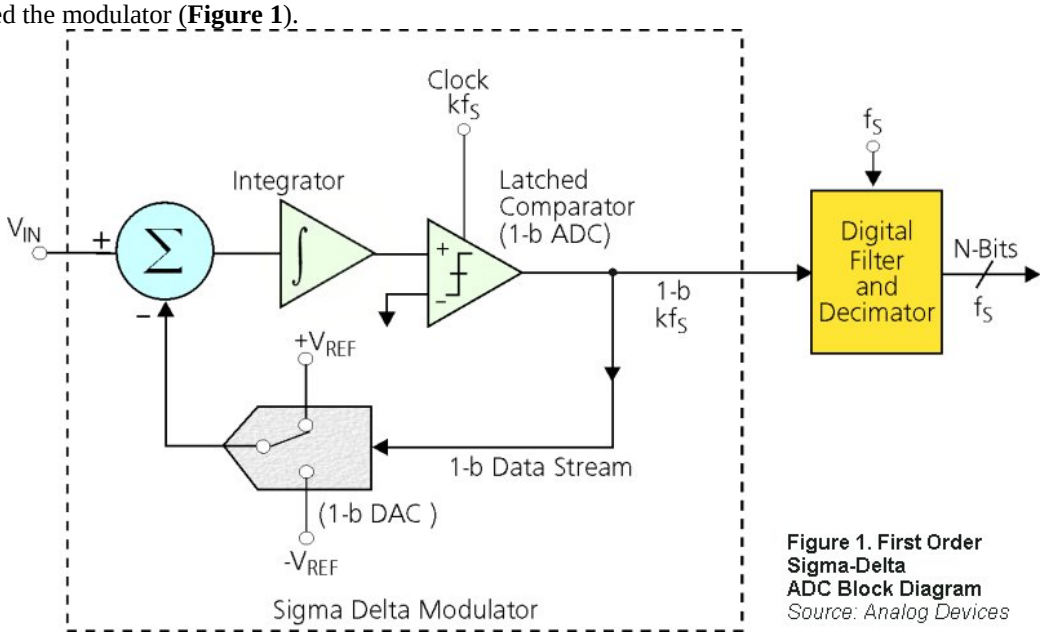


**Figure 1. First Order Sigma-Delta ADC Block Diagram**
*Source: Analog Devices*

In the same way that the output of a digital rate multiplier represents the value of its digital input word, the output of a sigma-delta modulator corresponds to the value of the analog input signal. In both cases, the **density** of ones in the serial digital output is proportional to the input signal value.
Oversampling the input by a ratio much higher than required by Nyquist causes the digitization noise in the signal bandwidth to be reduced by the oversampling ratio (**OSR**). In addition, the modulator redistributes energy from the baseband to higher frequencies, providing further noise shaping. **Figure 2** shows the effects of **oversampling and noise shaping.**

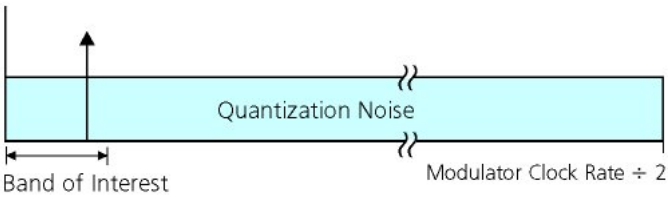


**Figure 2a. Oversampling Spreads Out Quantization Noise**
*Source: Analog Devices*

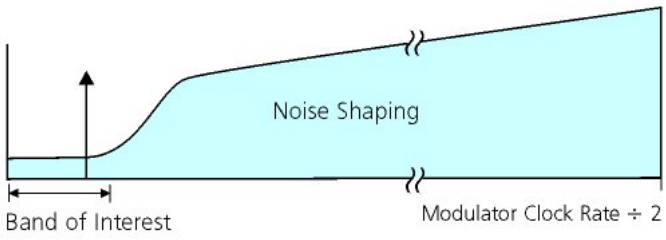


**Figure 2b. The Sigma-Delta Modulator Shapes the Noise Spectrum**
*Source: Analog Devices*

Modulators containing N stages of integration, so-called higher-order modulators, increase the signal-to-noise ratio (SNR) by a factor of (6N+3) dB. Most manufacturers have adopted modulators with three, four, or five stages of integration.
A first-order modulator has the advantage of being inherently linear and stable. Unfortunately, first- and second-order modulators produce low-level idle tones when driven at or near to DC. Energy from the limit cycle switching of the 1-b ADC is concentrated at a particular frequency and not entirely removed by subsequent filtering.
Third- and higher order modulators alleviate most idle tone problems and improve the SNR for a given OSR but increase circuit complexity and may reduce stability. To address the stability issue, some designs cascade four integrators without intermediate feedback. Alternatively, the first two stages may have intermediate feedback, followed by two stages without feedback.[1]

## The Output Filter

Assuming that the digital **bit stream** from the modulator correctly represents the input signal amplitude, it's the job of the digital output filter to produce the actual data words. It does this by averaging the modulator's bit stream, which improves resolution, and removing energy at frequencies above its passband. The **Sinc$^n$ filter** characteristic is particularly popular because it has a series of nulls that can be used as 50-Hz or 60-Hz notches to eliminate AC power interference.
As an example, consider the fifth-order Sinc filter used in the *Burr Brown (Texas Instruments)* Model ADS1251 24-b delta-sigma ADC. Figure 3 shows the equally spaced nulls and the passband ahead of the first null. The system clock frequency is divided by six to drive the modulator, and the modulator sampling rate has an OSR of 64. For that reason, the filter must decimate the modulator data rate by 64, and the data output rate equals the system clock rate divided by 384.
The first null frequency is equal to the data output rate, which also is the increment between successive nulls. For example, to reject 60 Hz, the data output rate should be 60 Hz and the system clock equal to 60 × 384 = 23.040 kHz.
System clocks up to 8 MHz can be used with this device, but the output data rate and null locations scale with the clock frequency. This means that additional, external filtering is needed if both a wide bandwidth

and 60-Hz rejection are required.

The **data output rate** referred to is the maximum rate at which data is loaded into the output data register. After the data-ready line goes low, successive bits of the 24-b offset two's complement formatted data are output on the positive-going edges of the SCLK signal. Data-ready and SCLK handshaking synchronizes the output data to devices such as microcontrollers or microprocessors that will process the data.

The output filter design determines the ADC's **latency**. In addition to the time taken to convert the input signal, the ADS1251 filter requires five complete conversions to settle to full accuracy. This means that the data at the output of the filter is not valid until after 5 × 384 = 1,920 system clocks. In general, a $Sinc^n$ filter requires n conversion cycles to settle. In some ADCs with different filter designs, the latency can be as high as 40 conversions.

Latency is not a major problem in single-channel applications. However, in multiplex applications, it can severely degrade throughput and complicate system timing. This is the reason that manufacturers have developed so-called zero-latency or no-latency products. Basically, they have designed filters and modulators that can be reset and settle to the required accuracy within one conversion.

The *Intersil* HI7188 eight-channel, 16-b A/D subsystem is a good example of a device with automatic channel switching and zero latency. According to the data sheet, "The microsequencer supports on-the-fly multiplexer reconfiguration…and zero step response delay during internal or external multiplexer channel changes….

Data out of the filter is available after 201 bits are received from the modulator."[2]

AC power noise is removed in this ADC by a process of cancellation so that the output filter is not constrained to provide a null at 50 Hz or 60 Hz. The signal is sampled at either a 240-Hz rate for 60-Hz power systems or at a 200-Hz rate for 50-Hz power. Groups of four successive samples are stored and averaged for each channel.

Considering only the 50-Hz or 60-Hz part of the signal, the four samples always will fall at the same points within a cycle. There will be two pairs of equal magnitude but opposite polarity points that will average to zero.

## Calibration

In addition to the modulator, filter, control circuitry, and possibly input multiplexing, a sigma-delta ADC may contain selectable gain preamplifiers and some means of calibration. For example, in the HI7188, a programmable gain instrumentation amplifier is provided with selections of ×1, ×2, ×4, or ×8 gain. The amplifier is after the multiplexer, and control registers support different gain selection per channel.

Changing the gain changes the size of the input sampling capacitors, which, in turn, alters the ADC input impedance. Because the sampling capacitors are not exactly in the 1, 2, 4, 8 ratio required, neither will the gain be exact. To correct offset and gain errors, the on-chip micro-controller records conversion results for zero, +full scale, and -full scale inputs. Correction factors are derived from these measurements.

According to the *Intersil* HI7188 data sheet, "A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the gain, bipolar, or unipolar input range."

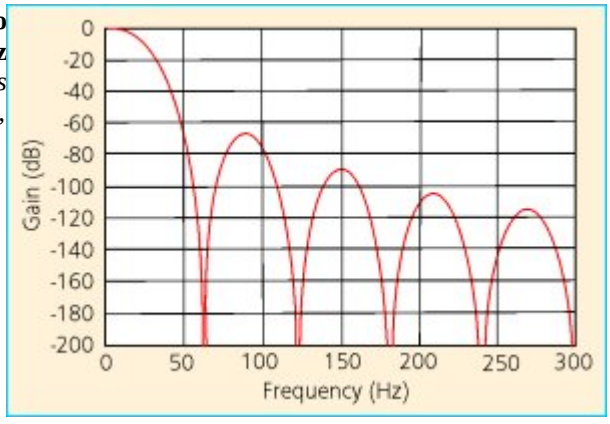


**Figure 3. $Sinc^5$ Output Filter Response Set to Reject 60 Hz**

*Source: Texas Instruments*

Although a calibration capability has been provided, you are left with an uneasy feeling. Calibration is very important if the full accuracy of the ADC is to be achieved. But how can you be certain when it should be done? For example, should it be performed very often, or should sensors be used to determine that the ambient operating temperature has changed?

One solution has been provided in the *Linear Technology* LTC2440 24-b differential delta-sigma ADC with on-the-fly calibration. Offset and gain errors are automatically corrected during each conversion cycle.

Several LTC24xx variants are available with different feature mixes. For example, the LTC2418 is a fully differential device with 16 single-ended or eight differential multiplexed inputs. The LTC2421 and

LTC2422 are two-channel, 20-b ADCs that automatically alternate the single-ended inputs for use in pseudodifferential measurement systems.

## User Comments

When we asked several data acquisition companies about their experience with sigma-delta converters, we received a wide variety of what seemed to be inconsistent answers.

For example, Gary Schneider, a senior product manager at *Nicolet Technologies*, replied that his company used sigma-delta converters in a dynamic signal analyzer, but that the devices were totally unsuited to data acquisition in the time domain. He explained that the very steep brickwall filter used in the converter allowed a wide input bandwidth in comparison to the sampling frequency, but that the poor filter phase response severely distorted transients.

The president of *Microstar Laboratories*, Neil Fenichel, said that good analog anti-alias filters are essential for frequency-domain data acquisition. Sigma-delta ADCs lead to aliasing, which is especially pronounced at low frequencies. If the ADC clock rate is variable, the anti-alias filter cutoff must be adjusted to match the sampling rate.

Other companies that replied didn't mention transient response or aliasing. "*National Instruments* has used sigma-delta ADCs for several years and developed products that deliver high accuracy for DC and AC applications," commented Armando Valim, the company's sound and vibration product manager. "For example, at low speeds, the new NI PXI-4070 **FlexDMM** employs FlexADC circuits that exploit the advantages of the sigma-delta converter. The lowpass filter uses the noise shaping necessary for good performance across all resolutions. The unique architecture of the FlexDMM offers a continuously variable reading rate from <5 S/s at seven digits to 1.8 MS/s at three digits."

Also expressing his enthusiasm for the sigma-delta approach was Thomas Lawson of *Lawson Labs*. "We have introduced 10 products based on sigma-delta conversion, and all 10 still are being made and sold. In general, Sigma-Delta ADCs will provide the best resolution, stability, and accuracy for the money as long as they are fast enough for the application.

"Sigma-delta converters allow users to get better results with less effort," he continued, "because they are more forgiving. For near-DC measurements, the low-pass characteristics of sigma-delta conversion make power distribution, shielding, grounding, and decoupling less critical. But, there is no magic involved, and for optimal performance, all these factors still must be addressed."

These apparently conflicting comments relate to how the ADC output filter has been constructed and to what extent the input signal has been band limited. Using an analog filter to remove the input signal's high-frequency components effectively eliminates aliasing. However, an overshooting and oscillating transient response is characteristic of the very steep rolloff $Sinc^n$ filter used in almost all integrated sigma-delta devices.

Providing more flexibility, the *Analog Devices* AD7724 device is a dual- channel, sigma-delta modulator without output filtering. The user connects the modulator outputs to a digital signal processor and designs whatever filter characteristic he requires. Similarly, the *Intersil* HI7188 device uses an integrating low-pass output filter rather than a filter with a $Sinc^n$ characteristic.

## Conclusion

Sigma-delta ADCs are **inherently monotonic**, no matter how many bits of resolution they provide. Performance is designed in and does not depend on exact component values or component matching. This characteristic is very important to a manufacturer, commented Chris Mostoller, *Maxim*'s business director for ADCs.

He said that sigma-delta converters are displacing traditional dual-slope ADCs in the panel-meter market, partially because testing conventional high-resolution ADCs is expensive. Great care still must be taken with sigma-delta products, but linearity and monotonicity are guaranteed by design. As a result, testing can be much faster and cost less.

Another way that manufacturers are competing and increasing the market for sigma-delta converters is through more levels of integration. For example, some models have very accurate internal clocks, eliminating the space and cost of an external crystal. Built-in calibration also reduces cost and simplifies system design. Simplifying the use of sigma-delta converters was a point that Mr. Mostoller returned to often.

Because these ADCs don't rely on accurate or closely matched components, they lend themselves to integration using low-cost CMOS processes. Manufacturers like making these kinds of parts, and they are easier to test than conventional converters.

**There is no question that sigma-delta ICs are the lowest cost ADCs.** As solutions to issues such as

latency, calibration, and external clocking continue to be introduced, the devices will become even more popular with designers.

However, **like most things that seem almost too good to be true, there are catches:** You must ensure that aliasing does not corrupt your signal and beware of the transient response of integrated sigma-delta converters.

If you are attracted by the many benefits sigma-delta ADCs have to offer, discuss your application with the appropriate manufacturer's technical support engineer. Be sure to cover aliasing and transient response in sufficient detail so you can be sure a sigma-delta part is right for you.

**References**

1. Noriega, G., "Sigma-Delta A/D Converters – Audio and Medium Bandwidths," RMS Instruments, Technical Note DT3, 1996, http://www.rmsinst.com/dt3.htm

2. "8-Channel, 16-Bit, High Precision, Sigma-Delta A/D Sub-System," Intersil data sheet HI7188, 2000.

**FOR MORE INFORMATION**

on basic sigma-delta ADC operation enter these rsleads URLs

www.rsleads.com/ee305-228

www.rsleads.com/ee305-229

on low-frequency sigma-delta applications enter this rsleads URL

www.rsleads.com/ee305-230

**Realizing an ADC's Full Potential**

As experienced engineers know, **buying a high-resolution ADC is one thing**. **It's quite another to achieve the full performance of the part in practice.**

As a guide to some of the factors influencing the use of high-precision ADCs, we've compiled a list of suggestions from several manufacturers' data sheets.

Underlying the list is the need to introduce as little noise as possible.

For example, consider an ad for the *Linear Technology* LTC2440: "With only 200 nV of rms noise, it has enough effective resolution to provide 500,000 counts for a ±50-mV input span." Without getting into details of how the peak values of the IC's random noise affect several levels out of the 500,000, adding even 1 µV of layout-related noise clearly is too much in this case.=

The list includes tips on the choice and use of components as well as PCB layout.

- Use a differential input ADC for best noise performance.
- Use a very low-noise, low-drift reference diode and filter it well.
- Don't run digital lines under the device because switching noise may couple into the die. It can be aliased into the passband and show up as an offset error.
- Use separate analog and digital ground planes with no overlap between them. If more than one converter is used, connect the planes at a central location. Determining the point at which to connect the two planes may take some experimentation.
- Decouple VDD to ground with a 10-µF electrolytic or tantalum capacitor in parallel with a 0.1-µF ceramic capacitor, all placed as close as possible to the pin being decoupled.
- Minimize the ground path impedances that may appear in series with the input and reference signals and reduce the current that may flow through these paths. The ground pin should be connected to a low-resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance.
- The input signal ground, the reference signal ground, the digital ground, and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to the ground pin as possible.
- Driving all digital CMOS signals to full levels minimizes potential errors due to additional ground-pin current.
- Control signal overshoot and undershoot can cause significant ground-pin current disturbances. Minimize reflections by keeping the tracks short. A driver producing a 1-ns transition signal should be connected to the converter with a trace <2.5". Alternatively, all control lines must be terminated to eliminate reflections. Parallel terminations raise power levels. Double-ended series terminations work well without increased power.
- Because of the switched capacitor networks used in integrated sigma-delta converters, small switching current spikes appear at the input and reference pins. The signal and reference impedances must be low enough to minimize errors due to this effect.
- Don't put ceramic decoupling caps side by side. Run them end to end so their electric fields don't interact.

Return to EE Home Page

**Published by EE-Evaluation Engineering**