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General Analysis of Resolution Enhancement on Time-Synchronized Sampling and Its Multi-Resolution Solution in 20GSPS Acquisition System

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ABSTRACT Multiple resolutions have become a new feature required in ultra-fast data acquisition systems (UF-DASs) for various high-end applications, especially for large-scale physical experiments and radar equipment. However, plenty of repetitive efforts are paid to build various UF-DASs with different resolutions for many similar purposes. In this paper, a system-level sampling solution featuring multi-resolution is explored for UF-DASs to make the trade-off between accuracy and speed. Firstly, a resolution enhancement mechanism based on a time-synchronized sampling technique is studied more generally with probabilistic and statistical theory, and its applicable premise is discussed quantificationally at the same time. Then, a hardware-based reconfigurable structure for the purpose of multi-resolution high-speed sampling is discussed with the combination of time-interleaved and time-synchronized sampling methods. Furthermore, to verify the proposed theory, a prototype with a maximal 20GSPS sampling rate and different resolutions of 8,9,10-bit is established. The experimental results show that three vertical resolutions of 8, 9 and 10-bit are achieved in the same prototype, and the effective-number-of-bit (ENOB) in the two higher resolution modes has been improved remarkably from a single low-resolution analog-to-digital converter (ADC). Therefore, the proposed theory and multi-resolution sampling solution are important guides to the resolution trade-off requirement in ultra-fast acquisition systems.

INDEX TERMS Ultra-fast data acquisition system, time-synchronized analog-to-digital conversion (TSADC), resolution enhancement and multi-resolution sampling.

I. INTRODUCTION

Ultra-fast data acquisition (UF-DAQ) technique plays an important role in modern electronic system design and testing for various high-end applications. According to observations in the past several years, these ultra-fast data acquisition systems (UF-DASs) have emerged with new features: they not only have a great demand for high sampling rate and high resolution, but also present the characteristics of multiple different resolutions in the same system [1], [2].

In large-scale physical experiments, in order to observe the waveform detail of transient physical signals, its wide-band DAS needs to work with more than 5GSPS sampling rate but a low resolution requirement (normally 8-bit); to observe better spectral information, the system is required with higher resolution of 14 or 16 bits [3]. Then several different oscilloscopes should usually be employed for different speeds and resolutions' requirement from the same signal. Similar application requirements can be demonstrated in the failure detection [4], ion accelerators [5], and LIDAR system [6]. Although these application scenarios are diverse, their goals and overall structures on the signal detection have

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great similarity. It not only brings about a lot of repetitive works, but also causes a huge cost of resources and energy. Therefore, a multi-resolution DAS is in high demand that supports different application scenarios and operates in different resolution modes. Such idea has been attempted in LeCroy's digital oscilloscope for time-domain testing with different accuracy observations.[7].

A typical DAS comprises an analog-to-digital converter (ADC) and an embedded controller for control operations. However, due to the constraint of speed-accuracy, high-speed and high-resolution indicators cannot be achieved simultaneously.

There are available on-chip or off-chip capabilities that have been exploited for the trade-off between speed and accuracy of DASs. On-chip technique is a direct way, but it is difficult to achieve high indicators at the same time. The famous sigma-delta ($\Sigma - \Delta$) modulators and cascaded $\Sigma - \Delta$ modulators can be seen as a spectral shaping of noise. They are a typical technique that improving resolution is at the expense of overall sampling rate downgrade. Therefore, this technique is used in low-speed high-precision applications (such as audio and other applications with a resolution over 14-bit). The available off-chip capabilities include oversampling and sliding averaging techniques. For applications where a full Nyquist bandwidth is not needed, the averaging can make the noise floor lower in the desired signal band. By averaging two successive points in a measurement, the effective-number-of-bit (ENOB) can be improved by 0.5-bit.([8]. Extra resolution improvement can be gained with more averaging points. Because of the simple idea of accuracy in exchange for speed in a single channel, these techniques reduce system bandwidth and are not suitable for UF-DAQ applications. Therefore, it is necessary to further study a scheme for improving the accuracy of the DAS while maintaining a high sampling rate.

Another consideration of the trade-off technique is based on hardware sampling architectures by exploiting multiple ADCs in parallel [9]–[12]. As reported in.[9], digital bandwidth interleaving (DBI) can achieve a high sampling rate and bandwidth through a frequency interleaved mode, but the challenge is the difficulty in post-processing for the equalization of all channels. The asynchronous time interleaving (ATI) technique presented in [12] doubles the sampling rate by two ADCs. However, the required mixer circuit introduces extra errors inevitably. The time-interleaved analog-to-digital conversion (TIADC) is an effective way to increase the sampling rate. Due to its flexibility and effectiveness, this architecture has been studied for several decades. The most challenge is the mismatch error calibration between multiple ADCs. Motivated by this, mixed signal calibration [13]–[15] and blind digital processing calibration [16], [17] have been researched. The sampling rate and analog bandwidth of these DASs can be achieved by these techniques.

Similar as the aforementioned architectures, a sampling technique with target of improving the resolution performance is called time-synchronized analog-to-digital conversion (TSADC). This architecture is reported by several literatures [18]–[21] that can be used to enhance the dynamic range and ENOB without the reduction of analog bandwidth. A typical report in [19] proves that TSADC is a method of dynamic range enhancement; in [20], the impact of correlation between signals, noise and harmonics in multi-channel has been investigated in depth. And its circuit applications can also be found in high-resolution ADC design, such as AD9253 designed by Analog Devices Inc.. However, there are still theoretical ambiguities for this method on the nature of resolution enhancement and its applicable constraint. This brings a great obstacle to the practical applications of this method.

In this paper, we focus on resolution enhancement solutions for UF-DAQ systems at high sampling rates. To solve this trade-off problem, we will take full advantage of the respective strengths of TIADC and TSADC. Firstly, we investigate the general theory of TSADC and reveal its nature of resolution enhancement as well as the applicable premise of background noise. Then, a novel sampling solution for UF-DAQ applications is proposed through different hardware reconfigurations that different resolutions in the same system can be achieved by a hybrid structure of TIADC and TSADC. Finally, a multi-resolution sampling prototype is implemented to verify: i) the effectiveness of TSADC resolution enhancement and ii) the feasibility of multi-resolution application in the same sampling system.

The paper is organized as follows: Section II focuses on general analysis of TSADC theory and its simulation; Section III illustrates the methodology and scheme of system deployment for multi-resolution sampling applications; In Section IV, a multi-resolution sampling prototype is implemented by improving an existed 20GSPS/8bit system, and experiments are performed for the effectiveness verification of proposed theory; Section V gives a brief conclusion of this paper.

II. GENERAL ANALYSIS OF TSADC THEORY

A parallel structure composed of M ADCs, as shown in **FIGURE 1**, can be configured as different sampling modes by setting different sampling clock phases ϕ_m on each ADC.

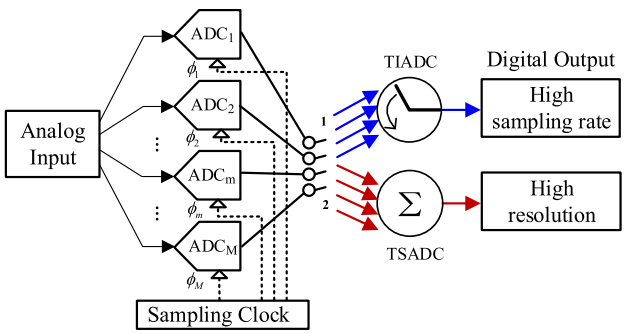


FIGURE 1. The structure of parallel ADC array.

For example, when $\phi_m = m \cdot 2\pi/M$ for $m = 1, 2, \cdots, M$, each ADC in this structure works in a time-interleaved manner to sample the same input signal. And then their output sampled data are combined in time order (switch on position '1' in **FIGURE 1**) into a digital output with high sampling rate, which achieves sampling rate M times of single ADC. This is a typical TIADC system. Nevertheless, if all clock phases are configured as $\phi_m = 0$ for $m = 1, 2, \cdots, M$, all ADCs sample the input signal at the same time. After summing their sampled data into a more-bit stream (switch on position '2' in **FIGURE 1**), high quantization resolution of M times of single ADC can be achieved. This is another hardware parallel sampling mode, called TSADC. Moreover, since the noise among channels is mainly uncorrelated, the ENOB of TSADC can be improved remarkably.

These two sampling modes are both effectively used in DAQ systems. But their advantage is only one side, either high sampling rate or high-resolution. For the trade-off between speed and accuracy, an optimal scheme for UF-DAQ systems featuring high-resolution should be studied.

In this section, we first analyze the quantization model of parallel sampling; and then give out the general principle of TSADC resolution enhancement in terms of probabilistic and statistical theory; Furthermore, the explicit premise of background noise and overall sampling performance are uncovered for the practical sampling applications.

A. QUANTIZATION MODEL

Since the introduced noise in DAS is derived from active devices (such as amplifiers and ADC internal circuitry), these types of noise usually behave as thermal noises and a certain amount of them are generated undesirably. It occurs in all real sampled-data systems even with a direct-current (DC) input signal, which is the reason for the existence of code transition noise in the transfer function of any converters [22]. The thermal noise usually follows Gaussian distribution and represented by Root-Mean-Square (RMS) value [23].

In terms of the quantization theory in...[24], the first-order probability density function (PDF) of quantized variable can be introduced into the quantizing analysis of parallel sampling. The PDF of the quantized variable from the quantizer output may be obtained by strictly linear operations performed on the PDF of the non-quantized variable from the quantizer input. It is assumed that $f(\widehat{x};\sigma)$ denotes the statistics PDF of the input quantizer, where $\widehat{x}$ is the value of a random variable $\widehat{X}$ of the quantizer input signal and σ is its standard deviation. Moreover, $\widehat{x}$ is usually a continuous amplitude with a Gaussian distribution, whereas the output variable X has a discrete value x that is an integer multiple of the least significant bit of ADC, denote as q.

In actual acquisition systems, thermal noise determines the quantizing accuracy for wide-band signals beyond other noise sources, such as jitter or aperture. **FIGURE 2** sketches the PDFs of quantizer input and output in the case of DC signal with thermal noise. The area within a certain quantized band

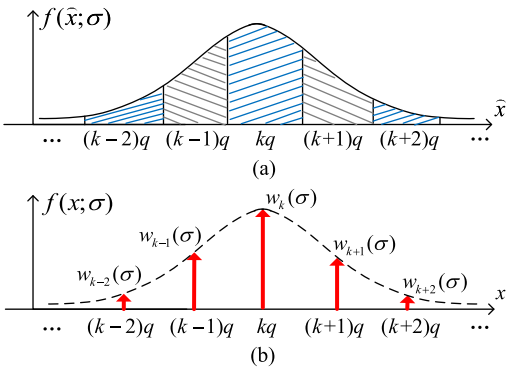


FIGURE 2. PDFs of quantizer (a) input and (b) output in the case of DC signal with thermal noise.

$(\pm q/2)$ under $f(\widehat{x};\sigma)$ is compressed into an impulse value through the quantization process. Therefore, the output PDF $f(x;\sigma)$ is transferred into a train of impulse values which locate at the center of quantized band, expressed as

$$f(x;\sigma) = \sum_{k=-\infty}^{\infty} w_k(\sigma)\delta(x - kq), \tag{1}$$

where index k indicates the digital code of a specific quantized value over q, and $k \in [0, 2^b - 1](k \in \mathbf{Z}$, b is the resolution of ADC) because the distribution of x is finite. Besides, the weight $w_k(\sigma)$ is the integral area of quantized band, given by

$$w_k(\sigma) = \int_{(k-1/2)q}^{(k+1/2)q} f(\widehat{x};\sigma)\, d\widehat{x}. \tag{2}$$

These weights meet the constraint of $\sum_{k=-\infty}^{+\infty} w_k(\sigma) = 1$. This special type of sampling is called an 'area sampling' in literature [24] and the 'sampling period' is q.

B. VERTICAL RESOLUTION

According to the quantization model, the behavior of resolution enhancement for TSADC systems can be further revealed. Consider a general case that $f(x;\sigma)$ mainly covers two impulse values (quantizing bands) at kq and $(k+1)q$ center points, as shown in **FIGURE 3.**. Then other quantizing

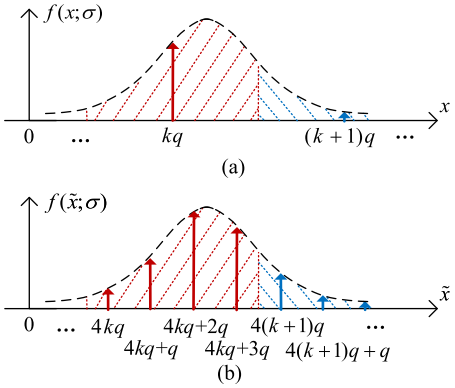


FIGURE 3. A PDF instance of output signal in (a) single channel and (b) 4-channel TSADC system.

bands still exist but just appear with a small probability. Therefore, quantized variable x is a random variable that obeys '0-1' distribution of Bernoulli experiments, and its PDF can be written as $f(x;\sigma) = w_k(\sigma)\cdot\delta(x-kq) + w_{k+1}(\sigma)\cdot\delta(x-(k+1)q)$.

In an M-channel TSADC system, the total sampled data before digital summing can be written as a matrix

$$\boldsymbol{Q} = \begin{pmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \cdots \\ \mathbf{x}_M \end{pmatrix}_{M\times 1} = \begin{pmatrix} x_{11} & x_{12} & \cdots & x_{1N} \\ x_{21} & x_{22} & \cdots & x_{2N} \\ \cdots & \cdots & \cdots & \cdots \\ x_{M1} & x_{M2} & \cdots & x_{MN} \end{pmatrix}_{M\times N}, \tag{3}$$

where $\mathbf{x}_i = \begin{pmatrix} x_{i1} & x_{i2} & \cdots & x_{iN} \end{pmatrix}_{1\times N}$ is the data vector of the i-th channel, $i = 1, 2, \cdots, M$, and N is the data quantity. x_{ij} denotes a determined sampling value, $j = 1, 2, \cdots, N$. After the summing, M vertical sequences of sampled data are formed into a sequence $\tilde{\mathbf{Q}} = \begin{pmatrix} \tilde{x}_1 & \tilde{x}_2 & \cdots & \tilde{x}_N \end{pmatrix}_{1\times N}$, where $\tilde{x}_j = \sum_{i=1}^{M} x_{ij}$. This summing process can be thought as an independent Bernoulli experiment, so the new random variable $\tilde{x}$ leads to a Binomial distribution, that is $\tilde{x} \sim B(M, w_m(\sigma))$, $m = 0, 1, \cdots, M-1$.

Based on the quantization model, the PDF of $\tilde{x}$ is transferred to a train of impulse values

$$f(\tilde{x};\sigma) = \sum_{m=0}^{M-1} w_m(\sigma)\delta(\tilde{x} - Mkq - mq). \tag{4}$$

$w_m(\sigma)$ is the new weight of each impulse value, written as

$$w_m(\sigma) = C_M^m w_k^m(\sigma)(1 - w_k(\sigma))^{M-1-m}, \tag{5}$$

where $C_M^m = \frac{M!}{m!(M-m)!}$, and $w_k(\sigma)$ has been given in (2). The new weight $w_m(\sigma)$ also meets the constraint of $\sum_{m=0}^{M-1} w_m(\sigma) = 1$. After the summing, the quantity of impulse values in each quantizing band is increased from one to M ($M \geq 1$). A more intuitive explanation is illustrated in **FIGURE 3** with a comparison between the output signal of single ADC and four-channel TSADC. In this case, three new quantizing values in each band are generated by the code summing. In other words, the quantity of impulse values in the latter increases four times, which means the maximum of output codes is also enlarged four times. More impulse values mean more vertical quantizing steps. And the increase quantity of impulse values is strongly related to the channel quantity. At the same time, this can also be extended to the case of arbitrary channel quantity. Generally, an M-channel TSADC can increase (M-1) output codes (quantizing steps) in each quantizing band.

Next, we discuss a more general case of full-scale input signal passing through an M-channel TSADC system. The total number of codes $\widehat{T}$ can be expressed as

$$\widehat{T} = T + (T-1)(M-1) = MT - (M-1), \tag{6}$$

where a number of $T_a = (T-1)(M-1)$ additional codes are interpolated into the original T codes from single ADC, where $T = 2^b$. As a result, the expression for actual quantizing resolution is

$$b_q = \log_2 \widehat{T} = b + \log_2[M - \underbrace{(M-1)\cdot 2^{-b}}_{\text{missing bits}}]. \tag{7}$$

In (7), a term of missing bits is exposed, because there are no interpolated codes in the range of upper than the maximum code and lower than the minimum code. Therefore, the TSADC is not an ideal $b_q - bit$ converter. However, when $b \geq 7$, the missing bits $(M-1)\cdot 2^{-b}$ is less than 1% of the major bits M, which means $M-(M-1)\cdot 2^{-b} \approx M$. Therefore, the enhanced vertical resolution (i.e. enhanced quantizing resolution) is $b_{eq} = b_q - b \approx \log_2 M$. This is an important theoretical basis for revealing the resolution enhancement of TSADC system.

C. PREMISE CONDITION ANALYSIS

Note that the enhanced quantizing resolution is based on the statistics characteristics of summed result of quantizing values, which requires that $f(x;\sigma)$ covers more than one impulse in each least quantizing band of new summed result. Otherwise, there is no difference between $f(\tilde{x};\sigma)$ and $f(x;\sigma)$, which leads that TSADC makes no contribution to resolution enhancement. Considering about the applicability of concrete cases, more explicit premise for resolution enhancement in TSADC systems should be further discussed.

With the diminution of the standard deviation, less impulses can be covered by $f(x;\sigma)$. **FIGURE 4** illustrates a specific instance of input signal PDF in TSADC systems, extreme low noise condition in TSADC systems, where the noise level is so low that only one impulse value is covered and located at the center of one quantizing band. Because the quantizer can only recognize the measured signal in $[x-q/2, x+q/2]$ as an integer x, the code k in this instance is determined by $[(k-1/2)q, (k+1/2)q]$. In terms of the Pauta Criterion, the maximum occurrence possibility of single impulse value should satisfy that the possible magnitude (shaded area in the figure) needs locate in the range of $\pm 3\sigma$ deviated from the distribution center μ. It requires the standard deviation σ of norm distribution meets $\sigma/q < 1/6$. With the increase of σ, at least two codes may be quantized by different converters, which means $f(x;\sigma)$ consists of more than one impulse value. Therefore, it can be concluded that

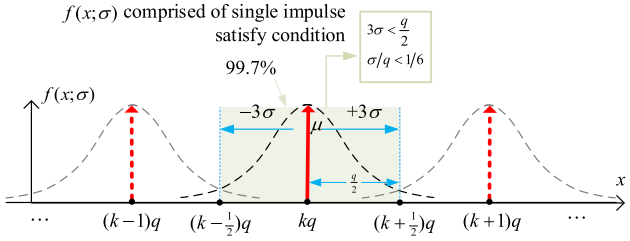


FIGURE 4. The PDF instance of extreme low noise condition in TSADC systems.

the premise in TSADC systems requires σ of noise should be more than the critical value $q/6$. Thereupon, a more comprehensive expression of TSADC quantizing resolution enhancement can be proposed with the constraint of noise, written as

$$b_{eq} = \begin{cases} 0 & 0 < \sigma/q < 1/6 \\ \log_2 M & \sigma/q \geq 1/6\,. \end{cases} \tag{8}$$

That is to say a TSADC structure is equivalent to a higher resolution ADC under this precondition at $\sigma/q \geq 1/6$. The enhanced quantization bit is almost $b_{eq} = \log_2 M$ and more precise for the resolution of original ADC $b \geq 7$. Notice that the condition of $b_{eq} = 0$, for high performance ADCs with very low noise, TSADC has no longer an effect of resolution improvement. In order to improve the resolution in such case, it is possible to use dithering technique [25], which is a useful method in ADC design.

Consequently, TSADC systems can achieve theoretically a maximal quantizing resolution of b_q-bit from M ADCs of b-bit. A measured value σ/q determines whether it meets the condition of resolution enhancement, so it should be first estimated before employing a TSADC system.

D. ENOB ANALYSIS

Although the foregoing sections has completely confirmed that the quantizing resolution in a TSADC system can be enhanced remarkably, the real manifestation of a DAS performance should be further evaluated by its ENOB.

In brief, ENOB can be derived according to the measurement value of signal to noise and distortion (SINAD), that is

$$ENOB = \frac{1}{6.02} \cdot (SINAD_{dB} - 1.76 + 20\log\frac{V_{fullscale}}{V_{in}}). \tag{9}$$

Unavoidably, the original signal s is corrupted by thermal noise, denote as n, in practice. On the other hand, after sampling and quantization, quantization noise is introduced inevitably. For an M-channel TSADC system, the total noise v_{tot} of final output values is given by the mean-square error (MSE) of digitized signal, represented as

$$v_{tot}^2 = MSE\left(\bar{x}_j - s_j\right). \tag{10}$$

where, s_j denotes the j-th voltage of total sampled points in original signal and $\bar{x}_j = \frac{1}{M}\sum_{i=1}^{M} x_{i,j}$ is the ensemble mean of the j-th sampled data performed by all different channels at the same time. If the signal is averaged by huge times records, the thermal noise is almost disappeared and quantized data is silent without noise exposure, that labels $\hat{x}_j = \lim_{M\to\infty} \frac{1}{M}\sum_{i=1}^{M} x_{i,j}$. Based on that, a clearer representation of the total noise is

$$\begin{aligned} v_{tot}^2 &= \frac{1}{N}\sum_{j=1}^{N}\left(\bar{x}_j - s_j\right)^2 = \frac{1}{N}\sum_{j=1}^{N}\left(\bar{x}_j - \hat{x}_j + \hat{x}_j - s_j\right)^2 \\ &= E\left\{\left(\bar{x}_j - \hat{x}_j\right)^2\right\} + E\left\{\left(\hat{x}_j - s_j\right)^2\right\} \\ &= var[\bar{n}] + E\left\{e_j^2\right\}, \end{aligned} \tag{11}$$

where $var[\bar{n}]$ represents the residual Gaussian noise, and $E\left\{e_j^2\right\}$ denotes the dynamic quantization noise with thermal noise. Based on the analysis in [25], [26], the term of $E\left\{e_j^2\right\}$ has an evaluation of the deviation factor (DF)

$$DF = E\left\{e_j^2\right\} = \frac{1}{q}\int_0^q \left(e_{j|s}\right)^2 p(s)ds. \tag{12}$$

For the full-scale signal, $q = 1/2^N \cdot V_{ref}$ is sufficiently small. Expanding on this condition, s varies linearly over any quantization interval, i.e. s is uniform distribution. Thus, $e_{j|s}$ can be derived from the Fourier series [25],

$$e_{j|s} = \sum_{k=1}^{\infty} \frac{(-1)^{k+1}q}{\pi k} \exp(-2\pi^2 k^2 (\frac{\sigma}{q})^2) \sin(\frac{2\pi ks}{q}), \tag{13}$$

where σ is RMS of thermal noise. Note that its higher order terms are less than 1% of the first two terms as soon as $\sigma/q > 1/6$. In this case, a closed-form equation with approximation is given by

$$\begin{aligned} e_{j|s} = \frac{q}{\pi} &\exp(-2\pi^2(\frac{\sigma}{q})^2)\sin(\frac{2\pi s}{q}) \\ &\times[1 - \exp(-6\pi^2(\frac{\sigma}{q})^2)\cos(\frac{2\pi s}{q})] \end{aligned} \tag{14}$$

Substituting (14) into (12), DF is given as a function of σ

$$DF(\sigma) = \frac{q^2}{2\pi^2}\exp(-4\pi^4(\frac{\sigma}{q})^4) + \frac{q^2}{32\pi^2}\exp(-40\pi^4(\frac{\sigma}{q})^4). \tag{15}$$

According to [27], the effective number of bits is defined as

$$b_e = b + \frac{1}{2}\log_2\frac{q^2/12}{v_{tot}^2(\sigma, M)}, \tag{16}$$

where b_e is ENOB that can be achieved, and the excess bit of ENOB (EBOB) can be derived as $b_{ex} = b_e - b$. When $v_{tot}^2(\sigma, M) < q^2/12$, M-channel TSADC improves ENOB. Based on the quantization theory, b_{ex} can be derived by (12) and (13) as

$$b_{ex} = \frac{1}{2}\log_2\frac{q^2/12}{\text{var}[\bar{n}] + DF(\sigma)}. \tag{17}$$

When $M = 1$, as reported in [28], total noise is independent of the dither noise and $v_{tot}^2 = q^2/12 + \sigma^2$, and the excess bit is $b_{ex} = \frac{1}{2}\log_2\frac{q^2/12}{q^2/12+\sigma^2} < 0$. In this case, b_{ex} decreases monotonically with the increasing σ.

Further discussions about (17) for $M \geq 2$are expanded as the following.

- ***Discussion 1:*** When $0 < \sigma/q < 1/6$, it depicts that the system is in extreme low thermal noise and the input signal between channels are strongly correlated. Such case has been discussed previously in (8), and $\text{var}[\bar{n}] \approx 0$ in (11). Then the quantization noise has an averaged power of $DF(\sigma) \approx q^2/12$, i.e. $v_{tot}^2(\sigma, M) \approx q^2/12$, which will lead to an unwanted result $b_{ex} = 0$. Therefore, TSADC has no improvement for ENOB in this case. In order to break through this limitation,

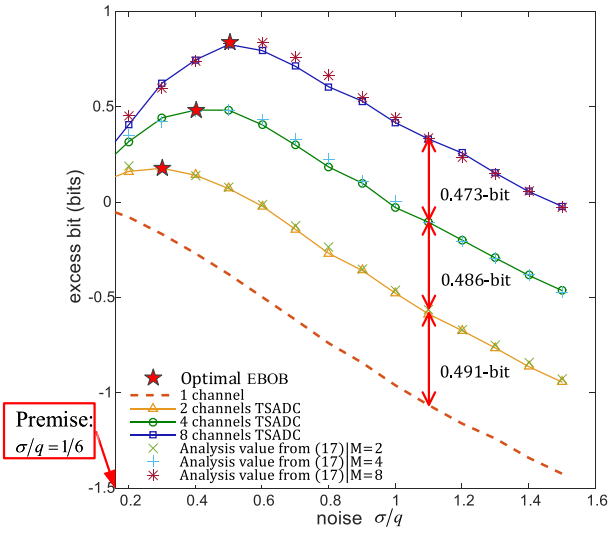


FIGURE 5. Numerical result of EBOB in the theory and simulation based on TSADC structure.

a decorrelated technique can be considered that adds more Gaussian noise to the signal before sampling [25], which ispopularly used in the design of high performance ADC [29].

• ***Discussion 2:*** When $\sigma/q > 1/6$, b_{ex} is not monotonic with the increase of σ, but it exists a maximum. To obtain the maximum b_{ex}, the optimal solution σ_{opt} needs to satisfy

$$\frac{\partial}{\partial\sigma}\left(\frac{q^2/12}{\text{var}[\bar{n}]+DF(\sigma)}\right)\Big|_{\sigma=\sigma_{opt}}=0. \tag{18}$$

Although the exact value of σ_{opt} is difficult to solve by a closed-form equation, b_{ex} increases with the increase of σ when $1/6 < \sigma/q < \sigma_{opt}$. This conclusion is proven through the numerical simulation.

To simplify the simulation, it is assumed that only uncorrelated noise exists. The relevant configuration parameters are introduced as follows: the original ADC resolution is $b = 8$; then, we set $M = 1, 2, 4, 8$ respectively and let σ/q increase with a minor step 0.1 in one curve. Different EBOB curves in (17) are plotted in **FIGURE 5** for different M associated with σ/q, which are represented by different symbols '$\times$', '$+$' and '$*$' in terms of $M = 2, 4, 8$ respectively. From this figure, the theoretical analysis almost coincides with the simulated results and the optimal EBOB is marked by a star '★'. For each curve, EBOB increases with the noise increasing in the range of $1/6 < \sigma/q < \sigma_{opt}$.

• ***Discussion 3:*** When $\sigma/q > \sigma_{opt}$, b_{ex} is steadily decreasing with the increase of noise. In this case, the relationship of $\lim_{\sigma\to\infty} DF(\sigma) = 0$ is established according to (15). The input signals among different channels are fully uncorrelated, and the variance of thermal noise is reduced by a factor M through M channel average, that is $\text{var}[\bar{n}] = \text{var}[n]/M$. This can be identified similarly as the sum of M ADC outputs reduces the variance of thermal noise by an only factor of M, that gives

$$b_{ex}=\frac{1}{2}\log_2\left(M\cdot\frac{q^2}{12\sigma^2}\right), \tag{19}$$

From the simulation result of **FIGURE 5**, it can be seen that the quantization for large noise $\sigma \geq \sigma_{opt}$ is no longer dominant effectivity compared to the effect of the noise itself. Moreover, EBOB decreases as the increasing of noise, but the EBOB difference between the curves of twice M is 0.48-bit approximatively.

In this section, a more general analysis of TSADC theory was made in terms of resolution enhancement and its effective premise, which is the fundamental theory of high-resolution sampling as well as expandable sampling applications featuring multi-resolution.

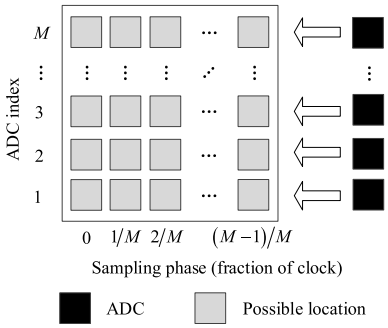


FIGURE 6. The general arrangement diagram of multi-compnent locations for multi-resolution UF-DAQ applications.

III. MULTI-RESOLUTION SAMPLING SOLUTION

In terms of the above renewal analysis, a TSADC structure can improve single ADC resolution definitely by the way of parallelized synchronization sampling. However, a sampling system with multiple ADCs has not yet to reach its maximum hardware value. If sampling clocks of these ADCs could be switched into a suitable phase interval, this system will achieve a higher sampling rate by the way of time-interleaved sampling. Therefore, in order to give full play to hardware value, it is of great significance to realize a multi-resolution capability in a same sampling system for different applications as well as energy saving. In this section, we will take full advantage of the respective strengths of TIADC and TSADC, and propose a novel multi-resolution sampling solution in the same hardware system by the way of configurable ADC arrangement.

For an UF-DAQ application, the arrangement of parallel ADCs can be illustrated with a conceptual scheme of an $M \times M$ array, as shown in **FIGURE 6**. M black-squares in the right column represent M ADCs. The vertical axis is the index of ADCs, and the horizontal axis is their clock phases, where any component could be placed at any grey-square in a row.

For a DAS composed of four 5GSPS/8-bit ADCs, there are three possible arranging schemes for the purpose of different resolutions.

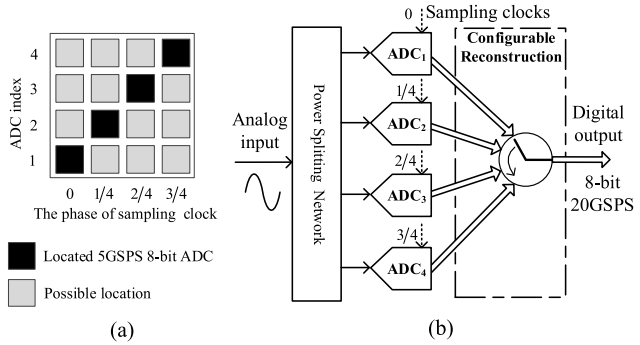


FIGURE 7. The time-interleaved scheme of highest sampling rate with four 5GSPS ADCs: (a) 20GSPS 8-bit arrangement topology, (b) its system diagram.

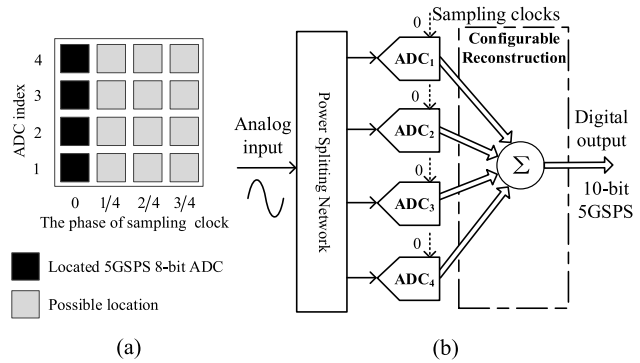


FIGURE 8. The time-synchronized scheme of highest resolution with four 5GSPS ADCs: (a) 5GSPS 10-bit deployment topology, (b) its system diagram.

Scheme 1: The highest sampling rate based on a conventional four-channel TIADC structure is shown in **FIGURE 7 (a)**, and its system scheme diagram is shown in FIGURE 7. **(b)**. The sampling clock distributed to ADC_1 is an initial phase and the increasing offset phase of 1/4cycle is set for ADC_2, ADC_3 and ADC_4 respectively. An analog input signal is digitized in time-interleaved manner by four ADCs, whose outputs are then multiplexed by the digital multiplexer to combine a final output with total sampling rate of 20GSPS and 8-bit resolution.

Scheme 2: The highest resolution arrangement based on TSADC structure is introduced into a configurable sampling system, as shown in **FIGURE 8**. All ADCs are deployed in the same phase and work with same sampling clock. **FIGURE 8(a)** depicts the topology of four 5GSPS 8-bit ADCs which can achieve a DAS with 5GSPS 10-bit, and its system block diagram is shown in **FIGURE 8(b)**. Then, the digitized outputs from the parallel channels are summed by a digital adder in configurable reconstruction module.

Scheme 3: A novel hybrid arrangement based on a combined structure of TIADC and TSADC is proposed for the trade-off consideration of high-speed and high-resolution. By taking an example for four ADCs shown in **FIGURE 9**, four ADCs are divided into two groups. ADCs in the same group work in two-channel time-synchronized manner, and different groups work in time-interleaved manner. The input

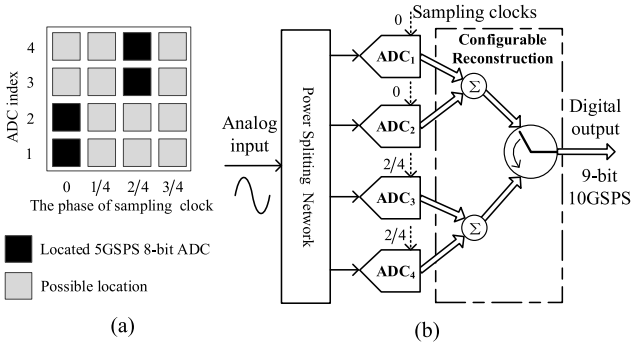


FIGURE 9. The novel hybrid scheme of trade-off performance with four 5GSPS ADCs: (a) 10GSPS 9-bit deployment topology, (b) its system scheme.

signal is digitized by the phase types $[0, 0, 1/2, 1/2]$ for each sampling clock of ADC. The digitized outputs from two parallel TS-channels are summed in first by the digital adder. Finally, the data of two TI-channels are merged into one stream by the configurable multiplexer.

The core of these arrangements contains two configurable modules: a generator of sampling clocks featuring adjustable phases, and a digital configurable reconstruction engine that is composed of multiplexers and adders. Through this solution, there are three resolutions of 8-bit, 9-bit and 10-bit that can be implemented in a same UF-DAS by three reconfigurable arrangements.

IV. IMPLEMENTATION AND VERIFICATION

In this section, the implementation details will be expounded for the multi-resolution UF-DAQ application that has been proposed in section III. Finally, three experiments will be performed on this platform to verify the feasibility of TSADC and its multi-resolution application.

A. PROTOTYPE IMPLEMENTATION

In order to test the performance of the proposed idea, a multi-resolution prototype is designed and implemented. Its material diagram is shown in **FIGURE 10: 1)** A conditioning channel module with low-pass filter, amplifiers; 2) a *power splitting network*; 3) Two *acquisition boards* comprised of four 5GSPS/8-bit ADCs and four field-programmable-gate-arrays (FPGAs); 4) A *processing board* comprised of one synthetical FPGA and a configurable sampling clock generator.

The input signal is split into four same channels by the power splitting network and fed into four ADCs. The reason of using four FPGAs in acquisition boards instead of one FPGA is the balance consideration of resources and cost performance. The core function of multi-resolution switching is performed by a phase-lock-loop (PLL) in clock generator and channel-select registers in ADC. Through the controlling bus, parallel sampled data are sent to the processing board for reconstruction. The waveform reconstruction module has been implemented in the FPGAx, in which other real-time digital signal processing algorithms can be realized. At the same time, the sampled data from multiple buffers is

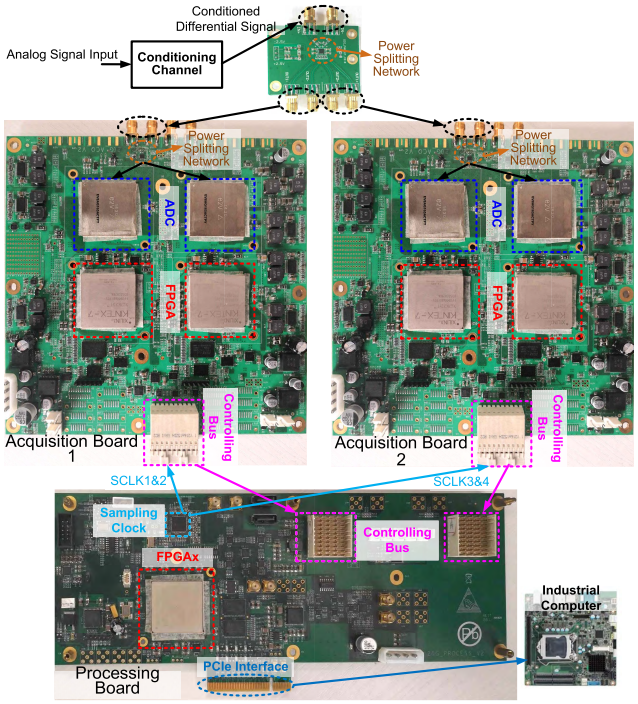


FIGURE 10. The material diagram of multi-resolution UF-DAQ prototype with four-channel hybrid sampling structure.

transferred through a PCIe interface to industrial computer for further data processing.

To find the sampling clock jitter requirements of the proposed system, a theoretical relationship between SNR and the jitter should be abided on the engineering by

$$t_{jitter_{rms}} = [10^{(SNR/20)}(2\pi f_{\text{analog}})]^{-1}. \tag{20}$$

According to the data sheet of EV8AQ165A, the SNR of the known ADC is over 42dB and the maximum bandwidth is 3.2GHz@-3dB. Therefore, if the input frequency f_{analog} of analog sinewave is set to 3.2 GHz, the maximum of sampling clock jitter $t_{jitter_{rms}}$ should be lower than 390*fs*, and can be less than 180*fs* in the actual test of designed prototype.

Before the verification of proposed theory and scheme, the parallel mismatch error among multiple channels should be calibrated firstly. Based on that, the overall workflow of three resolution modes in the system is explained as follows. When the system works in 8-bit mode, PLL is configured in four-channel time-interleaved manner to generate four sampling clocks with the phases of $\varphi = [0, \pi/2, \pi, 3\pi/2]$. As the mode changing to 9-bit, the PLL is reconfigured and generates sampling clocks with the phases of $\varphi = [0, 0, \pi, \pi]$. When the operation is switched to 10-bit mode, sampling array is configured to time-synchronized manner with four clocks of same phase.

B. TEST PLATFORM AND NOISE MEASUREMENT

Experimental verification is fully performed and analyzed on the test platform shown in **FIGURE 11**, which is comprised of the proposed prototype, signal generator and arbitrary

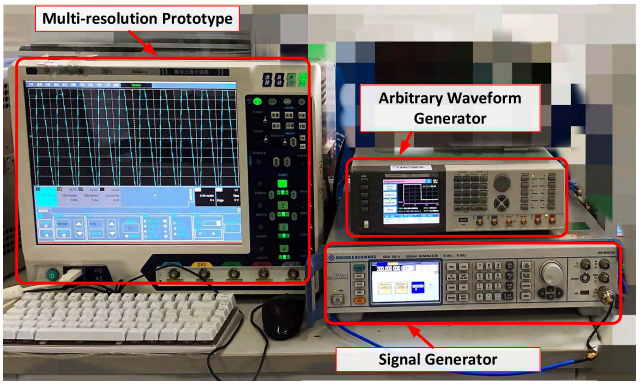


FIGURE 11. The test platform of multi-resolution UF-DAQ prototype.

waveform generator (AWG). Signal generator generates standard RF signal and AWG is used to generate complicated signals expediently. Both of these instruments are necessary. The big box in left is the designed multi-resolution prototype, where the configuration can be operated on the panel or peripherals.

First, the noise level of prototype itself should be tested that is denoted as σ/q in (8). Here, a classical thermal noise measurement method of the histograms measurement in reference. [23] can be employed for the evaluation of the RMS value of thermal noise in our system, because it is an effective method to avoid the interference of quantization noise and alternating-current noise. The core idea is to evaluate standard deviation σ of Gaussian noise by measuring the probability of output codes with a clean DC signal input.

Because a symmetric ordinary norm-distribution $X \sim N(0, \sigma^2)$ can be converted to a standard form $X/\sigma \sim N(0, 1)$, the same area of shaded tails requires that the integration limit should meet $x_s = x_o/\sigma$, where x_s, x_o is corresponding to the integration limit of standard form and ordinary form. Based on this relationship, the brief operation procedure is described as following.

- ***Step 1&2:*** Collect statistical data with the histogram. First, connect a DC signal to the analog input; then, save the conversion data and get the statistics histogram of digital code frequency. For example, the occurring probability of main code is denoted as P_{MC}, and the one side frequency of sidelobe codes that occur outside of the main code is denoted its probability as P_{SC}. That is $P_{SC} = (1 - P_{MC})/2$.
- ***Step 3:*** Find the limit of integration x_0 corresponding to the value of P_{SC} from the cumulative distribution function (CDF) F_{CD} of the standard norm-distribution with σ equal to unity:

$$F_{CD} = \frac{2}{\sigma\sqrt{2\pi}} \int_{-\infty}^{x} e^{-z^2/(2\sigma^2)} dz, \tag{21}$$

- ***Step 4:*** Solve for the RMS value σ of thermal noise determined from

$$\sigma = -0.5q/x_0, \tag{22}$$

The measurement procedure in our system is illustrated in **FIGURE 12**. The result shows that $\sigma/q = 0.3764$ in the prototype, which satisfies the premise of TSADC, $\sigma/q > 1/6$. Certainly, if the evaluation value of noise is so low that does not meet the applicable premise, there are additional techniques that could be applied to build a reliable, robust sampling system, such as dithering and different input offsets.

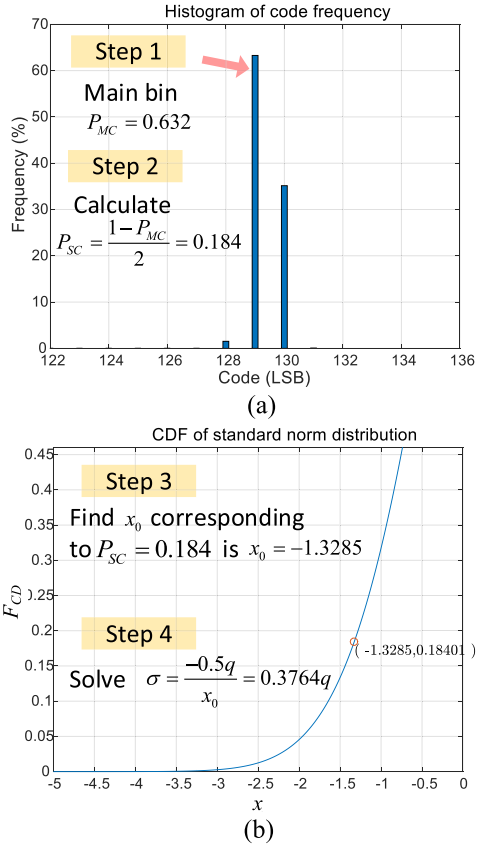


FIGURE 12. Experimental results of noise evaluation: (a) the histogram of digital code frequency and the instance of step 1&2; (b) the curve of CDF of standard norm-distribution and the instance of solving the RMS value of thermal noise at the step 3&4.

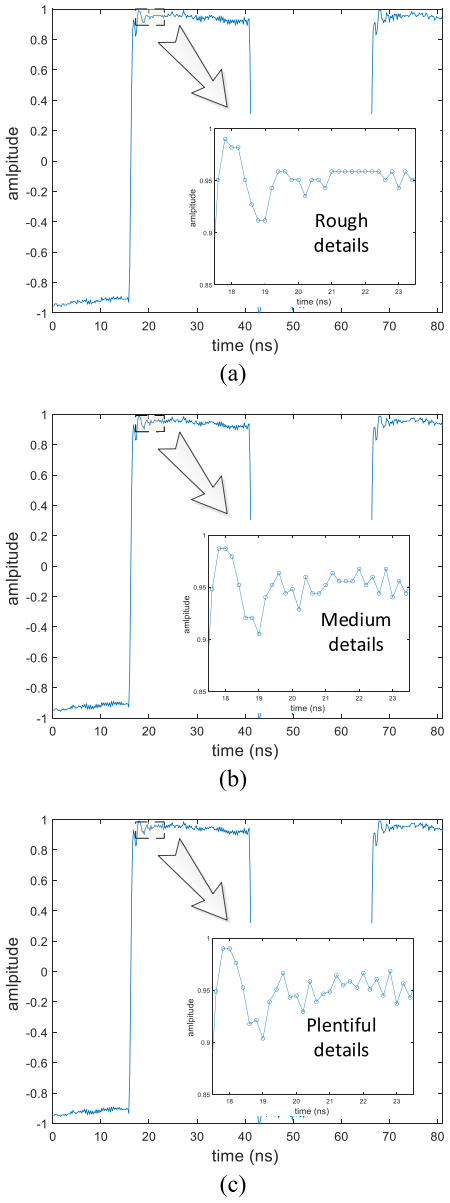
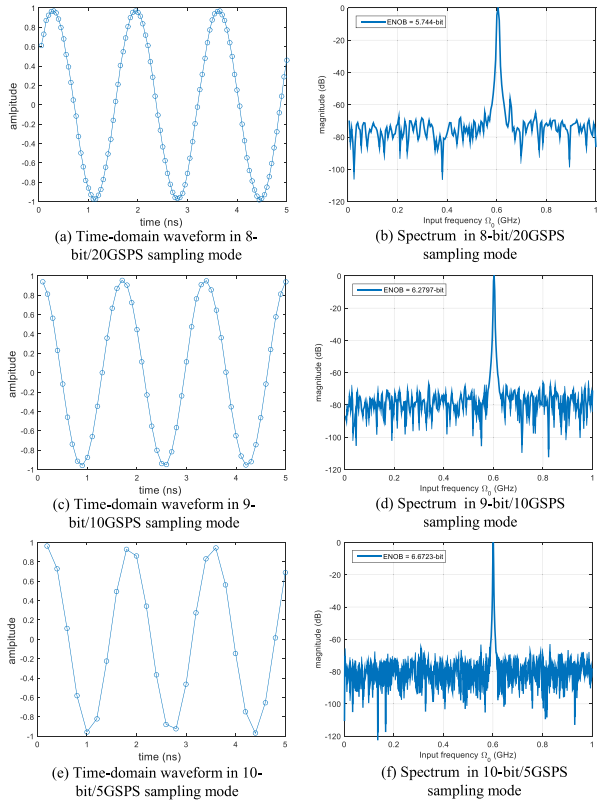


FIGURE 13. Time-domain waveforms of 20MHz square signal by (a) 8-bit (b) 9-bit and (c)10-bit sampling modes. The inside window is the zoomed view of waveform.

C. WAVEFORM TEST AND PERFORMANCE ANALYSIS

The result of noise measurement shows that the prototype meets the applicable premise of TSADC resolution enhancement, so we can evaluate its system performance further for the theoretical verification by three experiments in time-domain and frequency-domain.

The first experiment is aimed to reveal the visualized effect of resolution enhancement of TSADC system by testing the time-domain waveform with multiple resolutions. In this experiment, we select a square waveform with a frequency of 20MHz. To fully display the difference of multiple resolutions, the sampling rate is set to 5GSPS for all acquisition modes. **FIGURE 13** shows three sampled waveforms that are digitized with the resolutions of 8-bit, 9-bit and 10-bit respectively. To achieve a more precise observation, the same part in each waveform is observed by a zoomed window where the waveform details and the quantized steps can be illustrated more clearly. It can be seen from **FIGURE 13(a)** that the detail of original signal is hardly observed by 8-bit sampling mode. This is because the big quantized step of 8-bit ADC cannot capture the slight variations of original signal. In **FIGURE 13(b)**, the signal detail that is acquired by 9-bit sampling mode appears more plentifully but the quantized step is still rough obviously. Compared with the 8-bit and 9-bit sampling mode, it can be seen that the waveform in 10-bit mode is the cleanest and closest to the real signal. These results indicate that high resolution implemented by TSADC has an intuitive effect from the time domain observation. With the increase of resolution, more waveform details



(a) Time-domain waveform in 8-bit/20GSPS sampling mode
(b) Spectrum in 8-bit/20GSPS sampling mode
(c) Time-domain waveform in 9-bit/10GSPS sampling mode
(d) Spectrum in 9-bit/10GSPS sampling mode
(e) Time-domain waveform in 10-bit/5GSPS sampling mode
(f) Spectrum in 10-bit/5GSPS sampling mode

FIGURE 14. Time- and frequency-domain results of the prototype at different sampling modes with 600MHz sinusoidal signal input.

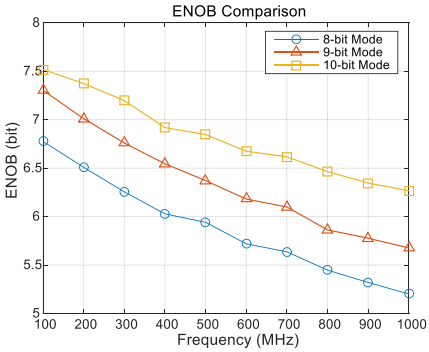


FIGURE 15. ENOB curves with different input frequencies and in different resolution modes.

can be presented, and then the acquisition effect is closer to the real signal.

The second experiment tests the actual behavior of the prototype in both time-domain and frequency-domain, shown in **FIGURE 14**. In this experiment, we select a signal with relative low frequency in order to fully display the visible details of digitized signal, so a 600MHz full-scale sinusoidal signal is employed. **FIGURE 14(a)(c)(e)** are the time-domain waveforms digitized in 8-bit/20GSPS, 9-bit/10GSPS and 10-bit/5GSPS sampling modes respectively. Additionally, their corresponding spectrograms are shown in **FIGURE 14(b)(d)(f)**. The digital output is fed to the computer for spectrum analysis by using 8192-point Fast-Fourier-Transform (FFT). From top to bottom in **FIGURE 14**, it is obvious that the sampling rate is decreasing with the increase of resolution. The spectrograms show that the noise floor of 8-bit resolution is higher than −80dB and reflects the system ENOB of 5.74-bit. The ENOBs of 9-bit and 10-bit resolutions are 6.27-bit and 6.67-bit. This performance means an 8-bit/20GSPS sampling system can achieve a resolution enhancement of 0.93-bit if it works in 10-bit mode. When the requirement of resolution is not high but sampling rate higher, the system can be switched into 8-bit and 9-bit sampling modes. Therefore, thanks to the hybrid reconfigurable design of TSADC and TIADC, the proposed system can be flexibly configured between high sampling rate and high resolution.

In the third experiment, the dynamic performance is verified at different frequencies in the range of 1GHz. **FIGURE 15** depicts the comparison of multiple resolutions. The setup uses a set of sinusoidal signals with single frequency from 100MHz to 1GHz. Using the same calculation process, the ENOBs are obtained at different frequencies and then plotted as the curve of ENOB versus frequency. By horizontal comparison, we can know that the ENOB decreases with the increase of frequency. This performance degradation is due to the jitter of sampling clock, increased distortion and nonlinearities. Through the vertical comparison, it can be seen that the highest ENOB is 7.5-bit@100MHz in 10-bit mode, whose enhancement is 0.2-bit higher than 9-bit mode and 0.75-bit higher than 8-bit mode at the same frequency. In the other frequencies, the ENOB enhancement of 10-bit mode is nearly 0.5-bit higher than the 9-bit mode. The same result happens in the 9-bit and 8-bit mode. Therefore, these experiment results are consistent with simulation result and they both manifest the theoretical correctness of (19). It is concluded that the experiment verifies the effectiveness of ENOB enhancement in different resolution modes.

From these three experiments, we not only confirm the RMS value of thermal noise in the prototype meets the applicable premise, but also verify the effectiveness of resolution enhancement in time- and frequency-domain. Meanwhile, the ENOB curve in different resolution modes tested in the prototype gives a practical guide for the multi-resolution sampling application. Furthermore, the characteristics of static and dynamic non-linearity revealed by INL/DNL and SFDR indexes is also evaluated for the prototype in terms of the analysis method of [30]. The testing results show that the non-linearity indexes are close to the level of selected ADC itself and have little effect on the ENOB evaluation.

In addition, compared to traditional single-resolution sampling system, the proposed multi-resolution system has achieved the sampling result of three resolutions in the same system only by the switching of sampling clocks' phase and

mismatch calibration method. The phase relationship and calibration method in each resolution mode are the same as the single-resolution sampling system, and depends only on the sampling technology itself. That is to say, they have the same kind and amount of employed components at the sampling mode of same single technique and the only difference is that it can switch among multiple sampling modes. Therefore, the power consumption of proposed technique between different resolution modes is almost the same, and also similar to that of single-resolution sampling system.

V. CONCLUSION

This paper presents a circuit-level reconfigurable method for multi-resolution real-time sampling applications. The mechanism of TSADC resolution enhancement is first studied fundamentally from three aspects of vertical resolution, the applicable premise and ENOB. Then three deployment strategies with the hybrid structure of TIADC and TSADC are designed for a multi-ADC system that can work in different resolution modes by a variety of specific hardware reconfigurations. Simulation results show that the enhancement effect of quantizing resolution and ENOB is remarkably consistent with the proposed theory. In addition, a maximal 20GSPS prototype with multi-resolution (8, 9, 10-bit) is built to verify the effectiveness of theoretical analysis. Experimental data sourced from this prototype show that the actual vertical resolutions of 8, 9, 10-bit have been realized by different arrangement schemes of four 8-bit ADCs. Compared with traditional DASs, the proposed reconfigurable multi-resolution DAS could achieve a different-resolution acquisition goal in the same hardware platform by an optimization of hardware resource. Besides, it also provides a novel design idea for ultra-fast DAS as well as ADC integrated-circuit, which need the trade-off sampling requirement of accuracy and speed.

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