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Analog-to-Digital Converters

A review of the past, present, and future

This article discusses current commercially available analog-to-digital converter (ADC) technology, analyzes its key performance parameters, reviews its historical trends over the past two decades, and postulates future ADC capabilities. Based on an extensive data set including nearly 1,000 commercial products released over the past 20 years, our results show new trends compared to the well-known ADC survey by Walden [1]. It is also shown that advanced semiconductor technologies and emerging communication applications are strongly influencing the future of ADCs.

ADCs play an important role in almost all application fields, which makes it important to review the technology trends every few years. The communications industry has consistently pushed the boundaries of ADCs, and current advances in ultra-wideband (UWB) and software defined radios (SDRs) continue the trend. Today, sensor technologies are becoming increasingly popular and are another area where ADCs play a major part. Here, we analyze ADCs with a general overview suitable for any area of need and present general technology trends apart from technology-specific areas.

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Understanding the trends in ADC performance is the key for designers to predict the evolution of future communication systems, especially SDR technology [2]. Walden produced perhaps the best overview for understanding ADC performance trends in his well-known paper from 1999 [1]. However, Walden's ADC survey was published just prior to a large performance leap in ADC technology, which the literature over the past six years does not reflect, and thus a new survey with up-to-date ADC database is needed. We have collected a comprehensive sample set of commercial ADCs from the past two decades to advance upon Walden's work and extend understanding of the performance trends of ADCs. First, we look into key performance parameters of ADCs such as resolution (number of bits), sampling rate, and distortion; then, we extract their historical trends with relationship to power dissipation. We also show the performance dependency on ADC architectures and ADC trends exhibited over the years.

The ADC process consists of two steps, sample-and-hold (S/H) operation followed by digital quantization. ADC performance is mainly limited by noise introduced by the S/H circuit and signal distortion due to quantization. In the literature, a set of parameters are defined to quantify ADC performance, e.g., signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) [2]. It is a common practice to measure the effective resolution of an ADC as the effective number of bits (ENOB) to evaluate its performance against noise and distortion based on an equivalent ideal ADC. The effective resolution is a result of the degradation in the stated resolution (the nominal number of bits listed in the product datasheets) resulting from both noise and distortion. Therefore, the effective resolution is a better performance indicator for ADCs.

In the analysis of ADCs, two figures-of-merit P and F are widely used, which are defined as

$$P = 2^B \cdot f_s \tag{1}$$

$$F = \frac{2^B \cdot f_s}{P_{\text{diss}}}. \tag{2}$$

Here, B is the ENOB (also known as SNR b), f_s is the sampling rate, and P_{diss} is the power dissipation. P is a figure-of-merit for evaluating the combined performance of resolution and speed, and F is a figure-of-merit for evaluating the power efficiency with resolution and speed.

Walden's paper derives the equations of ADC performance limitations due to thermal noise, aperture jitter, and comparator ambiguity. It focuses on the ADC resolution versus the sampling rate where the resolution is either SFDR or SNR [what we refer to as the signal-to-noise-plus-distortion ratio (SNDR) in the performance analysis]. Walden's analysis concentrates more on SNR than SFDR due to the inclusion of noise and error in ADC operation.

Walden concludes that F has been increasing over time while P has remained relatively steady. His explanation for this trend is that F has been growing due to the reduction in power dissipation as ADC designs become more monolithic and power efficient, while the resolution and sampling rate are remaining relatively constant. His comments on P and F are unfortunately not applicable to ADC technologies developed since 1997 when his data ends. Furthermore, Walden gives minimal analysis of ADC architectures like flash, pipelined, sigma-delta, and folding. Again, to build upon this starting point, we show with our data that power dissipation has a first-order relationship to the ADC structure.

Another interesting ADC survey, published in 2003 by Merkel and Wilson [3], discusses the selection requirements for high-speed ADCs for military applications. The authors give a detailed analysis of 150 ADCs chosen from both commercial and research sources, but because they are specifically interested in military applications, they only analyzed ADCs of 12 b or higher resolution and sampling rates greater than 1 Ms/s. The insight on their paper comes from their comparison among competing manufacturers, substrate processes, and architectures, which is an extension of Walden's work. Merkel's is still a limited survey, however, as they only have the high-performance needs of the military in mind, and so their ADC analysis lacks the generality develop here.

We look at a much wider selection of commercially available ADCs, analyzing key ADC parameters and looking into technology trends. Our data comes solely from commercially available ADCs, and we focus on four major IC manufacturers: Analog Devices, Maxim, National Semiconductor, and Texas Instruments. In total, we have collected information on 914 ADCs that are market available with manufacturing dates as far back as 1983. The collected information for each ADC includes the stated bits, sampling rate, power dissipation, SFDR, SNDR, architecture, substrate technology, number of ADC channels per packaged unit, price, and manufacturing date. All data comes from the manufacturer's Web sites and data sheets. Not all parameters are available for some ADCs, such as the architecture, which we label as an unknown structure. In the following analyses and plots, we include all the ADCs with the relevant parameters, and we ignore any devices for which such information is lacking.

PERFORMANCE ANALYSIS

For all types of ADCs, there are three universal performance parameters: sampling rate, resolution, and power dissipation. Their combinations form two widely used figures-of-merit, P and F [(1) and (2)]. We first compare commercial ADC performance limitations to test the hypothetical prediction. Then we look into the trends seen in sampling rate with resolution and discuss the source of distortions. We follow this by looking at how ADCs depend on power dissipation.

SAMPLING RATE VERSUS NUMBER OF BITS

Figure 1 shows a performance overview in terms of stated number of bits versus sampling rate plotted with the complete sample set. It is obvious that ADCs are grouped by structure and each ADC structure dominates a specific application area with certain resolution and sampling rate. There are seven types of structures for the ADC sample set: flash, half-flash, folding, successive approximation register (SAR), pipelined, sigma-delta, and unknown. Reed [2] gives a detailed description of all these structures.

The pipelined structure and unknown structure have the best overall performance, so that they are best suited for applications with high performance requirements, such as wireless transceiver applications and military use [3]. SAR ADCs have widely ranging sampling rates, though they are not the fastest devices. Still, these devices are popular for their range of speeds and resolutions as well as low cost and power dissipation. It can be seen that there is a borderline of sampling rate at around 30 Ms/s separating the sigma-delta and flash ADCs. Sigma-delta ADCs have the highest resolution with relatively low sampling rates from kilosamples per second to megasamples per second, while flash ADCs have the highest sampling rates up to Gsps due to their parallel structure but with a resolution limited to no more than 8 b due to nonlinearity. Between these two structures are unknown structures compromising speed and resolution.

We are also interested in the envelope of the sample distributions in this plot since such an envelope indicates the performance limitations. It is reasonable to extract the envelope information based on the ADCs with the highest performance to postulate the design challenges and technology trends.

In Figure 1, if Walden's claim that P is relatively constant is true, according to (1), the envelope line should show that a 3 dBs/s increment in f_s corresponds to a 1-b reduction in resolution. However, Figure 1 shows that the real tradeoff is 1 b/2.3 dBs/s. Compared to the 1 b/3 dBs/s slope hypothesis, there is an improvement in P at low sampling rates and degradation at high sampling rates. This trend indicates that the ADC performance boundary is varying with sampling rate, as illustrated by Figure 2 where ENOB is plotted versus the sampling rate.

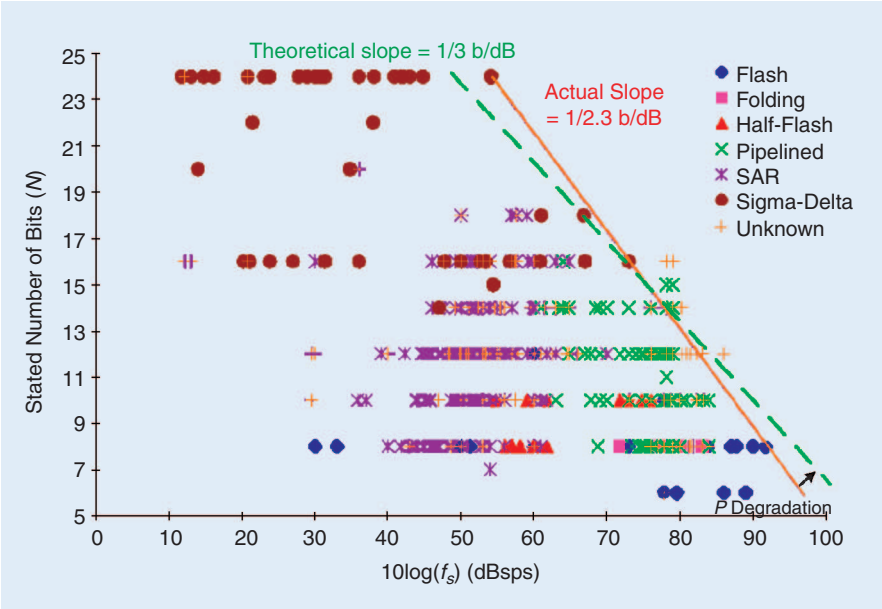
As stated previously, noise and distortion cause most of the performance degradation in practical ADCs. The internal sample-hold-quantize signal operations are nonlinear, and those effects are represented as equivalent noise effects so that they can be unified into noise-based equations to simplify the performance analysis. Therefore, besides thermal noise, we have two additional noise sources, quantization noise [2] and aperture-jitter noise [1].

THERMAL NOISE

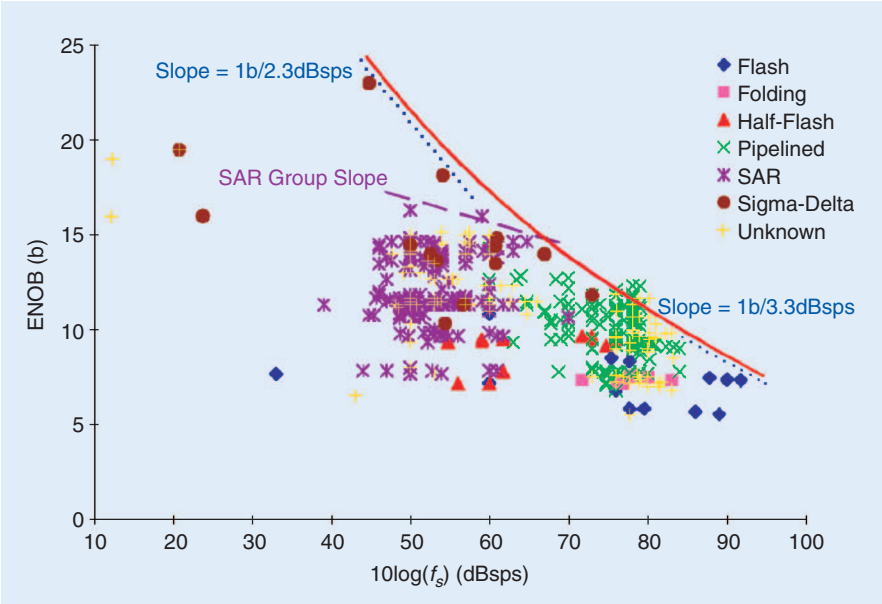
Thermal noise by itself [1] has a 1 b/6 dBs/s relationship to sampling frequency assuming Nyquist sampling [2]. However, it is usually overwhelmed by the capacitance noise since the S/H stage, as the input stage of an ADC, shows strong capacitive characteristics. Therefore, the capacitance noise (modeled as kT/C noise [4], where k is Boltzmann's constant, T is the temperature, and C is the capacitance) is usually assumed as the input noise floor.

QUANTIZATION NOISE

The signal distortion in quantization is modeled as quantization noise with a signal-to-quantization-noise ratio (SQNR) definition of



[FIG1] **Stated number of bits versus sampling rate.**



[FIG2] **ENOB versus sampling rate.**

$$\mathrm{SQNR} = 6.02B + 4.77 - 10\log_{10}\eta\,\mathrm{dB}, \tag{3}$$

where η is the signal's peak-to-average-power ratio [2] and B is the ENOB corresponding to SQNR. For sinusoidal signals, $\eta = 2$, thus $\mathrm{SQNR} = 6.02B + 1.763$ dB. This definition of SQNR by (3) assumes

- samples of input signal are random, zero-mean, and uniformly distributed across quantization levels over the full-scale range (FSR) of the ADC, i.e., the quantization error is uniform over $[-\Delta/2, +\Delta/2]$, where Δ is the distance between two nearest quantization voltage levels
- the input signal loads the quantizer without clipping, i.e., the peak signal amplitude does not exceed FSR, $V_{FS}/2$.

FOR ALL TYPES OF ADCs, THERE ARE THREE UNIVERSAL PERFORMANCE PARAMETERS: SAMPLING RATE, RESOLUTION, AND POWER DISSIPATION.

APERTURE JITTER NOISE

Practical ADC sampling times are generated from an external clock. Due to clock accuracy limitations and S/H circuit imperfection, some variation in the clock timing is unavoidable. Although the average value of the intervals between clock pulses is constant, the instantaneous spacing between samples varies. This sample-to-sample uncertainty, called aperture jitter, will cause uncertainty in the timing of sampler signal, degrade the ADC's noise floor, and increase the possibility of inter-symbol-interference (ISI). Aperture jitter is directly proportional to the input signal's slew rate depending on both frequency and amplitude. Usually, the input signal's amplitude swing is clamped by an automatic gain control (AGC) circuit to ensure FSR utilization. The input signal's frequency and the ADC's resolution determines the maximal aperture jitter by

$$\tau_a = \frac{1}{2^N \cdot \pi \cdot f_{\max}}, \tag{4}$$

where τ_a is the aperture jitter [2], $f_{\max}$ is the maximum frequency of the input signal, and N is the stated number of bits (note the difference between N and B, the ENOB). To model the distortion by aperture jitter as another noise source, [5] gives an equation of signal-to-aperture-jitter-noise ratio (SANR) versus sampling rate

$$\mathrm{SANR} = -20\log_{10}(2\pi \cdot f_s \cdot \tau_a)\,\mathrm{dB}, \tag{5}$$

where f_s is the sampling frequency.

To include both noise and distortion effects, SNDR is finally defined to evaluate ADC's performance. SNDR is the sum of all three noise sources and represents the overall effective resolution, which can also be represented as ENOB [2]

$$\mathrm{ENOB} = (\mathrm{SNDR} - 1.763)/6.02. \tag{6}$$

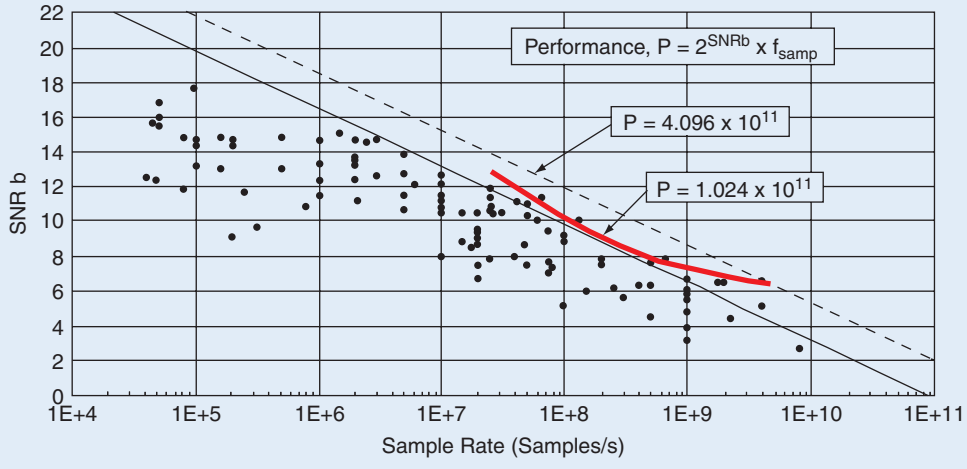
ENOB is a more accurate metric than the stated number of bits when describing an ADC's real resolution. The relation between resolution and signal quality in (6) can be used to calculate an equivalent resolution for a specific effect. Looking at just SANR, we can represent the number of bits, B, as

$$B = -3.322\log_{10} f_s - 3.322\log_{10}\tau_a - 2.945, \tag{7}$$

which has a 1 b/3.322 dBs/s slope for aperture jitter τ_a.

A plot of ENOB versus sampling rate is shown in Figure 2, using the same sample set as in Figure 1. Figure 2 shows several interesting trends.

- Compared to Figure 1, samples are still grouped by structures. However, sigma-delta ADCs, which have the highest resolution, experience the biggest difference between the



[FIG3] **SNR b versus sample rate (reproduced from Walden's work [1]).**

stated number of bits and the ENOB. Within the sigma-delta group, the higher-resolution ADCs have a larger difference between the stated number of bits and the ENOB, which indicates that distortion increases with resolution, and this trend is also valid for all other structures, although the source of such degradation for each one may be different. It is distortion that limits the flash ADCs' resolution from going higher. Many researchers have discussed this problem for flash ADCs in the literature [6], [7], where the number of comparators is proportional to the number of bits, N, as $2^N - 1$, and often one or two additional comparators are used for handling overflow. When the sampling rate increases, the rise in capacitance at the input becomes a critical issue that limits the input frequency and increases the conversion time. The input will act as a high-pass filter, thus high-frequency components of the input signal will be attenuated more than others, which increases distortion.

- In Figure 2, the slope of the performance envelope is decreasing from 1 b/2 dBs/s to 1 b/3.3 dBs/s. A slope of 1 b/2.3 dBs/s with the stated number of bits shown in Figure 1 already reveals an averaged mismatch between practical performance and the hypothetical boundary. Such a mismatch indicates that performance limitation may depend on sampling frequency, i.e., the practical performance envelope is not a straight line with a fixed slope. This is proved clearly by the ENOB plot in Figure 2, since ENOB reflects the real resolution. The reason for this frequency dependency is that the contribution from each noise source is different at different sampling rates. As shown in Figure 2, the combination of thermal and quantization noise dominates at sampling rates less than several tens of megasamples per second, showing a slope similar to Figure 1; after that, the aperture jitter effects start to take over, forcing the envelope's slope toward an asymptote of 1 b/3.3 dBs/s. This trend is very important in predicting ADC performance at different sampling rates and is useful when selecting different types of ADCs for different speed requirements.
- Walden's thermal noise equation [1] has a slope of 1 b/6 dBs/s; thus it seems that the combination of thermal and quantization noise produces a slope less than 1 b/3 dBs/s at low sampling rates. Why is the slope at the lower sample rates in Figure 2 close to 1 b/2.3 dBs/s? The most convincing explanation is that the noise shaping techniques used in sigma-delta ADCs [8] mostly affect the performance envelope at low sampling rates. In contrast, we can see that the performance envelope of the SAR ADC group is much closer to the thermal noise boundary. The results of this trend are due in part because SARs use no noise shaping loop and have capacitance noise at both S/H stages and internal digital-to-analog converters (DACs).
- The sampling-frequency dependency can also be observed in Walden's sample set [1]. One of his plots is reprinted in Figure 3 and shows such slope variation with a corner frequency almost the same as in Figure 2.

A noise-source analysis using closed-form equations can explain the performance boundaries for classic ADC structures such as flash and sigma-delta; however, these equations are difficult to apply to pipelined or unknown ADC structures where noise sources may be more complicated due to internal DACs, buffer stages, and other proprietary blocks. Due to the lack of information from our commercial sample set, it is not possible to explain why pipelined and unknown ADCs have a noticeable performance improvement in Figure 2.

PERFORMANCE VERSUS POWER DISSIPATION

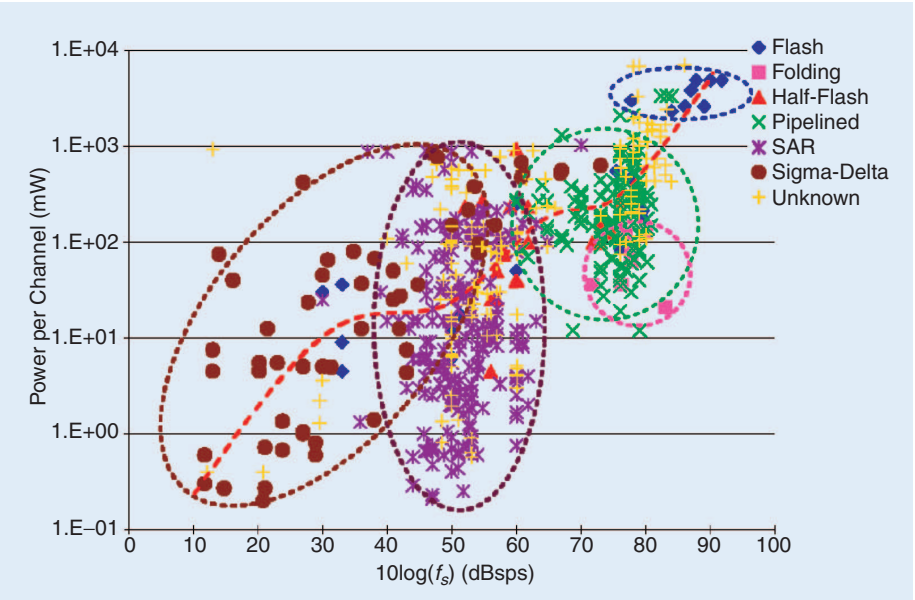
A derivation of power dissipation of an ideal ADC is presented in [9] and based on two assumptions:

- power is consumed only at the S/H block
- the input signal is supplying the power to charge the S/H capacitance.

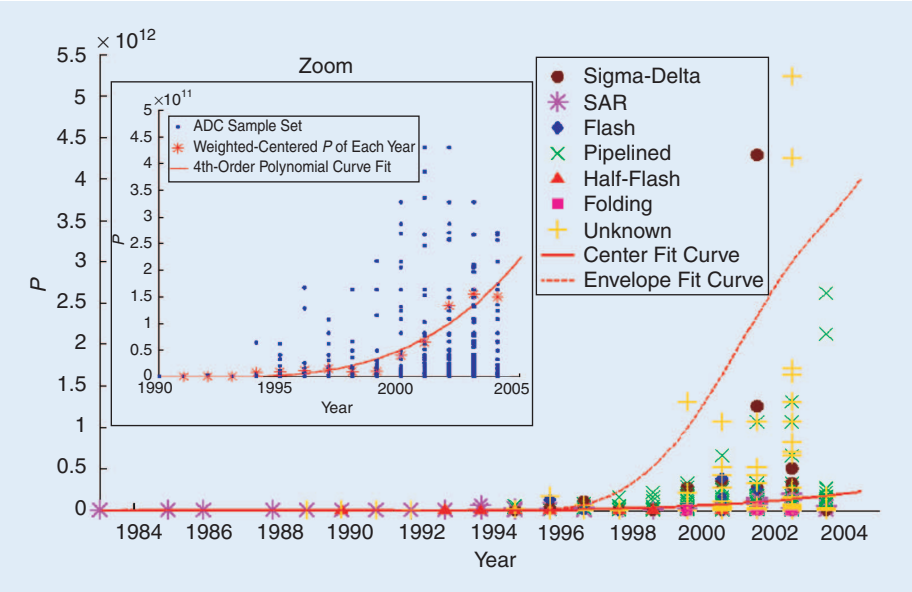
Starting from an intuitive criterion that quantization noise should be no larger than the thermal noise dominated by S/H capacitance within the required bandwidth, a structure- and substrate-independent relationship between minimal power, $P_{\min}$, sampling rate, and resolution is:

$$P_{\min} = k \cdot T \cdot f_s \cdot 10^{(6N+1.76)/10}\ \text{W}, \tag{8}$$

where k is Boltzmann's constant and T is temperature. This is as derived in [9]. This equation can be rewritten as



[FIG4] **Power versus sampling rate.**



[FIG5] **Historical trend in figure-of-merit *P*.**

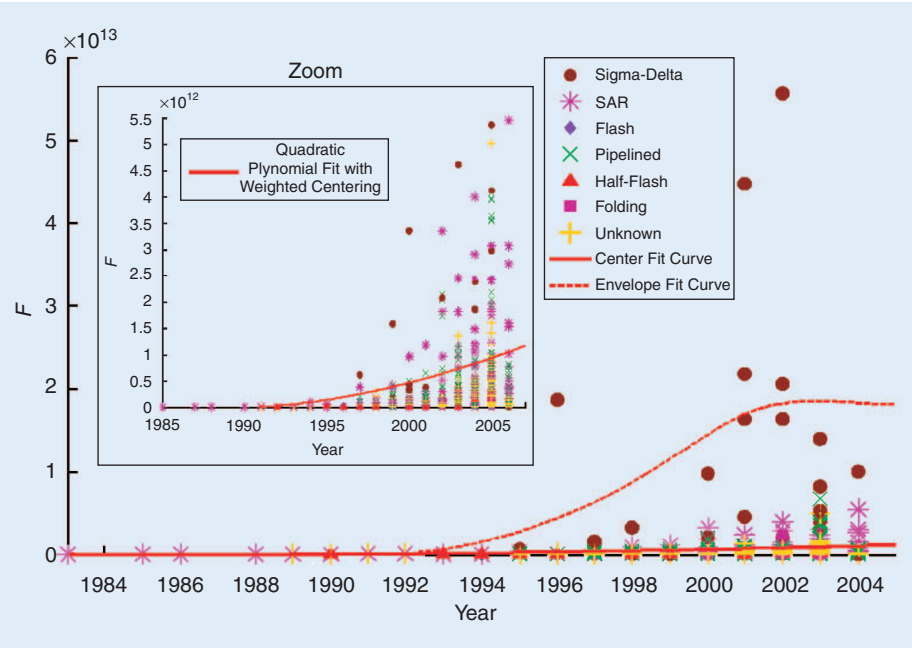
$$\log_{10}(P_{\min}) = \log_{10}(f_s) + \frac{6N}{10} + \log_{10}(k \cdot T) + 0.176. \quad (9)$$

Equation (9) implies two basic relations:

1) $\log_{10}(P_{\min})$ and $\log_{10}(f_s)$ have a linear relationship with slope of 1
2) $\log_{10}(P_{\min})$ increases with the number of bits, N, with a slope of 6/10.

However, these are not observed clearly from our ADC sample set. This means that the two relationships are not independent from each other. Thus, a combination of f_s and N is plotted versus power in Figure 4, which shows a neat linear slope close to 1, as predicted in (9).

In Figure 4, however, the linear regression line yields a slope of 1.1, a little larger than predicted by (9). The reason is that the assumptions for (9) oversimplify the ADC, so this derivation only serves to calculate the theoretical minimal power that the S/H circuit should require in an ADC. In other words, (9) completely ignores the power used by other active circuits in practical ADCs, including buffer amplifiers, internal DACs, and digital encoders. Equation 9 also ignores the structure differences that have strong impact on power dissipation. Practical comparators' accuracy is limited by random voltage offsets, which can only be overcome with improved transistor matching at the cost of increasing device size and using calibration or error correction [10], [11]. Increasing the device size will increase capacitive loading for the S/H stage as well as parasitic capacitive loss, and using calibration and error correction will also increase additional power dissipation. The parallel structures, although having superior speed, offer dynamic performance highly dependent on an accurate definition of the reference voltage sensed by each comparator so that they have critical issues of mismatch compensation and accuracy calibration to reduce distortion [6]. For example, the flash structure, even with the smallest number of bits, consumes the highest power per signal channel, as shown in Figure 5.

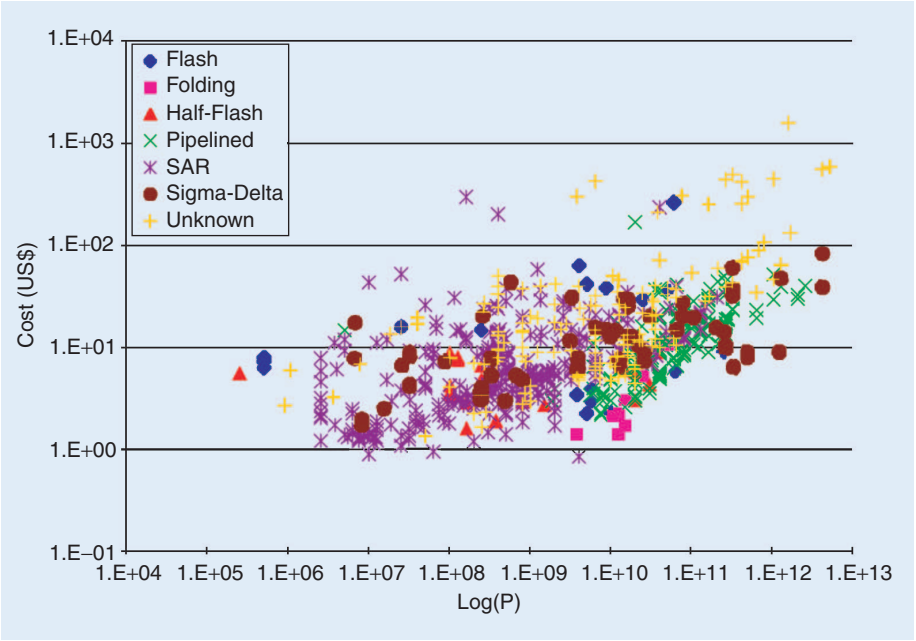


[FIG6] **Historical trend in figure-of-merit *F*.**

In Figure 4, as shown by the minimal-mean-square-error curve fitting line for all the ADC samples, power dissipation shows a monotonically increasing trend with sampling rate. However, this trend is hard to quantify because power dissipation largely depends on specific semiconductor technologies, and those proprietary technologies make the general power analysis very difficult. It is even worse in the case of multichannel ADCs, which only require the same power as single-channel counterparts. This makes the power analysis per ADC channel almost meaningless without knowing the internal ADC structure, such as drain-current sharing circuitry or multichannel multiplexing mechanism. As a result, power dissipation per channel is preferably analyzed

with respect to specific structures. Such structure-dependent power grouping is clearly shown in Figure 4 with a comprehensive sample set from over 21 years, a time period long enough for ADCs to break this grouping rule if they can.

Why does power directly depend on the ADC structures? Power is mostly consumed in the comparator processes. According to different comparing mechanisms, the actual number of comparisons per seconds ranges from Nf_s (SAR structure) to $2^N f_s$ (flash structure). Flash ADCs consume the highest power with the lowest ENOB because of their purely parallel structure. Pipelined and half-flash mostly overlap because they have same iterative (half-parallel) structure. Although SAR also has an iterative structure, it consumes much less power because it reuses the same comparator. Besides structure, power dissipation also depends on sampling rate and resolution. For example, SAR devices have a spread of power dissipation as wide as sigma-delta ADCs but have much higher sampling rates; on the other hand, sigma-delta ADCs consume relatively higher power due to high over-sampling rates, but have much higher resolution (see Figure 1). It is our belief that this structure dependency will keep determining the power dissipation of different ADCs in the future.

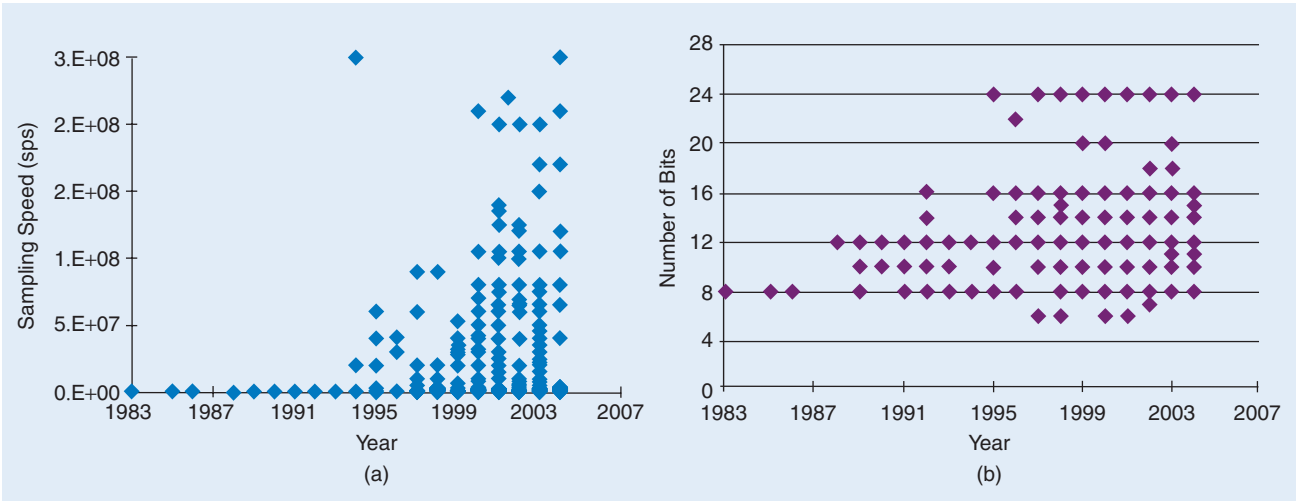


[FIG7] **Cost versus performance P for different structures.**

HISTORICAL TRENDS IN ADC PERFORMANCE

It is interesting to look at the development of ADCs over the years. The historical trends of ADCs provide some insight into their progress and development, which we can then compare with Walden's publication that discusses the ADC trends up to 1997 with future projections into 2015. Walden holds a relatively pessimistic view for the future of ADC improvement as he points out a lack of general improvement in the P (1), where the F (2) has steadily increased due to the trend towards monolithic and power-efficient devices. Up to the time where his data and analysis ends, he is correct; however, our data shows ADCs seven years beyond Walden's data and refutes his low expectations.

In both Figures 6 and 7, although the envelope of the sample set by itself already exhibits the exponential improvement with time, we apply curve fitting (using MATLAB) to extract the accurate trend for the entire sample set. Both the envelope and the mean of P (in Figure 6) and F (in Figure 7) are extracted since the envelope shows



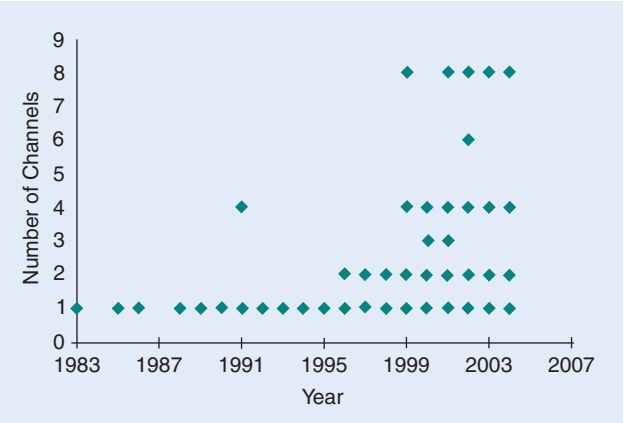
[FIG8] **Historical trends in (a) sampling speed and (b) number of bits.**

the performance boundary and the mean of the sample set indicates the application demand. To achieve the best match with the least residual error, both smoothed-spline curve and weighted-centered polynomial curve are applied to the envelope and mean respectively. Note that there are more than 900 ADC samples in the plots, so the concentration of the samples is less obvious than the spread due to overlapping. In both Figures 6 and 7, there is a small plot inside showing a zoomed curve fitting for the mean of the sample set where the sample overlapping is easier to see.

Looking at these two figures, Walden's claim of improvement in F but not in P holds true to the time when his paper was published. But since about 1994, P and F have started increasing almost exponentially. Walden's analysis is still true about the improvement in F as low-power devices are increasingly available on the market. At the same time, P has started to increase rapidly due to the larger number of available devices with faster sampling rates and higher resolution.

Besides the trend extraction for the entire sample set, the structure information is also provided. Defined as a product of resolution and sampling speed, P does not have a strong structure dependency, while F does because power dissipation is strongly related to structure.

Looking closely at both the graphs, sigma-delta ADCs do not always have the highest P, but they form the highest F envelope in 1995–2004. However, a decrease in F is shown as a result of increased power dissipation for higher resolutions. As shown in Figure 1, sigma-delta ADCs are the only choice when more than 16-b resolution is required. To overcome the increased distortion due to higher resolution, higher over-sampling rates are needed, which consumes much more power. From our data, sigma-delta converters have an average power-to-sampling-speed ratio of 0.1096 mW/sps, this is two orders of magnitude above flash, SAR, and half-flash devices. For comparison, pipelined ADCs have this ratio of only 1×10^{-5} mW/sps due to a much smaller number of comparisons, and folding converters have the smallest ratio at 1.502×10^{-6} mW/sps due to their having the least number of comparators. The power-to-sampling-speed ratio tells us that the faster sigma-delta converters are pushed, the more power they will consume, which negatively affects F more than the speed increase improves P.



[FIG9] Historical trends in number of channels per ADC package. (Note that there are many ADC samples overlapped at different number of channels.)

Sigma-delta and flash converters are the only two structures that have a decreasing F over time. The reason is probably due to the commercial demand. Flash devices specialize in very high sampling rates but achieve poor linearity for high resolutions, while sigma-delta converters enjoy much better linearity with high resolutions but suffer in their maximum effective sampling rates. These two types of ADCs are more niche products serving specific requirements. Sigma-delta converters are desired for high resolutions with low speeds, while flash devices are used for the exact opposite purpose. Both of them have to sacrifice much more power for more balanced performance, which causes a decreasing F. SAR, pipeline, and other structures fill in the midrange demands for speed (flash) and resolution (sigma-delta), achieving decent speeds and decent resolutions and giving themselves large performance metrics.

Figures 4 and 5 show that the choice in selecting an ADC is strongly tied to application requirements as a guide for design engineers. To provide another dimension for comparison beyond the technical discussions, we wish to provide a shopping guide with performance versus cost, especially for our entire commercially available ADC sample set, as shown in Figure 7.

It is interesting to see that folding converters, although not widely available on the market, have the best quality-to-cost ratio around the middle performance range. At higher performance range, sigma-delta ADCs become the first choice. Also, sigma-delta ADCs have the widest spread of performance. It is not surprising to see SAR ADCs, the most classical and popular type, cover the main performance area. However, SARs have a medium quality-to-cost ratio. Pipelined ADCs focus on higher-performance applications with a little higher cost. Flash ADCs tend not to be the most cost efficient choice, although they have a performance range as wide as sigma-delta. It is important to mention that Figure 7 is not only a price list but a global view of performance and application distributions among all ADC technologies.

FUTURE TRENDS OF ADCS

For over 20 years, the development of ADC technologies has always been driven by emerging applications, which results in an exponential P increase. However, the specific requirements for sampling speed and number of bits have different trends, as shown in Figure 8.

Note that in the right plot of Figure 8, there are many ADC samples overlapped at discrete resolutions. The demand for higher sampling speeds keeps increasing, while the requirement for greater resolution has ceased since 1995. It is because such ADC resolution is enough for most modern applications such as 3 G cellular and wireless LAN. Although there are other applications pushing ADC performance extremities, such as UWB, orthogonal frequency division multiplexing (OFDM), and radar systems, the major challenge in ADC design has changed from the performance expansion to power reduction, especially for mobile communications and

SDRs. During recent years, we have witnessed a rapid increase of multichannel ADCs with nearly the same power as single-channel counterparts, as shown in Figure 9. ADCs with multiple channels are ideal solutions for diversity-based wireless applications and SDR platforms. More importantly, power dissipation and cost are greatly reduced for each signal channel, especially for mobile communications.

As SDR becomes the most promising radio platform for wireless communications in the near future, the development of ADC technology turns out to be the key issue in enabling wideband spectrum analysis, radio-frequency digital processing, and multistandard communications [9]. There is increasing interest of achieving ultra-high speed sampling devices on the order of 100 GHz with sampling bandwidths of tens of megahertz [11]–[13], which points to the resurgence in the research for faster and more accurate ADCs that Walden showed was lacking just a few years ago. Unfortunately, power, size, and cost are the major barriers that prevent lab prototypes from entering the market.

With the demand for higher speed and resolution, power saving will continue to be a hot research area for ADCs. Although general relationships between performance and power are illustrated in Figures 4–6, it is hard to derive a general closed-form equation of P versus power for all types of ADCs because of the strong structure dependency. For example, different combinations of ENOB and f_s can result in the same P, while they may result in totally different power dissipations. Therefore, a structure-based power analysis might be a promising future research topic. Furthermore, various substrate technologies further increase the complexity of power analysis [3].

CONCLUSIONS

We have analyzed the internal relationships of the performance parameters of ADCs, showing their frequency dependency and structure dependency. We have looked into the history and current trends in ADC technologies based on the P and F figures-of-merit. Historically, there was an increase in performance around 1994, with a share rise around 1997, which broke the stagnant performance discussed by Walden [1]. While the past few years have shown a sharp increase in ADC performance, we have shown that performance and power dissipation depend greatly on the ADC structure and the target applications. With the progression of wideband radio systems like UWB and OFDM comes a growing demand to provide faster sampling rates and higher resolutions with lower power dissipation. With the innovation of advanced communication techniques like multi-input/multi-output and multistandard radios, the demand is growing to provide multichannel programmable data conversion, both of which are pushing the performance of ADCs further in the coming years.

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