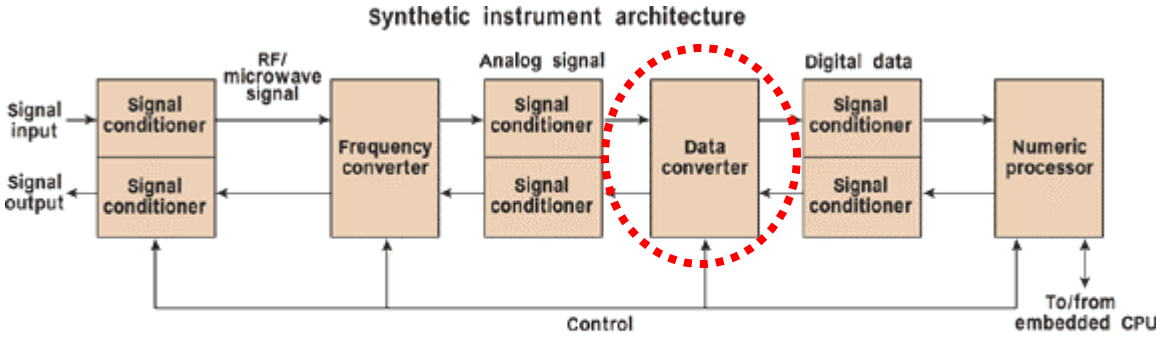
Typical SI architecture

A Synthetic Instrument (SI) is a reconfigurable system that links a series of elemental hardware and software components, with standardized interfaces, to generate signals or make measurements using numeric processing techniques. In other words, it's a concatenation of hardware and software modules used in combination to **emulate** a traditional piece of electronic instrumentation.



A basic SI system consists of a high-speed ADC and DAC at the core of the measurement system, as well as signal conditioning and up-converters and down-converters. Some would recognize this concept as "software radio."

http://www.mwrf.com/Articles/ArticleID/9795/9795.html
http://rfdesign.com/mag/411defensef3.pdf
http://www.analogzone.com/tmed0124.htm

Synthetic or virtual?

You're probably wondering, "What's the difference between a *synthetic* instrument and a *virtual* instrument?"
Mike Granieri of Phase Matrix says "A virtual instrument utilizes the functionality of several independent, or discrete, instruments under a common software framework, as if they were one instrument."
He defines a synthetic instrument as a collection of **reusable** building blocks (**ADCs, DACs,** upconverters, and downconverters) with automated software that perform a specific test measurement or stimulus function.
That is, a synthetic instrument focuses on the repeated use of **core** functional components instead of higher-level discrete instruments.
http://www.reed-electronics.com/tmworld/article/CA385792.html

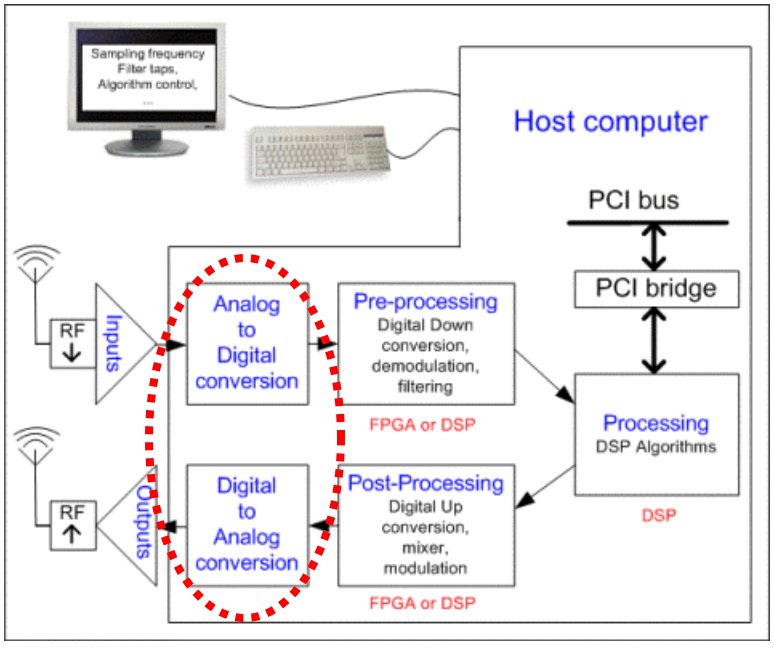
Typical SDR architecture

Software Defined Radio (SDR) is a collection of hardware and software technologies that enable reconfigurable system architectures. SDR provides an efficient and comparatively inexpensive solution to the challenge of building multi-mode, multi-band, multi-functional wireless devices that can be adapted, updated, or enhanced by using software upgrades.

http://www.4dsp.com/SDR.htm

http://www.broadcastpapers.com/broadband/WiproSDRadio.pdf

http://www.sdrforum.org/



New technology facilitates true software-defined radio

While the article summarizes products available for software-radio application, it presents for the first time a carrier speed 5 GHz RF to a digital converter, which when coupled with state-of-the-art filtering software, can be used to meet the SDR Forum's definition of the ideal software radio. With this technology, the article demonstrates the first true software radio.

By Ronald M. Hickling

Radio technology as we know it is undergoing sweeping changes. For those of you old enough to recall, many of the earliest radio receivers were built using crystals and fine wire probes that were moved by the listener to form a diode and included a variable inductor with a slider to tune the receiver to a radio station's frequency so one could hear music or voice. The need for precise tuning has changed little in the more than 80 years since CW transmitters replaced the very broadband spark gap approach originally used by Marconi. Today, even with advancements in RF design and the powerful digital processing available, all radio receivers still use analog parts to tune the radio to a specific carrier frequency. But this is about to change. The FCC, the SDR Forum and the radio industry are united in the pursuit of the ideal software-defined radio or SDR.

According to the Federal Communications Commission (FCC), "In a software-defined radio (SDR), functions that were formerly carried out solely in hardware, such as the generation of the transmitted signal and the tuning and detection of the received radio signal, are performed by software that controls high-speed signal processors." The SDR Forum defines an SDR device as one that functions independently of carrier frequencies and can operate within a range of transmission protocol environments. But the SDR Forum goes a step further by defining the ideal SDR as one that has transceivers that perform upconversion and downconversion between baseband and the RF carrier itself exclusively in the digital domain, reducing the RF interface to a power amplifier in the transmit path, a low noise amplifier in the receive path, and little or no analog filtering. In this ideal radio, it is possible to upgrade or completely change the features by simply uploading new software.

This ideal radio defined by the SDR Forum has, until recently, been unachievable due to the lack of very high-frequency RF to digital converters capable of converting carrier frequencies directly to digital data. Now new integrated circuit processes are offering higher speed and lower power. State-of-the art IC design is being applied to these new processes to enable RF to digital conversion directly on carrier frequencies above 5 GHz.

This article describes the products available in production today and then presents the first carrier speed 5 GHz RF to digital converter to be proven in silicon. This converter, coupled with state-of-the art filtering software, can be used to meet the SDR Forum's definition of the ideal SDR. With this technology the first true software radio is achievable.

Effective radio communication

SDR is of critical importance to the future of efficient and effective radio communication that must include interoperability. As we have seen, municipal services such as fire departments and police departments often have radios that will not communicate between services. With the ideal SDR radio, software can be used to act as an interpreter between completely incompatible radio frequencies and modulation techniques. 900 MHz radios can talk to 2.4 GHz radios, GSM cell phones can communicate with CDMA phones. And the military can start to move to radios that allow all of the services to communicate seamlessly. The U.S. Military Joint Tactical Radio System (JTRS) program has announced the goal of supporting 33 modulation techniques on multiple carrier frequencies ranging from 2 MHz to 55 GHz with one radio design. The ideal SDR radio will be critically important in meeting that goal.

Until now, radio design has been limited to the use of analog RF front ends (RFEs) for upconversion and downconversion to an intermediate frequency (IF) of below 100 MHz that off-the-shelf analog to digital converters (ADCs) could handle (Figure 1).

The radio receiver is the toughest challenge for the ideal SDR. The ideal receiver must extract rapidly changing information from small RF signals buried within a sea of noise. Newer RFEs are using superheterodyne, direct-conversion, and hybrid techniques. But these radios do not meet the ideal radio defined by the SDR Forum. Instead, they extend the software-defined baseband processors that today's cell phones employ to become software-defined IF processors.

As an example, a GSM900 receiver with a center

Parameter	GaAs	SiGe
Maximum clock frequency	> 5 GHz	> 15 GHz
SINAD (signal to noise+distortion)	> 70 dB	> 110 dB
Eff. resolution bits at 2.5 GHz carrier:	14 bits	18 bits
10 MHz BW	11 bits	14 bits
100 MHz BW		
Matching I/Q	within -70 dBc	Within -90 dBc
RF input voltage range (differential)	-1.5 V <Vin < 1.5 V	-0.5 V < Vin < 0.5 V
Power supplies	Single +6 V	Single +3.3 V
Power dissipation	5 W	< 1 W
High-speed interface levels	PECL	LVDS
Number of taps in FIR	2048 I / 2048 Q	8192 I / 8192 Q
Digital interface levels	2.5 V/3.3 V CMOS	1.8V /2.5 V CMOS

Table 1. RF to digital converter target specs by process.

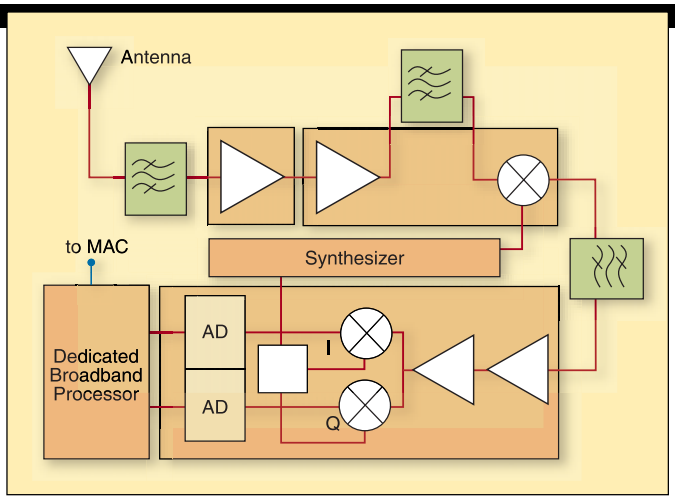


Figure 1. Up to now, SDR receivers depended on analog front ends to feed 70 MHz ADCs.

frequency of 947.5 MHz and a 25 MHz bandwidth has an 80 MHz IF that is at nearly the maximum analog-to-digital conversion (ADC) rate for today's off-the-shelf high-resolution ADCs. This radio's high-frequency mixing process generates spurious images in frequency bands between 1095 MHz and 1220 MHz. Image rejection filters can reduce these images, but not by the 110 dB that the blocking specification requires. Moving the IF up to 500 MHz creates images 1 GHz above the signal frequency that are easier to filter but require multiple downconversion steps to reach the usable ADC sample rates.

Until recently, the best off-the-shelf ADCs offered input frequency-handling capability that is limited to 70 MHz to 125 MHz at 14-bit resolution. Most radio designers are currently using IF at about 60 MHz to 70 MHz. Sources for these ADCs include Analog Devices, Linear Technology Corp., Maxim Integrated Products, Texas Instruments Inc. and TelASIC. These sources have defined the next target as about 170 MHz, which makes it easier to meet blocking-signal specifications and simplifies the first RF downconversion stage.

RFEs still rely on analog components

GSM cell phones incorporate traditional superheterodyne receivers that translate incoming RF to a fixed IF value by multiplying the signal with a local oscillator frequency in an analog mixer, offering simpler gain and filter design. For example, downconverting a 1 MHz signal into a 100 kHz IF, the first local oscillator frequency is 1.1 MHz. This mixing process generates spurious images that differ in frequency from the wanted signal by twice the IF value, requiring image-rejection filters to eliminate noise. These unwanted images cause designers to use higher IF frequencies to increase the separation between the signal and its image, simplifying filter requirements. Because the ideal SDR radio receiver requires wide bandwidth to accommodate protocols such as CDMA or simply to search for signals of interest, the narrowband superheterodyne model is not usable. The first IF filter in a superheterodyne cell phone receiver is usually a surface acoustic wave (SAW) device that tunes the receiver to meet the incoming signal specifications.

Another approach to current SDR front ends uses a variation of the direct conversion receiver architecture that eliminates SAW filters. Instead, an in-phase/quadrature (I/Q) mixer

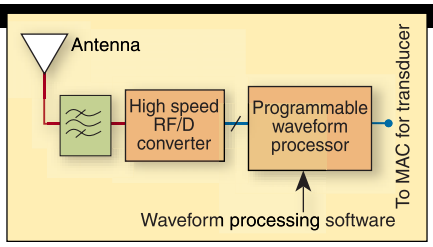


Figure 2. True software radio uses a single-carrier speed RF-to-digital converter to eliminate all analog front-end components. The output is then fed through proprietary filtering software and firmware.

transforms the RF to complex baseband in one step, typically centered on dc, and a low-pass filter can then condition the signal before ADC. Mixing the signal down to dc (zero-IF) folds the spectrum around zero frequency, producing positive and negative frequencies and dividing the signal bandwidth in two. A demodulator and DSP resolve the ambiguity in the received signal's instantaneous frequency by observing the I/Q phase relationship: If Q leads I, the frequency is positive. Otherwise, it is negative. If the mixers were ideal (i.e., produced only sum and difference products) and the I and Q paths operated in perfect quadrature and had perfect amplitude balance, the image signals self cancel. In practice, imbalances in the real (I) and imaginary (Q) paths allow the unwanted sideband to interfere with the signal of interest. Furthermore, since phase noise peaks at zero offset from the carrier frequency (correspondingly "dc" at baseband frequencies), that translates to a wandering "dc" level that sets a lower frequency limit in which modulating information can be contained and conveyed.

Software-controlled radios

Recently, Vanu Inc. became the first company to successfully complete the FCC's certification process governing software-radio devices. The FCC has officially recognized a new category of radios—software-defined radios. The Vanu Software Radio consists entirely of software applications that support all of the GSM cellular base station functionality running on off-the-shelf Hewlett Packard ProLiant servers with an Analog Devices Corporation Digivance™ RF subsystem. This system can support multiple radio standards, protocols and frequencies on a single industry standard server. It allows modification of the RF planning and assignment of standards through remote software parameter changes. It supports upgrades to

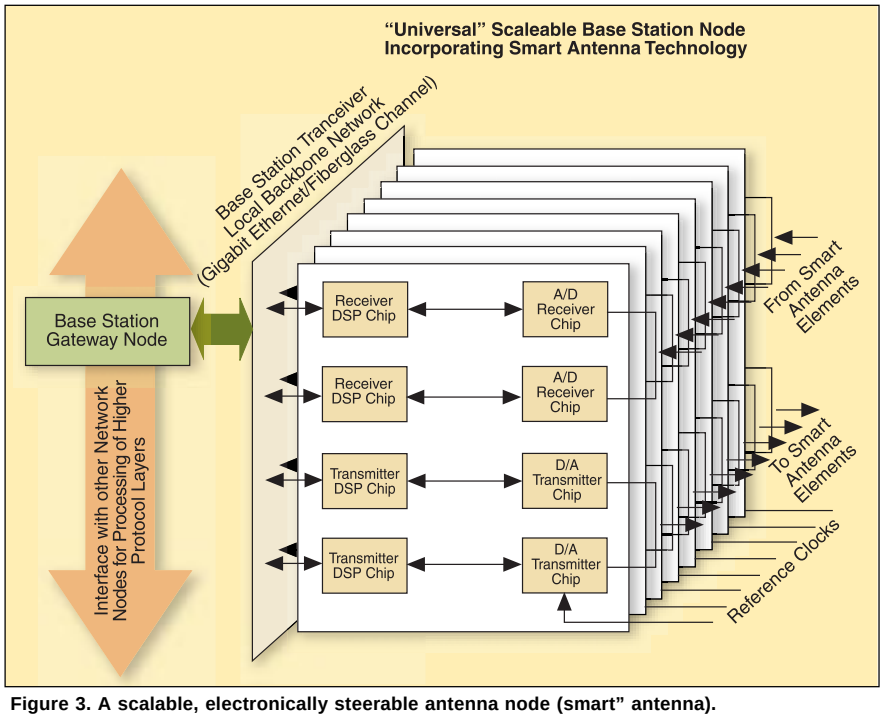


Figure 3. A scalable, electronically steerable antenna node (smart" antenna).

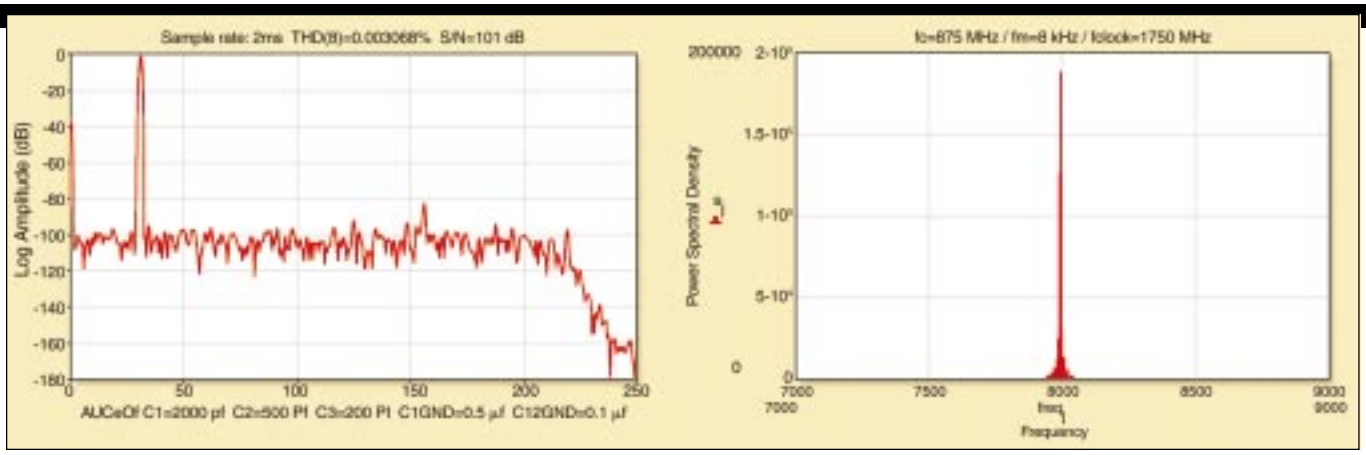


Figure 4. Performance of delta-sigma A/D converters using (a) CMOS technology and (b) GaAs MESFET technology.

new standards through a software download. Note that the ADC RF subsystem is based on a purely analog RFE with an IF at 70 MHz.

Sirific Wireless Corporation offers a single-chip CMOS RF transceiver for multistandard applications. This device incorporates all the traditional AFE components on a single IC including a direct conversion receiver, a direct modulation transmitter, and a Sigma-Delta fractional-N synthesizer. It needs only a few external components in order to support up to four distinct frequency bands. The direct conversion receiver includes a four-band differential LNA, a quadrature demodulator, dc offset correction, digitally tunable baseband filters and variable gain amplifiers. Sirific's family of RF transceivers is based on its Virtual LO™, a local oscillator frequency planning technique, and FlexRF™, a dual mixer down/upconversion approach. Both patented pieces of intellectual property work together in the receiver and transmitter to enable multistandard multiband RF transceivers that adhere to and exceed both standard RF criteria as well as direct conversion parameters.

Hypres Inc. uses superconducting electronics to achieve SDR operating parameters that are close to the ideal SDR. The company's technology is presently available up to 2 GHz range and offers 14 to 24 effective number of bits (ENOB) with 100 dB to 160 dB SFDR. The high-resolution ADC offers 20 ENOB with 130 SFDR with 60 MHZ bandwidth at 2 GHz carrier frequency. The RF front end offers orders of magnitude better sensitivity with ultralow noise and bit error rates (BERs) less than 10 to 15 at even wide bandwidths.

Philips Semiconductors recently announced its SAF7730—a single-chip, dual-IF car radio and audio DSP that enables designers to cost effectively implement a range of functions, such as adaptive ultrabass boost, to further product differentiation using a single platform. Elsewhere, equipment designers such as U.K.-based RadioScape are using software techniques at the core of their digital audio broadcast (DAB) and digital radio mondiale (DRM) products. RadioScape

bases its consumer-level RS200 DAB/FM receiver module on Texas Instruments' DRE200 receiver chip.

Present ADC technology

The state-of-the-art in off-the-shelf ADCs is presently limited to less than 100 MHz and, therefore, requires that all SDR implementations use analog downconverters and upconverters to get to the 2 GHz to 5 GHz RF carrier signals. One exception is the ADC from Hypres, which is a superconducting technology that has a significant difference in cost than IC technology used by the majority of ADC suppliers.

All ADCs must have an input bandwidth and linearity (i.e., effective number of bits or ENOB) that is sufficiently high to avoid distorting the signal. One example is TI's all-CMOS, 125 Msps ADS5500, which consumes just 780 mW from a 3.3 V supply. Its input sample-and-hold amplifier has an analog bandwidth of some 750 MHz that allows direct IF sampling beyond 300 MHz. For a faster conversion rate, TelASIC's monolithic TC1410 uses SiGe/BiCMOS to achieve 240 Msps with 500 MHz input bandwidth; the trade off is as much as 14 W power dissipation from ±5 V supplies.

Protocols such as GSM and CDMA use frequencies that exceed 2 GHz, so the ideal SDR requires converters that run at 5 GHz or more. Although GSM shares 200 kHz among eight time-division multiple access (TDMA) slots, 3G services have channel bandwidths as high as 5 MHz that the protocols share between multiple sessions. This shift from narrowband to wideband demands digital signal processing (DSP) techniques for signal content extraction and will eliminate analog filters by moving filtering, channel selection, and baseband processing into the digital domain.

RF to digital converter

TechnoConcepts' RF to digital converter is the first 5 GHz carrier speed RF to digital converter capable of direct conversion of a 5 GHz RF carrier, eliminating all analog IF circuits. This receiver is based on a very high speed 5 GHz delta-sigma converter that digitizes signals by modulating the analog input (radio signal) into a high-speed 1-bit digital datastream. The datastream is then digitally processed on the same IC to produce a high-resolution multiple bit word stream sent at a slower data rate. This is the first device to completely eliminate the need for conventional radio receiver downconverters and the associated external analog components. This RF to digital converter is a closed-loop system in which the order of the loop and the input bandwidth may be changed to achieve the desired resolution. A narrow bandwidth results in higher resolution than a wide bandwidth.

The underlying technology was originally developed under a Small Business Innovation Research (SBIR) Program sponsored by the U.S. Department of Energy. The company then took the development further by inventing a circuit architecture that simultaneously extracts the information signal from an incoming radio transmission and digitizes it with extremely high resolution. This architecture is capable of achieving dynamic ranges of up to 110 dB, enabling the processing of weak signals even in the presence of strong interference. A dynamic range of 55 dB to 100 dB (depending on bandwidth) is achievable using this architecture. The performance analysis of high-order delta-sigma RF to digital converters operating at 5 GHz shows that the expected signal-to-noise ratio (SNR) depends on the operational spectrum width and the order of delta converters. For instance, the estimated value of SNR in decibels for a second-order delta converter with an operational spectrum width of 30 MHz is 55.

The third-order SNR for the same spectrum width is 80. The estimated value of SNR in decibels for a second-order delta converter with an operational spectrum width of 10 MHz is 75. The third-order SNR for the same spectrum width is 100. The estimated value of SNR in decibels for a second-order delta converter with an operational spectrum width of 2 MHz is 100. Other performance specifications for this device are given in Table 1.

The company has further improved this technology by developing a full spectrum of software filters that work in conjunction with the digitized RF signal. These filters do the work previously done by the analog downconverters, mixers and IF analog circuitry. The result is the first true software radio small enough to actually be packaged at the antenna and present digital data to off- the-shelf baseband digital processors (Figure 2).

Other key technologies

Although high-speed RF/D converter technology has been the key enabler in software radio, advances in other key technologies have also contributed to making tunerless frequency agile software radios practical. These include:

- compact, wideband antennas;
- electronically steerable antennas;
- deep submicron semiconductor technology; and
- deep submicron semiconductor technology.

Wideband antennas: Thus far, the advancements in microelectronics have far outpaced the advances in antenna technology with respect to the implementation of ideal (tunerless) software radio. But the advent of inherently wideband antenna technologies (for example, fractal antennas) has greatly reduced the need for tuning the resonance of the antenna. This important advancement has obviated the need for complex band switching in the antenna-matching system.

Electronically steerable antennas: Electronically steerable antennas (also called "smart" antennas) have been in existence since their initial introduction in defense electronics decades ago. Yet, the unavailability of low cost, low-power microelectronics had been a barrier to their use until the 1990s. True software radio permits the user to share multi-element antennas between multiple signals, each with a different frequency and radiation pattern (and therefore different direction of maximum gain).

Deep submicron semiconductor technology: With the rapid advance of deep submicron lithography semiconductor processes, the ft has exceeded 50 GHz for even commercial CMOS processes. This has enabled the development of circuits previously thought impractical—namely RF CMOS. Furthermore, the ability to integrate higher-speed bipolar processes on the same substrate as CMOS has made possible the operation of high-speed mixed signal functions at speed previously thought impossible. Besides improving yields, monolithic approaches to receiver front-end circuits have avoided the need for driving high-speed signals into and out of large capacitive loads (from packaging) that have resulted in a dramatic reduction in power dissipation for a given operational speed.

Conclusion

The availability of high-speed RF/D converters has made possible the implementation of true software-radio transmitters and receivers that avoid the use of passive components to tune and modulate/demodulate high-speed wireless signals. These converters using conventional CMOS and advanced semiconductor technologies have been demonstrated to have performance comparable to or better than conventional analog front-end circuits and enable tunerless architectures wireless transmitters and receivers. Next-generation devices promise to further exceed the performance of analog components enabling the extraction of weak signals in noisier and more interference-ridden environments. RFD

ABOUT THE AUTHOR

Ronald M. Hickling, co-founder, CTO, director, holds a master of science in electrical engineering from UCLA. He has nearly 25 years of experience in communications systems and integrated circuits related to communications for U.S. defense and commercial contractors. Beginning in 1980, Hickling began his career with Hughes Space and Communications, a Hughes Aircraft company, developing circuits for satellite communications.

He joined start-up Gigabit Logic in 1984 and headed development teams on numerous mixed-signal communications projects. He was involved in development efforts with contract clients such as DEC, Rockwell-Collins and Bell Communications Research.

Hickling has been awarded five U.S. patents with others pending. He has been published in numerous industry journals and is a member of the IEEE and Tau Beta Pi.