Analog-to-Digital Converter Survey and Analysis

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***Abstract*—Analog-to-digital converters (ADC's) are ubiquitous, critical components of software radio and other signal processing systems. This paper surveys the state-of-the-art of ADC's, including experimental converters and commercially available parts. The distribution of resolution versus sampling rate provides insight into ADC performance limitations. At sampling rates below 2 million samples per second (Ms/s), resolution appears to be limited by thermal noise. At sampling rates ranging from $\sim$2 Ms/s to $\sim$4 giga samples per second (Gs/s), resolution falls off by $\sim$1 bit for every doubling of the sampling rate. This behavior may be attributed to uncertainty in the sampling instant due to aperture jitter. For ADC's operating at multi-Gs/s rates, the speed of the device technology is also a limiting factor due to comparator ambiguity. Many ADC architectures and integrated circuit technologies have been proposed and implemented to push back these limits. The recent trend toward single-chip ADC's brings lower power dissipation. However, technological progress as measured by the product of the ADC resolution (bits) times the sampling rate is slow. Average improvement is only $\sim$1.5 bits for any given sampling frequency over the last six–eight years.**

***Index Terms*—Analog-to-digital converters, aperture jitter, comparator ambiguity, input-referred noise, signal-to-noise ratio, spurious-free dynamic range.**

I. Introduction

DURING the past two decades, the rapid evolution of digital integrated circuit technologies has led to ever more sophisticated signal processing systems. These systems operate on a wide variety of continuous-time signals including speech, medical imaging, sonar, radar, electronic warfare, instrumentation, consumer electronics, and telecommunications (terrestrial and satellite). One of the keys to the success of these systems has been the advance in analog-to-digital converters (ADC's) which convert the continuous-time signals to discrete-time, binary-coded form. As an example, in the telecommunications arena, advances in software radio development [1]–[3] have provided impetus for ADC performance improvements, especially for sampling rates of approximately 100 million samples per second (Ms/s). More generally, the large number of signal types to be digitized has led to a diverse selection of data converters in terms of architectures, resolution, and sampling rates.

Despite the variety in ADC's, their performances can be summarized by a relatively small number of parameters: stated resolution (number of bits per sample), signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and power dissipation $P_{\rm diss}$ [4]. Two-tone intermodulation distortion is also important for ADC's to be used in receivers. Fig. 1 shows ADC resolution, as stated by the manufacturer versus sampling rate, $f_{\rm samp}$. Over 150 converters (listed in Appendix I), including experimental systems and commercially available parts, are represented in the graph. Strictly speaking, this data does not represent measured performance. It does, however, show two important features. First, approximately one bit of resolution is lost for every doubling of the sampling rate. This is indicated by the state-of-the-art line on the graph. Second, the highest Nyquist sampling rate attained is 8 giga samples per second (Gs/s) [5]. An analysis of SNR shows that the 1-bit per octave slope is related to the sample-to-sample variation of the instant in time at which sampling occurs. This variation is called aperture jitter or aperture uncertainty.[1] In addition, the speed of sampling is limited by the ability of the comparator(s) to make an unambiguous decision regarding the relative amplitude of the input voltage due to comparator ambiguity. This is related to the speed of the device technology used to fabricate the ADC. Device speed is measured as the frequency f_T, at which there is unity current gain.

Section II of this paper discusses how ADC's are evaluated, then Section III deals with the performancae limitations in more detail. ADC architectures that are presently under investigation are presented in Sections IV and V. Performance trends are discussed in Section VI.

II. ADC Characterization

There are a number of ways to measure and compare ADC performance. This paper focuses on determining the resolution in bits for a given sampling rate. In an increasing number of applications, the power consumption is also important. Resolution can be determined both quasistatically and dynamically. Quasi-static measures include differential nonlinearity (DNL) and integral nonlinearity (INL). Dynamic measures include SNR, SFDR, and noise power ratio (NPR). These quantities are determined from spectral analysis, usually in the form of a fast Fourier transform (FFT) of a sequence of ADC output samples. This study focuses on SNR and SFDR because dynamic performance is most important for high-speed applications and SNR and SFDR provide a more accurate measure of ADC performance than the stated-number-of-bits. In addition, SNR and SFDR are universally accepted performance measures.

SNR is the ratio of the root-mean-square (rms) signal amplitude to the square-root of the integral of the noise power

Manuscript received November 17, 1997; revised June 3, 1998 and August 9, 1998.

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Publisher Item Identifier S 0733-8716(99)02983-2.

[1] In this paper, the terms aperture jitter and aperture uncertainty are synonymous. Another term, aperture time, relates to the fact that sampling is, in fact, not instantaneous, but is actually the result of a weighted averaging of the sample over a period of time. This effect does not limit SNR to the degree that aperture jitter does, however variations in aperture time can be thought of as being included in the jitter effect.

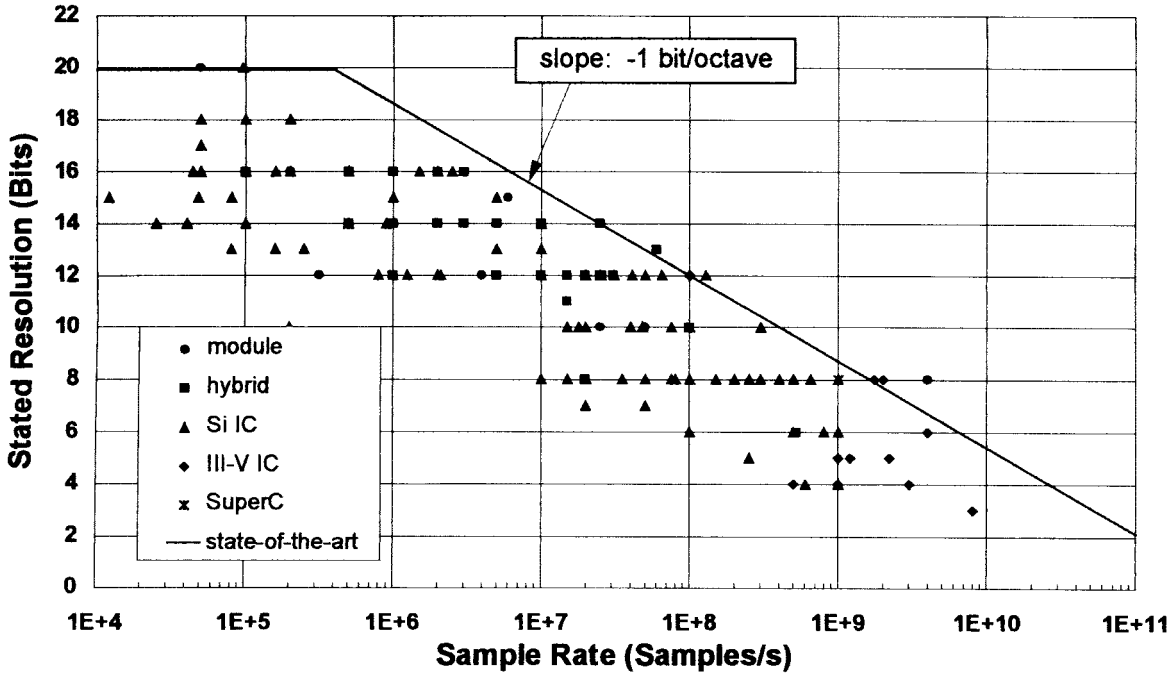


Fig. 1. Survey of ADC's.

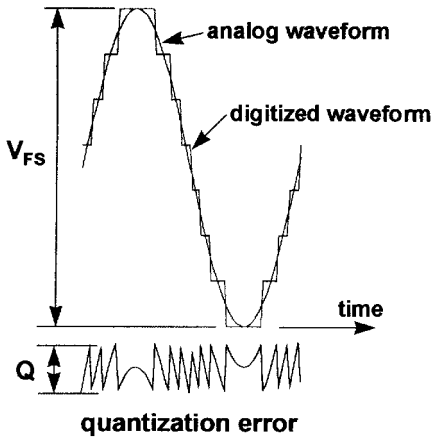


Fig. 2. Example of quantization error. V_{FS} is the full-scale voltage range, and Q is the size of the LSB.

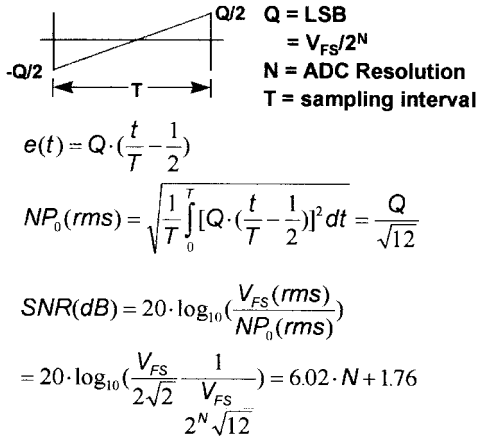


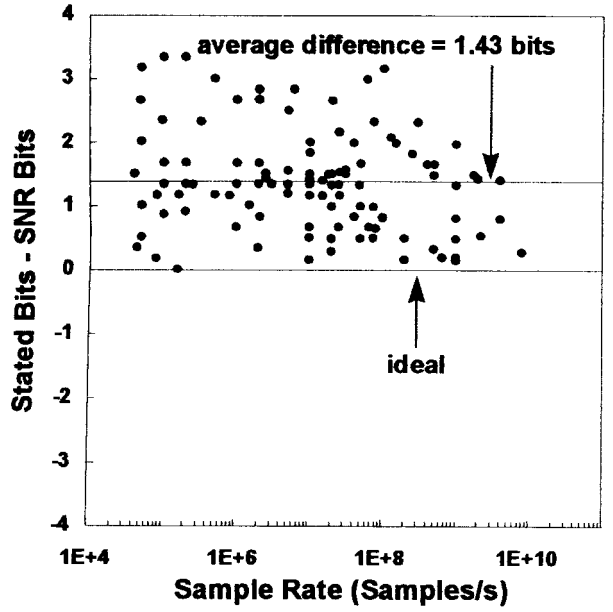
Fig. 3. Random approximation for quantization error. All errors within the range $\pm Q/2$ are equally likely. The resulting SNR is linear in the number of bits of resolution N.

spectrum over the frequency band of interest. For a Nyquist converter the frequency band of interest ranges from 0 to $f_{\text{samp}}/2$ Hz. The noise spectrum contains contributions from all the error mechanisms present. These include quantization noise, circuit noise, aperture uncertainty, and comparator ambiguity.

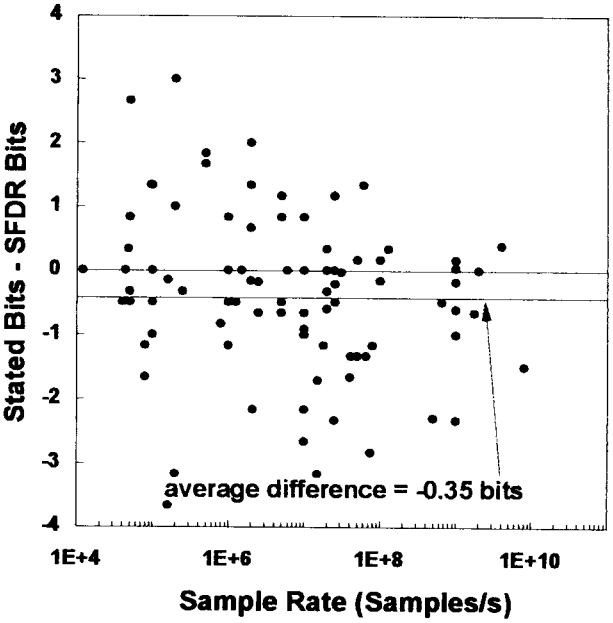
The only error mechanism present in an ideal ADC is quantization. This error arises because the analog input signal may assume any value within the input range of the ADC while the output data is a sequence of finite precision samples [6]. The example of Fig. 2 compares a sinusoidal waveform and its (reconstructed) digitized representation. The difference is the quantization error. Q is the size of the elementary quantization step, which is the least significant bit (LSB) of a binary representation of that value. In this case, the quantization error waveform and the analog waveform are strongly correlated. In a more typical case, the analog input contains frequency content due to the simultaneity of complicated signals and noise. In this situation, the quantization error is approximately random. The common white noise approximation is to assume that the probabilities of quantization errors are equal. This random error process is described in Fig. 3 with the equations of SNR due solely to quantization noise. T, the sampling interval, equals $1/f_{\text{samp}}$. N is the resolution of the converter in bits. The SNR (in dB) of an ideal ADC is shown in the lower portion of the figure $(\text{SNR} = 6.02N + 1.76)$. It can be improved only by increasing N.

In physical ADC devices, additional error mechanisms are present. Some of these other errors may also be characterized as white noise with the same expression for SNR as in Fig. 3, except that N represents N_{eff}, an effective number of bits. The notation SNR-bits refers to N_{eff}. SNR-bits is given by

$$\text{SNR bits} = (\text{SNR(dB)} - 1.76)/6.02. \quad (1)$$



(a)



(b)

Fig. 4. Comparisons of stated bits (number of output leads) with (a) SNR-bits and with (b) SFDR-bits.

The difference between stated resolution and SNR bits for a given ADC indicates the degradation in SNR due to all other error sources. Fig. 4(a) exhibits this difference with a degradation of approximately 1.5 bits for a given sampling rate, with scatter in the data.

The effective number of bits associated with SFDR is

$$\text{SFDR bits} = \text{SFDR(dBc)}/6.02. \tag{2}$$

SFDR is the ratio of the single-tone signal amplitude to the largest nonsignal component within the spectrum of interest. Fig. 4(b) shows the difference between stated resolution and SFDR-bits. Although the average difference is less than .5 LSB, there is more scatter in this plot than for the SNR data of Fig. 4(a). There are many reasons for such a wide variation. The design emphasis may render SNR more important in some cases and SFDR more important in others. Other factors include how well the design overcomes noise, aperture jitter, comparator ambiguity, and the nonlinearity of the transistors.

A complete characterization of an ADC includes the values of SNR and SFDR as a function of frequency f_{sig}, with f_{samp} as a parameter. For low values of f_{sig}, the SNR is constant. It decreases as f_{sig} increases. The value of f_{sig} at which the SNR decreases to 3 dB below the low-frequency value is the effective resolution bandwidth (ERBW). This important characteristic implies the range of frequencies over which the converter may be used. If $\text{ERBW} \geq f_{\text{samp}}/2$, then the ADC is a Nyquist converter, which is the design goal of many ADC's. The characterization of an ADC includes the highest value of f_{samp} for which Nyquist operation is sustained.

Not all widely published reports on ADC's include the conditions for Nyquist conversion. However, some still achieve noteworthy sampling speed, SNR or SFDR. To include these, the criterion for inclusion in this study is that $\text{ERBW} > \sim f_{\text{samp}}/4$. Furthermore, the low-frequency values of SNR and SFDR are used.

P, a universal measure of ADC performance, is the product of the effective number of quantization levels, $ql_{\text{eff}} = 2^{\text{SNRbits}}$, times the sample rate

$$P = 2^{\text{SNRbits}} f_{\text{samp}}\,. \tag{3}$$

F, a figure of merit that includes power dissipation [4], is

$$F = \frac{2^{\text{SNRbits}} f_{\text{samp}}}{P_{\text{diss}}}. \tag{4}$$

This figure of merit emphasizes efficiency with respect to dissipated power, P_{diss}. SNR, SFDR, P, and F are used subsequently to quantify ADC performance.

Two-tone intermodulation distortion (IMD) of ADC's is particularly relevant to receiver applications. One excites an ADC with two sinusoids of equal amplitude but with different frequencies, f_1 and f_2, observing spurious tones in the FFT spectrum of the ADC output. The strongest such tone is usually either second- $(\pm f_1 \pm f_2)$ or third-order $(\pm f_1 \pm 2f_2$ or $\pm 2f_1 \pm f_2)$. Unfortunately, IMD data reported in the literature is minimal. In addition, there is no standard set of conditions for IMD evaluation, making comparisons between ADC's more difficult. Hence, IMD's must be evaluated by the prospective user for the intended application.

III. Performance Analysis

For a better understanding of ADC performance limits, it is helpful to plot the effective resolution as determined from SFDR and SNR. Fig. 5 shows the reported SFDR (where available). Comparing Figs. 1 and 5 indicates that the effective resolution expressed as SFDR-bits is roughly the same as the stated resolution for the population is taken as a whole.

This is somewhat misleading because the difference Stated-bits minus SFDR-bits [see Fig. 4(b)], for a given converter is $\sim \pm$ 3 bits, a wide variation.[2]

[2] The terms stated bits and stated resolution are synonymous.

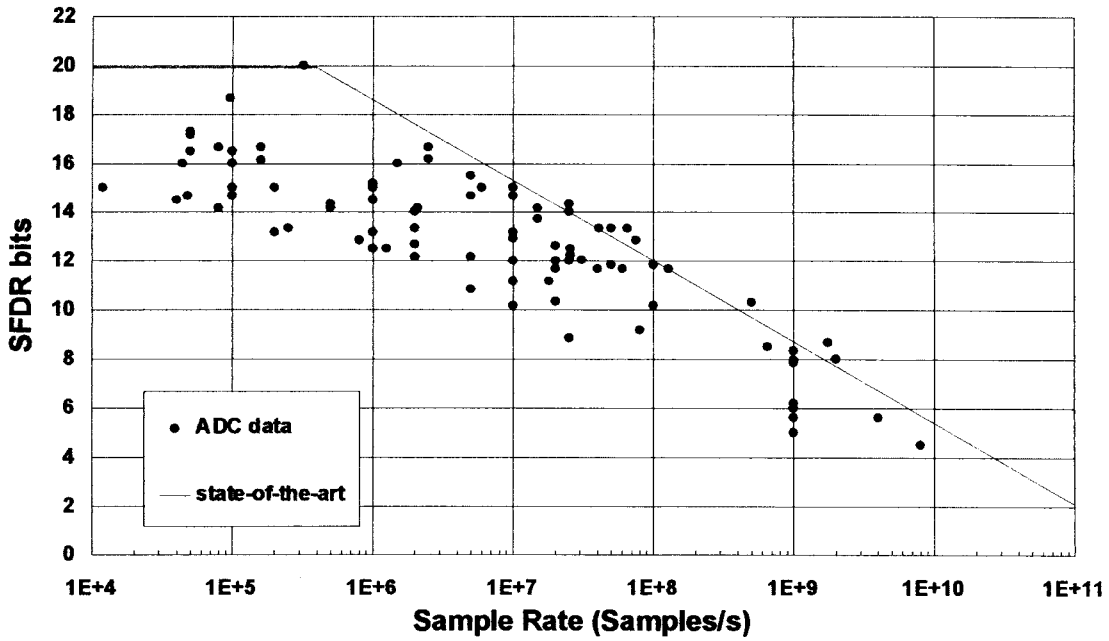


Fig. 5. Spur-free dynamic range expressed as effective number of bits according to SFDR-bits = SFDR(dBc)/6.02.

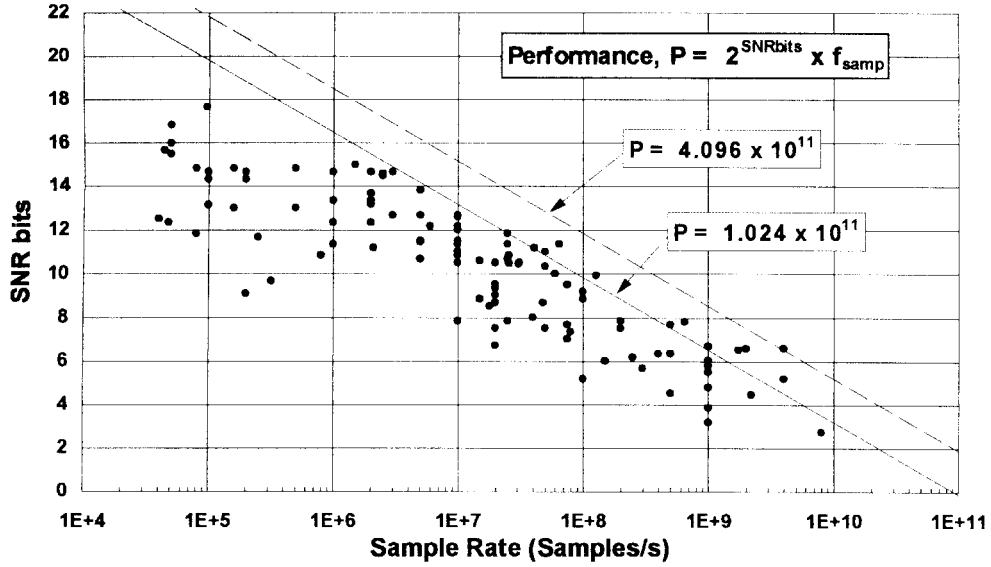


Fig. 6. Signal-to-noise ratio expressed as effective number of bits according to SNR-bits = (SNR(dB) − 1.76)/6.02. The two values of P bracket the current state of the art.

A similar graph of SNR-bits versus sample rate is shown in Fig. 6. Comparing with Fig. 1 shows that the distribution of ADC's in the SNR-bits plane is approximately 1.5 to 2 bits lower than the distribution of stated resolutions. This conclusion is consistent with Fig. 4(a). From the figure, the state-of-the-art corresponds to the range $1 \times 10^{11} < P < 4 \times 10^{11}$.

The data of Fig. 6 reveal global performance factors for the ADC population. Many factors and loss mechanisms affect ADC performance. Aside from quantization noise, three mechanisms limit achieved SNR: input-referred circuit noise (equivalent thermal noise), aperture uncertainty, and comparator ambiguity. The equations that calculate the associated maximum achievable resolutions, in SNR-bits, are

thermal noise (referred to the input:)

$$B_{\text{thermal}} = \log_2 \left(\frac{V_{FS}^2}{6kTR_{\text{eff}} f_{\text{samp}}} \right)^{1/2} - 1 \qquad (5)$$

aperture uncertainty:

$$B_{\text{aperture}} = \log_2 \left(\frac{2}{\sqrt{3}\pi f_{\text{samp}} \tau_a} \right) - 1 \qquad (6)$$

comparator ambiguity:

$$B_{\text{ambiguity}} = \frac{\pi f_T}{6.93 f_{\text{samp}}} - 1.1. \qquad (7)$$

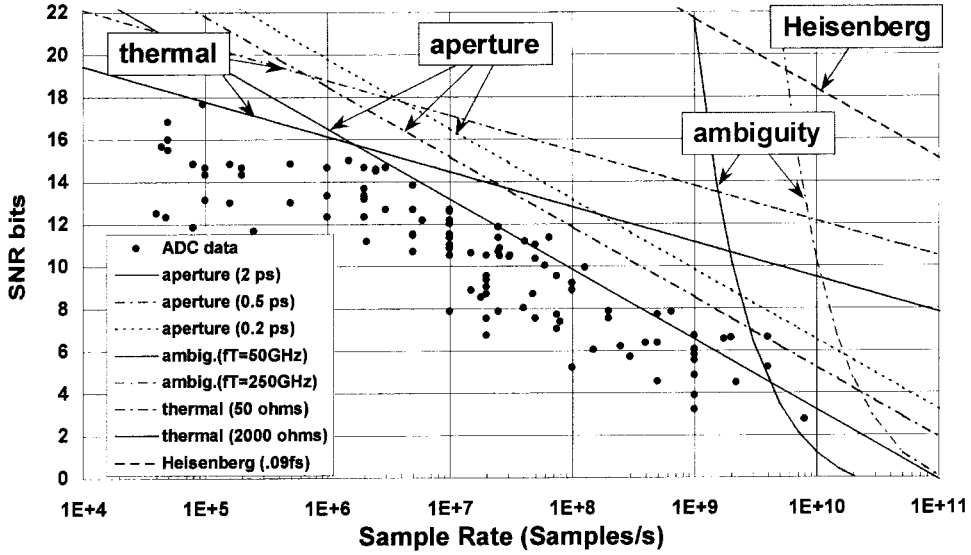


Fig. 7. Signal-to-noise ratio according to SNR-bits = (SNR(dB) − 1.76)/6.02. Three sets of curves show performance limiters due to thermal noise, aperture uncertainty, and comparator ambiguity. The Heisenberg limit is also displayed.

The derivations of these three equations are given in Appendix II. To summarize, B_{thermal} and B_{aperture} were derived by developing expressions for the noise voltages associated with thermal noise and aperture jitter, respectively and then equating each with the equivalent quantization noise $Q/\sqrt{12}$. The equivalent thermal noise resistance is denoted as R_{eff}. The rms aperture jitter is denoted as τ_a. The expression for $B_{\text{ambiguity}}$ reflects the probability that the comparator will make an ambiguous decision [7], treating the result as additive noise to the otherwise ideal quantization noise. The ambiguity probability is related to the regeneration time constant t_{reg} of the comparator. This is related to the unity-current-gain frequency of the transistors employed in the circuit. An analysis of the flash ADC in [5] indicated that $t_{\text{reg}} \sim 2.5/\pi f_T$ [8].

From these expressions SNR curves are calculated for values of input-referred thermal noise, aperture jitter, and f_T which measures comparator ambiguity. Assume $V_{FS} = 1$ V, $T = 300$ K for the thermal noise curves. Aperture jitter is calculated for Nyquist sampling, i.e., $f_{\text{sig}} = f_{\text{samp}}/2$. Comparator ambiguity is determined from the regeneration time constant of the IC technology. These are included in Fig. 7, which contains the same SNR data as Fig. 6. The current state-of-the-art is limited by the equivalent of thermal noise associated with a $\sim$2 kΩ resistor for sampling rates under 2 Ms/s. Aperture jitter, in the range 0.5 ps to 2 ps, limits SNR for the sampling frequency range of $\sim$2 Ms/s to 4 Gs/s. Comparator ambiguity is limited via the regeneration time constant corresponding to a value of $f_T \sim 50$ GHz for ADC's at the highest sampling rates. The 3-bit, 8 Gs/s Nyquist ADC [5] was fabricated with an $f_T \sim 80$ GHz InP process. The aperture uncertainty results in the -1 bit/octave slope; this is the dominant factor because the range of affected f_{samp} values is so large.

To continue to advance the state-of-the-art requires low-noise designs that achieve less than 0.5 ps of aperture uncertainty and/or technologies with $f_T \gg 50$ GHz. Experimental HBT and HEMT IC technologies have been reported that have devices with f_T and $f_{\max}$ ranging from $\sim$150 GHz to $\sim$260 GHz [9]–[11]. Hence, one can envision an eventual increase in sampling rates of a factor of two to about four beyond today's 8 Gs/s.

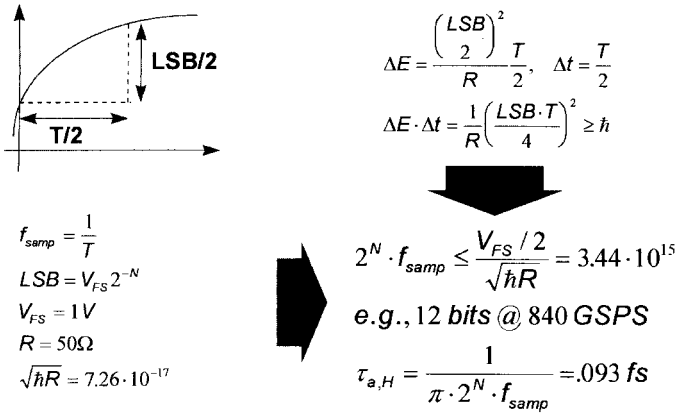


Fig. 8. Applying the Heisenberg uncertainty principle to ADC performance indicates that the ultimate limit in the resolution–sampling rate product is approximately four orders of magnitude beyond the current state of the art.

The ultimate limit to the ADC resolution-sampling rate product P, may be estimated using the Heisenberg uncertainty principle. Let $\Delta E \Delta t > h/2\pi$, where ΔE is the energy of the smallest resolvable signal, equivalent to .5 LSB, Δt is .5 sampling period $(T/2)$, and $h = 6.626\,17 \times 10^{-34}$ J-s is Planck's constant. The analysis is summarized in Fig. 8. For 50 Ω impedance and a 1 V peak-to-peak input signal, that limit is approximately four orders of magnitude beyond the state-of-the-art, which is aperture jitter limited (see the curve labeled Heisenberg in Fig. 7). There are probably other limiting factors between aperture jitter and the uncertainty principle. Although these are worthy of study, it is more urgent to develop a thorough understanding of aperture jitter.

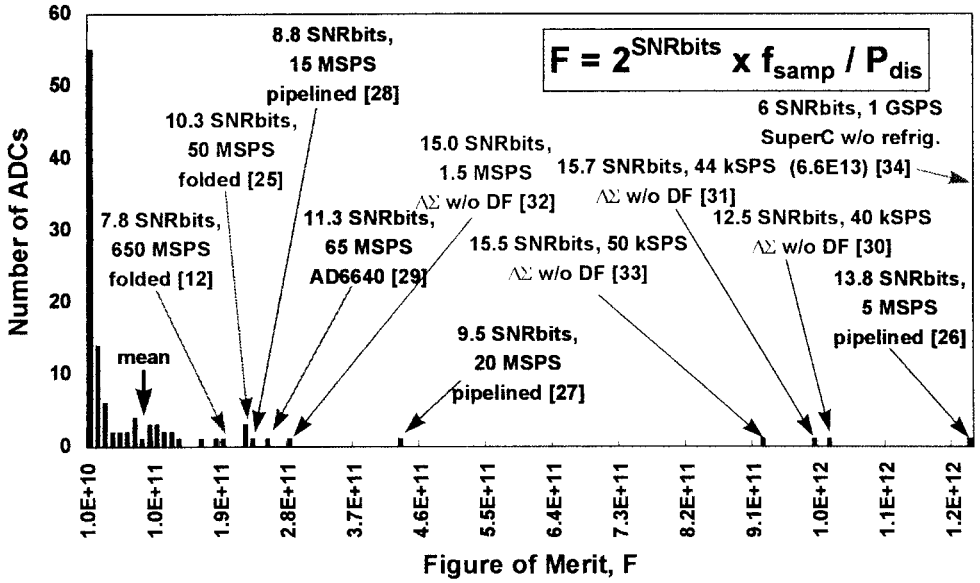


Fig. 9. Histogram of the figure of merit F. The most power-efficient ADC's have been reported within the past six years.

IV. High-Performance ADC Architectures

The ADC's of the preceding figures include architectures ranging from flash, a parallel technique, which is the fastest, through integrating which is probably the most accurate but which also is the slowest. Most of the converters have been fabricated in silicon, while a few have been realized in gallium arsenide (GaAs) and indium phosphide (InP).

The flash architecture uses $2^N - 1$ comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The fastest ADC reported is the 3-bit, 8 Gs/s Nyquist flash converter [5] cited above. This ADC had a maximum sampling rate of 14 Gs/s.

The parallelism of the flash architecture has drawbacks for high-resolution applications. The number of comparators grows exponentially with N. In addition, the separation of adjacent reference voltages grows smaller exponentially. Consequently, this architecture requires very large IC's. It has high power dissipation. It is difficult to match components in the parallel comparator channels. Finally, increasingly large input capacitance reduces analog input bandwidth. Most flash converters available today have $\leq$ 8-bit resolution. In order to overcome these problems, variations on the flash architecture have been developed which use relatively few comparators yet retain good speed. Examples capable of Gs/s rates are the folded-flash [12]–[14]; and pipelined [15], [16] architectures.

Another approach to high-speed conversion is to time-interleave two or more converters [17]. The reported ADC achieves $<$1 ps aperture jitter, but requires two hybrids, each with five LSI chips. The total P_{diss} is 40 W, roughly an order of magnitude larger than single-chip converters.

An architecture that trades speed for resolution combines delta–sigma ($\Delta\Sigma$) modulation with digital decimation filtering [18]. Delta–sigma converters sample the analog input signal at a rate which is many times the Nyquist output rate. Integration and feedback suppress the quantization noise in the lower portions of the spectrum relative to the delta–sigma clock frequency. This technique requires few analog components.

The challenge is that a high speed IC technology is needed for RF applications. Recently, near ideal performance was reported with an InP HBT second-order $\Delta\Sigma$ modulator with a sampling rate of 3.2 Gs/s and an over-sampling ratio of 32 for a Nyquist rate of 100 Ms/s [19]. This converter technology has $f_T = 70$ GHz and $f_{\max} = 90$ GHz.

Delta–sigma modulators may be designed with a bandpass characteristic [20]–[22]. This is useful when a relatively narrow band of intermediate frequencies contains the signal to be digitized. Furthermore, the center frequency of the converter is tunable. Finally, in receiver applications, down conversion stages are eliminated. Recently two bandpass delta–sigma modulators were reported with a 60 MHz center frequency [21] and an 800 MHz center frequency [22]. Both of these sample at 4 GHz. These are the fastest bandpass $\Delta\Sigma$ modulators yet built. Further discussion of bandpass sampling for RF applications can be found in [2].

V. Low-Power ADC Architectures

Another facet of ADC performance is power dissipation P_{diss}. Generally the highest performing converters also dissipate the most power. A convenient way to include P_{diss} in the performance comparison is to use the figure of merit, F, defined above. Fig. 9 shows a histogram of F for the ADC population under study. Most of the ADC's have values of $F \leq 7.9 \times 10^{10}$ (the mean).

Two fictitious examples of converter specifications that would correspond approximately to this value of F are: 1) 13 SNR-bits, 10 Ms/s, 1.1 W, and 2) 7 SNR-bits, 1 Gs/s, 1.75 W. These two examples would represent present-day state-of-the-art performance and correspond to an aperture jitter of $\sim$2 ps (see Fig. 7).

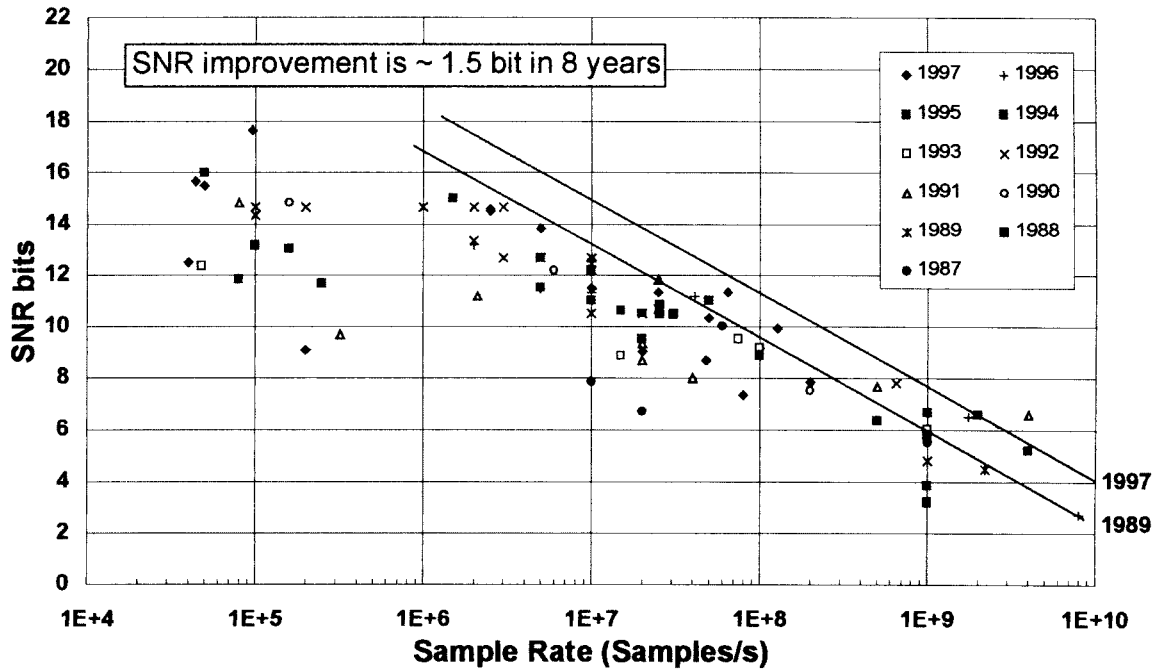


Fig. 10. Trend in SNR bits over time.

There are a few ADC's with F values significantly above 7.9×10^{10} and some of these are pointed out in the figure. These power-efficient converters utilize four architectures: flash (low resolution only) [23], [24], folded-flash [12], [25], pipelined [26]–[29], and $\Delta\Sigma$ modulation [30]–[33]. These particular $\Delta\Sigma$ modulators, in contrast to the GHz circuits mentioned above, were designed in CMOS using switched-capacitors and are oriented toward lower frequency applications. In addition, the accompanying digital decimation filters for these modulators have not been included in the power dissipation, so the actual complete ADC's will have somewhat lower values for F. The highest value of F is 6.6×10^{13}, and corresponds to a superconducting (denoted by S.C. in Fig. 1) ADC [34]. The refrigeration overhead was not included in the determination of F for this circuit. Most of these very efficient converters have been reported within the last six years.

VI. ADC Performance over Time

It is revealing to examine the trends in ADC performances during recent years. As an example, the data in Fig. 9 show that excellent progress has been made recently in developing power-efficient designs. However, the same is not true for the advancement of the resolution-speed product P. To show this, the SNR data in Fig. 6 were sorted according to the year in which the ADC's were reported. The results are given in Fig. 10, and it is evident that relatively little improvement has been made over the last six–eight years or so. From the scatter in the data it is also evident that the improvement is quite sporadic. A similar lack of advancement for SFDR-bits also holds.

If it is assumed that aperture uncertainty is the performance limiter for the best converters and if it is further assumed that all of the ADC's represented in Fig. 10 are Nyquist converters (optimistic) then, for each converter a value of τ_a can be derived from each value of P using the relation

$$\tau_a = \frac{1}{\pi\sqrt{3}P}.$$

Using this relation a graph of τ_a as a function of time (year) can be generated and is shown in Fig. 11. In this figure only the best results ($\tau_a \leq 6$ ps) are shown and the very best aperture jitter values achieved in each year are connected by a line. The scatter in the data emphasizes the sporadic nature of improvement in P, however, a least squares fit through the logs of the very best yearly data values indicates a gradual improvement over time. It can be conjectured that there may be an aperture uncertainty barrier of $\sim$0.5 ps. Some other reasons for the stagnation in ADC performance improvement may be: 1) that much of the recent research has been aimed at monolithic, and therefore, power-efficient ADC's (c.f. Fig. 9); 2) a recent and general de-emphasis on research and development; and 3) few application drivers that push the state-of-the-art. Although software radios ($\sim$100 Ms/s) and satellite communications ($>$1 Gs/s) may provide the incentives for a breakthrough.

VII. Summary

The state-of-the-art for ADC's has been reviewed and analyzed. Data for SNR and SFDR as functions of $f_{\rm samp}$ has been discussed. The SNR data show that converter performance is limited by input-referred noise, aperture uncertainty and comparator ambiguity. The best results have been achieved for flash, folded-flash, pipelined, and time-interleaved architectures.

It is clear from the data presented above, that in order to improve upon the present state-of-the-art in ADC performance, significant technical challenges must be met. Specifically 1) a reduction in aperture uncertainty to well below 1 ps, 2) an

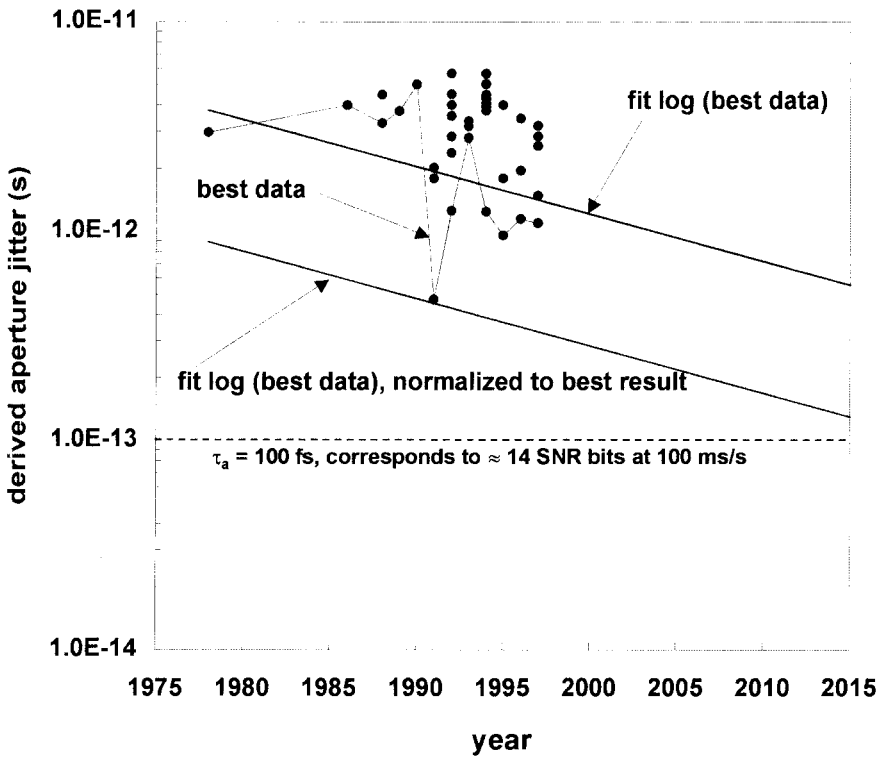


Fig. 11. Derived aperture jitter for the best ADC performances as a function of the year of introduction. Converter performances are gradually improving, although actual progress is sporadic.

increase in the maximum sampling frequency to beyond 8 Gs/s, and 3) accomplishing both 1) and 2) while maintaining low power consumption, e.g., < 5 W.

With respect to aperture uncertainty, only about 1.5 bits of overall improvement has been achieved over the last six–eight years in SNR (and only one bit in SFDR). The best effort was the time-interleaved ADC which achieved $\tau_a < 1$ ps [17]. In addition, while significant progress has been made in achieving power-efficient ADC designs (high F), none of these efforts has gone below $\sim$0.5–2 ps of aperture jitter.

APPENDIX I

See Table I.

APPENDIX II

This appendix contains the derivation of the three equations which calculate the maximum ADC resolutions in SNR-bits for input-referred thermal noise, aperture uncertainty, and, comparator ambiguity. The first two equations are obtained by developing expressions for the noise voltage due to each mechanism and then equating to an equivalent quantization noise. The ambiguity equation is developed by generating an expression for the probability that an ambiguous decision will be made by a particular comparator, then summing the probabilities for all comparators, then adding the resulting noise to an otherwise ideal quantization noise voltage. All three equations are developed as if each error (thermal, aperture, ambiguity) is acting alone.

Thermal Noise Derivation: The spectral noise density seen at the ADC input consists of various contributions such as thermal noise, shot noise, $1/f$ noise, and input-referred noise. The thermal and shot components are white while the $1/f$ and input-referred components are frequency dependent. The resulting input-referred noise voltage is obtained by integrating these spectra over the full-Nyquist band $f_{\rm samp}/2$ and can be expressed as

$$\langle v_n^2 \rangle = 4kTR_{\rm eff} f_{\rm samp}/2$$

where k is Boltzmann's constant $= 1.380658 \times 10^{-23}$ J/K, $T =$ temperature in K (assumed $= 300$ K in Fig. 7), and $R_{\rm eff}$ is an effective thermal resistance which lumps together the effects of all noises. The equivalent quantization noise voltage is given by

$$\langle v_Q^2 \rangle = \frac{Q^2}{12} = \frac{V_{FS}^2 2^{-2B_{\rm thermal}}}{12}$$

where $B_{\rm thermal}$ is the maximum resolution in SNR-bits (for a given value of $R_{\rm eff}$). Equating these two expressions leads directly to the desired result

$$B_{\rm thermal} = \log_2 \left(\frac{V_{FS}^2}{6kTR_{\rm eff} f_{\rm samp}} \right)^{1/2} - 1.$$

Aperture Uncertainty Derivation: This effect comes about because an ADC does not sample the input signal at precisely equal time-intervals, $T = 1/f_{\rm samp}$. Instead the sampling process can be characterized by a mean and a standard deviation with regard to the location in time of when sampling

TABLE I

Institution	Author/Part No.	Year	fsamp(Hz)	Stated Bits	SNRbits	SFDRbits	Pdiss(W)	P(LSBs-Hz)	F(LSBs-Hz/W)	Derived τa	Vinput(V)	BWinput(Hz)
Crystal	CS5506	1990	2.00E+01	20								
Analog Devices	AD1175		2.00E+01	22	21.8	22.2		7.31E+07		2.52E-09		
Crystal	CS5324		1.00E+03	20								
UC Berkeley	Lee, et al.	1984	1.20E+04	15		15.0	0.02					
Harris	ICL 7115		2.50E+04	14								
Analogic	ADC 20048		3.00E+04	18								
TI & Waterloo	Chen & Leung	1997	4.00E+04	14	12.5	14.5	0.00023	2.31E+08	1.01E+12	7.94E-10	2.0	
van der Zwan	Philips Research	1997	4.41E+04	16	15.7	16.0	0.0023	2.27E+09	9.89E+11	8.08E-11		2.0E+04
TI & Vitesse	Fattaruso, et al.	1993	4.80E+04	15	12.3	14.7	0.1	2.48E+08	2.48E+09	7.42E-10		2.4E+04
Stanford	Rabbii & Wooley	1997	5.00E+04	16	15.5	16.5	0.0025	2.30E+09	9.19E+11	8.00E-11	3.2	
Fujitsu	MB87020		5.00E+04	16						3.68E-06		
Stanford	Williams & Wooley	1994	5.00E+04	17	16.0	17.3	0.047	3.25E+09	6.91E+10	5.66E-11		2.5E+04
Analog Devices	AD1879		5.00E+04	18	16.0	17.2	0.9	3.25E+09	3.61E+09	5.66E-11	6.0	2.2E+04
Analog Devices	Adams	1989	5.00E+04	18								
Hitachi	Matsumoto, et al.	1988	5.00E+04	18								
Analogic	ADC5120		5.00E+04	20	16.8	17.3	2.38	5.77E+09	2.43E+09	3.18E-11	10.0	1.4E+05
Bell Northern R	Longo, et al.	1988	8.00E+04	13	11.8	14.2	0.02	2.92E+08	1.46E+10	6.29E-10		
GE + Yokogawa	Ribner, et al.	1991	8.00E+04	15	14.8	16.7		2.32E+09		7.92E-11		
Leung, et al,	Crystal Semic.	1997	9.60E+04	20	17.6	18.7	0.76	1.97E+10	2.59E+10	9.32E-12	4.0	2.2E+04
Analog Devices	Fernandes, et al.	1988	1.00E+05	14	13.1	15.0	0.48	8.96E+08	1.87E+09	2.05E-10	10.0	6.0E+05
Motorola	DSP56ADC16	1992	1.00E+05	16	14.7	14.7	0.3	2.58E+09	8.62E+09	7.11E-11	3.5	5.0E+04
Micro Networks	MN6500	1992	1.00E+05	16	14.3	16.0	0.685	2.05E+09	3.00E+09	8.95E-11	10.0	5.0E+04
Analog Devices	AD1876		1.00E+05	16	14.7	16.5	0.235	2.58E+09	1.10E+10	7.11E-11	10.0	1.0E+06
Crystal	CS5126		1.00E+05	16								
Atmel	AT76		1.00E+05	18	14.7		1	2.58E+09	2.58E+09	7.11E-11	1.0	
AT&T Bell L	Norsworthy, et al.	1988	1.60E+05	13	13.0	16.7	0.075	1.31E+09	1.74E+10	1.41E-10		
Motorola	Rebeschini, et al.	1990	1.60E+05	16	14.8	16.2	0.076	4.64E+09	6.11E+10	3.96E-11		8.0E+04
Swiss Federal Institute	Hammerschmied, Huang	1997	2.00E+05	10	9.1	13.2	0.012	1.09E+08	9.10E+09	1.68E-09		
Analogic	ADC4357		2.00E+05	16	14.7	15.0	2.2	5.17E+09	2.35E+09	3.55E-11	10.0	
Burr-Brown	PCM78		2.00E+05	16	14.3			4.11E+09		4.48E-11	6.0	
Burr-Brown	PCM1750	1992	2.00E+05	18	14.7	15.0	0.21	5.17E+09	2.46E+10	3.55E-11	5.5	5.0E+05
UC Berkeley	Sutarja, et al.	1988	2.50E+05	13	11.7	13.3	0.015	8.13E+08	5.42E+10	2.26E-10		
Micro Networks	MN5420	1991	3.20E+05	12	9.7	20.0	6.5	2.61E+08	4.02E+07	7.03E-10		
Sipex	SP9478		5.00E+05	14								
Alcatel	Mietec (ISSCC)		5.00E+05	14								
Analog Devices	AD1382		5.00E+05	16	14.8	14.2	2.8	1.45E+10	5.18E+09	1.27E-11	10.0	2.0E+05
Datel	ADS 930		5.00E+05	16	13.0	14.3	3.4	4.09E+09	1.20E+09	4.50E-11	10.0	2.0E+06
Analog Devices	AD7886		8.00E+05	12	10.8	12.8	0.25	1.46E+09	5.85E+09	1.26E-10	5.0	1.0E+06
Harris	ICL 7135		9.00E+05	14								
Datel	ADS 112		1.00E+06	12	11.3	12.5	1.3	2.58E+09	1.99E+09	7.11E-11	10.0	1.0E+07
Univ. of Illinois	Song, et al.	1988	1.00E+06	12		13.2	0.4					
Analog Devices	AD7586		1.00E+06	12			0.2				4.0	
Datel	ADS941		1.00E+06	14	12.3	14.5	2.8	5.16E+09	1.84E+09	3.56E-11	10.0	6.0E+06
MIT & Harris	Karanicolas, et al.	1993	1.00E+06	15		15.0	1.8					
Analogic	ADC 4344		1.00E+06	16	13.3	15.2	3.4	1.03E+10	3.03E+09	1.79E-11	5.0	4.0E+06
Edge Technology	ET1661	1992	1.00E+06	16	14.7		5.5	2.58E+10	4.70E+09	7.11E-12	10.0	
Sipex	SP9490		1.00E+06	16								
Analog Devices	Mercer	1991	1.25E+06	12		12.5	0.6				5.0	8.5E+06
Katholieke Univ. Leuven	Yin & Sansen	1994	1.50E+06	16	15.0	16.0	0.18	4.88E+10	2.71E+11	3.76E-12	0.7	7.5E+05
Signetics	Kolluri	1989	2.00E+06	12		12.2	0.65				10.0	
Analogic	ADC3110		2.00E+06	14	13.7	12.7	4.1	2.59E+10	6.32E+09	7.09E-12	10.0	2.0E+07
Datel	ADS942		2.00E+06	14	12.3	13.3	2.9	1.03E+10	3.56E+09	1.78E-11	10.0	6.0E+06
Datel	ADS932	1996	2.00E+06	16	13.2	14.0	1.85	1.83E+10	9.91E+09	1.00E-11	5.5	4.0E+06
Edge Technology	ET1662	1992	2.00E+06	16	14.7		5.5	5.17E+10	9.40E+09	3.55E-12	10.0	
Analog Devices	AD1388	1992	2.00E+06	16	13.3		6.5	2.06E+10	3.17E+09	8.93E-12	10.0	9.0E+06
Stanford	Brandt, et al.	1991	2.10E+06	12	11.2	14.2	0.041	4.84E+09	1.18E+11	3.80E-11		1.0E+06
Analog Devices	Brooks, et al.	1997	2.50E+06	16	14.5	16.2	0.55	5.76E+10	1.05E+11	3.19E-12		
Analog Devices	AD9260	1997	2.50E+06	16	14.6	16.7	0.6	6.10E+10	1.02E+11	3.01E-12		1.3E+06
Edge Technology	ET1463	1992	3.00E+06	14	12.7		2.17	1.95E+10	8.98E+09	9.44E-12	2.0	
Edge Technology	ET1663	1992	3.00E+06	16	14.7		5.5	7.75E+10	1.41E+10	2.37E-12	10.0	
Raytheon	was Hughes	1978	4.00E+06	12								
Datel	ADS 118		5.00E+06	12	10.7	10.8	1.9	8.15E+09	4.29E+09	2.25E-11	2.0	6.5E+07
UC Berkeley	Cline & Gray	1996	5.00E+06	13	11.5	12.2	0.166	1.40E+10	8.44E+10	1.31E-11	6.6	5.0E+07
Burr-Brown	ADC614	1994	5.00E+06	14	12.7	14.7	6.1	3.25E+10	5.32E+09	5.66E-12	2.5	3.0E+07
Datel	ADS944	1994	5.00E+06	14	11.5		3.37	1.45E+10	4.30E+09	1.27E-11	2.5	
Edge Technology	ET1465	1992	5.00E+06	14	12.7		2.17	3.25E+10	1.50E+10	5.66E-12	2.0	
Univ of Illinois, Harris	Kwak et al.	1997	5.00E+06	15	13.8	15.5	0.06	7.18E+10	1.20E+12	2.56E-12		
Raytheon	Boyko, GSG	1990	6.00E+06	15	12.2	15.0	22	2.76E+10	1.25E+09	6.66E-12		
Raytheon	was Hughes	1984	1.00E+07	8	7.8	10.2	0.4	2.30E+09	5.76E+09	7.98E-11		
TRW	THC1202		1.00E+07	12	10.8	11.2	4.5	1.83E+10	4.07E+09	1.00E-11	2.0	7.0E+07

(a)

occurs. The mean is the average position of the sampling time and the standard deviation is a measure of the variation of the sampling point and is defined as the rms aperture jitter, τ_a. Assuming that τ_a is known, an expression for the voltage error due to τ_a can be derived. The worst case situation corresponds to sampling a sinusoidal waveform with the highest frequency in the Nyquist band, which is $f_{\rm samp}/2$, i.e., $v(t) = (V_{FS}/2)\ sin(\pi f_{\rm samp} t)$. The maximum rms voltage error will occur when attempting to sample the sinusoid at its zero-crossing, and is given by the product of the maximum slope of the wave and the aperture uncertainty

$$v_{\rm rms} = \pi f_{\rm samp} V_{FS} \tau_a / 2.$$

Equating this to the square root of the expression for $\langle v_Q^2 \rangle$ given above (here $B_{\rm thermal}$ is replaced by $B_{\rm aperture}$), leads to

TABLE I *(Continued.)*

Institution	Author/Part No.	Year	fsamp(Hz)	Stated Bits	SNRbits	SFDRbits	Pdiss(W)	P(LSBs-Hz)	F(LSBs-Hz/W)	Derived τa	Vinput(V)	BWinput(Hz)
Datel	ADS130		1.00E+07	12	10.5	11.2	3.85	1.45E+10	3.77E+09	1.26E-11	2.5	6.5E+07
Burr Brown	ADC603	1992	1.00E+07	12	10.5	12.0	6.1	1.45E+10	2.38E+09	1.26E-11	2.5	4.0E+07
Analog Devices	AD9220	1996	1.00E+07	12	11.3	12.9	0.28	2.58E+10	9.23E+10	7.11E-12		3.5E+07
Analog Devices	AD9220	1997	1.00E+07	12	11.5	14.7	0.25	2.90E+10	1.16E+11	6.34E-12		6.0E+07
TI + Army	Hamlett, et al.	1990	1.00E+07	12			1.6					
Univ. of Illinois	Shu et al.	1995	1.00E+07	13	11.0		0.36	2.05E+10	5.70E+10	8.95E-12		
Datel	ADS945	1994	1.00E+07	14	12.0	13.2	4.2	4.10E+10	9.75E+09	4.49E-12	2.5	5.0E+07
Analog Devices	AD9014	1992	1.00E+07	14	12.2	14.7	12.8	4.60E+10	3.59E+09	4.00E-12	2.0	6.0E+07
Analog Devices	AD9240	1997	1.00E+07	14	12.6	15.0	0.285	6.13E+10	2.15E+11	3.00E-12		7.0E+07
Edge Technology	ET1471	1992	1.00E+07	14	12.7		5.7	6.49E+10	1.14E+10	2.83E-12	2.0	
Harris	CA 3318C		1.50E+07	8								
Matsushita	Kusumoto, et al.	1993	1.50E+07	10	8.8		0.03	6.89E+09	2.30E+11	2.67E-11		3.0E+06
Raytheon	was Hughes	1986	1.50E+07	11		14.2	90					
Comlinear	CLC935B	1994	1.50E+07	12	10.6	13.7	4.75	2.34E+10	4.92E+09	7.87E-12	2.0	8.0E+07
Analog Devices	AD773		1.80E+07	10	8.5	11.2	1.2	6.57E+09	5.47E+09	2.80E-11	1.0	1.0E+08
Raytheon	was Hughes	1986	2.00E+07	7	6.7		0.64	2.10E+09	3.29E+09	8.73E-11		
Harris	HI 5700		2.00E+07	8	7.5			3.66E+09		5.02E-11		9.0E+06
Datel	ADC208		2.00E+07	8								
Analog Devices	AD9200	1997	2.00E+07	10	9.0	10.3	0.08	1.03E+10	1.29E+11	1.78E-11	2.0	9.0E+07
Analog Devices	Real, et al.	1991	2.00E+07	10	8.7	10.3	1	8.19E+09	8.19E+09	2.24E-11		1.5E+08
Univ. of Cal. Berk.	Cho & Gray	1995	2.00E+07	10	9.5		0.035	1.47E+10	4.21E+11	1.25E-11	2.0	
Sig Proc Tech	SPT7912	1991	2.00E+07	12	9.3	11.7	1.8	1.30E+10	7.21E+09	1.42E-11	2.0	1.2E+08
HP	Jewett, et al.	1992	2.00E+07	12	10.5	12.0	3.5	2.91E+10	8.30E+09	6.32E-12		9.5E+07
Comlinear	CLC936C	1994	2.00E+07	12	10.5	12.6	5.28	2.91E+10	5.50E+09	6.32E-12	2.0	9.0E+07
Raytheon	was Hughes	1982	2.00E+07	12								
Analog Devices	CAV1220		2.00E+07	12			20					
TRW	TAC1025		2.50E+07	10	7.8	8.8	7.8	5.76E+09	7.38E+08	3.19E-11	1.0	6.0E+07
Analog Devices	AD9032	1992	2.50E+07	12	10.7	12.0	5	4.08E+10	8.15E+09	4.51E-12	2.0	1.0E+07
Analog Devices	AD9225	1997	2.50E+07	12	11.3	14.3	0.3	6.46E+10	2.15E+11	2.84E-12		2.0E+08
Raytheon	was Hughes	1991	2.50E+07	14	11.8	14.0	30	9.13E+10	3.04E+09	2.01E-12		
Comlinear	CLC937B`	1994	2.56E+07	12	10.5	12.2	7.35	3.64E+10	4.95E+09	5.06E-12	2.0	1.0E+08
Comlinear	CLC950	1994	2.56E+07	12	10.8	12.5	2	4.68E+10	2.34E+10	3.92E-12	2.0	1.8E+08
Comlinear	CLC938C`	1994	3.07E+07	12	10.4	12.0	6.57	4.26E+10	6.49E+09	4.31E-12	2.0	1.0E+08
Analog Devices	AD9026	1994	3.10E+07	12	10.5		1.46	4.50E+10	3.09E+10	4.08E-12	2.0	
Sony	CXD1179Q		3.50E+07	8			0.1				1.8	
Sig Proc Tech	SPT7824	1991	4.00E+07	10	8.0	11.7	1.8	1.03E+10	5.74E+09	1.78E-11	1.8	1.2E+08
Analog Devices	AD9042	1996	4.10E+07	12	11.2	13.3	0.595	9.44E+10	1.59E+11	1.95E-12		1.4E+09
Broadcom Corp., UCLA	Bult, et al.	1997	4.80E+07	10	8.7		0.24	1.97E+10	8.19E+10	9.35E-12	2.0	3.2E+07
Raytheon	was Hughes	1989	5.00E+07	7			0.5					
Philips Research Labs	Van de Plaasche	1979	5.00E+07	7								
TRW	TDC1025		5.00E+07	8	7.5			9.15E+09		2.01E-11	2.0	1.3E+07
Datel	ADC9060		5.00E+07	10								
Philips Components, FR	Vorenkamp, Roovers	1997	5.00E+07	12	10.3	11.8	0.3	6.48E+10	2.16E+11	2.84E-12		2.6E+05
Analog Devices	Murden & Gosser	1995	5.00E+07	12	11.0	13.3	0.575	1.03E+11	1.78E+11	1.79E-12	1.0	2.0E+08
Raytheon	was Hughes	1978	6.00E+07	13	10.0	11.7	25	6.17E+10	2.47E+09	2.98E-12		3.0E+07
Analog Devices	AD6640	1997	6.50E+07	12	11.3	13.3	0.695	1.68E+11	2.42E+11	1.09E-12		2.5E+07
Sony	CXA1386P		7.50E+07	8	7.0		0.58	9.71E+09	1.67E+10	1.89E-11		1.5E+08
UCLA	Colleran & Abidi	1993	7.50E+07	10	9.5	12.8	0.8	5.46E+10	6.83E+10	3.36E-12		5.0E+07
Analog Devices	AD9060		7.50E+07	10	7.7		2.8	1.54E+10	5.50E+09	1.19E-11	4.0	1.8E+08
Analog Devices	AD9057-80	1997	8.00E+07	8	7.3	9.2	0.175	1.30E+10	7.45E+10	1.41E-11	2.5	1.2E+08
TRW	TDC1029		1.00E+08	6	5.2			3.65E+09		5.04E-11	1.0	5.0E+07
Philips Research Labs	Van de Plaasche	1988	1.00E+08	8			0.8				1.0	4.0E+07
NEC	Sone, et al.	1993	1.00E+08	10	9.2	10.2	0.95	5.78E+10	6.09E+10	3.18E-12		1.5E+07
Analog Devices	AD9070	1997	1.00E+08	10	9.2		0.7	5.78E+10	8.26E+10	3.18E-12		2.3E+08
Raytheon	was Hughes	1994	1.00E+08	10			1.8					
HRL Labs	Jensen, et al.	1995	1.00E+08	12	8.8	11.8	1	4.59E+10	4.59E+10	4.00E-12		
Hewlett Packard	Jewett, et al.	1997	1.28E+08	12	9.9	11.7	5.7	1.24E+11	2.18E+10	1.48E-12	0.5	2.5E+08
Sig Proc Tech	HADC77100		1.50E+08	8	6.0		2.6	9.73E+09	3.74E+09	1.89E-11	2.0	1.8E+08
Analog Devices	AD9054-200	1997	2.00E+08	8	7.8		0.5	4.61E+10	9.21E+10	3.99E-12		3.8E+08
Analog Devices	Mangelsdorf	1990	2.00E+08	8	7.5		2	3.66E+10	1.83E+10	5.02E-12		4.0E+08
Raytheon	was Hughes	1982	2.50E+08	5			2.2					
Sony	CXA1176K		2.50E+08	8	6.2		1.4	1.82E+10	1.30E+10	1.01E-11		2.5E+08
NTT LSI Lab	Akazawa, et al.	1987	3.00E+08	8								
Analog Devices	AD9028		3.00E+08	8	5.7		2.2	1.55E+10	7.03E+09	1.19E-11	2.0	2.5E+08
Matsushita		1992	3.00E+08	10			4					
Sony	CXA1276K		4.00E+08	8	6.4		3.1	3.27E+10	1.05E+10	5.62E-12		2.5E+08

(b)

the desired relation for B_{aperture}

$$B_{\text{aperture}} = \log_2\left(\frac{2}{\sqrt{3}\pi f_{\text{samp}}\tau_a}\right) - 1.$$

Comparator Ambiguity Derivation: This effect is due to the finite speed with which the transistors in the comparators are able to respond to a (small) voltage difference ($\sim$.5 LSB). The probability that the ith comparator will produce an ambiguous decision as to whether the input signal is above or below the reference voltage associated with said comparator is given by [7]

$$P_i = \frac{V_{FS}e^{-t/\tau_{\text{reg}}}}{A_0 Q}$$

where $t = .5$ clock period $= (2f_{\text{samp}})^{-1}$, τ_{reg} = regeneration time constant $= 2.5/\pi f_T$ [8], A_0 = comparator gain, and Q is the effective LSB voltage $= V_{FS}2^{-B_{\text{ambiguity}}}$. Making the implied substitutions yields

$$P_i = \frac{e^{-\pi f_T/5f_{\text{samp}}}}{A_0 2^{-B_{\text{ambiguity}}}}.$$

TABLE I *(Continued.)*

Institution	Author/Part No.	Year	fsamp(Hz)	Stated Bits	SNRbits	SFDRbits	Pdiss(W)	P(LSBs-Hz)	F(LSBs-Hz/W)	Derived ;a	Vinput(V)	BWinput(Hz)
TRW	L. Tran et al.	1993	5.00E+08	4			1					2.5E+08
Analog Devices	AD9006		5.00E+08	6	4.5		2	1.15E+10	5.76E+09	1.60E-11	2.0	5.5E+08
Micro Networks	MN6900	1991	5.00E+08	8	7.7	10.3	7.5	1.03E+11	1.37E+10	1.79E-12	0.5	1.2E+09
Raytheon	was Hughes	1988	5.00E+08	8	6.4		11	4.08E+10	3.71E+09	4.50E-12		2.5E+08
Raytheon	was Hughes	1984	5.20E+08	6			4.1					
Raytheon	was Hughes	1986	6.00E+08	4			1.8					
Philips, Netherl	van Valburg,et al.	1992	6.50E+08	8	7.8	8.5	0.81	1.46E+11	1.81E+11	1.26E-12	2.0	1.5E+08
Raytheon	was Hughes	1986	8.00E+08	6			7.9					3.5E+08
HRL Labs	W. & Schmitz, HRL	1988	1.00E+09	4	3.2	5.0	0.1	9.16E+09	9.16E+10	2.01E-11	1.4	1.0E+07
Inst. fur Electr., Ruhr Uni	Daniel et al.	1988	1.00E+09	4	3.9	6.0	2.4	1.45E+10	6.05E+09	1.27E-11	1.3	8.0E+08
TRW & Honeywell	Kleks et al.	1987	1.00E+09	4								1.0E+09
TRW	Oki et al.	1987	1.00E+09	4			2.25					5.0E+08
Rockwell	Wang et al.	1987	1.00E+09	4			0.6					
Fraunhofer & TriQuint	Hagelauer et al.	1992	1.00E+09	5	4.8	5.6	3.4	2.80E+10	8.24E+09	6.56E-12	1.8	5.0E+08
Raytheon	was Hughes	1986	1.00E+09	6	5.5	6.2	2.6	4.59E+10	1.77E+10	4.00E-12		5.0E+08
NTT LSI Lab	Wakimoto, et al.	1988	1.00E+09	6	5.8	8.3	2	5.59E+10	2.79E+10	3.29E-12	2.0	1.7E+09
Signal Processing Tech	SPT7760A	1995	1.00E+09	8	6.7	7.8	5.5	1.03E+11	1.87E+10	1.79E-12	2.0	9.0E+08
HYPRES	Stebbins & Bradley	1993	1.00E+09	8	6.0	8.0	0.001	6.56E+10	6.56E+13	2.80E-12	0.3	
Raytheon	was Hughes	1989	1.20E+09	5			3					
TRW	B. Wong, et al	1996	1.75E+09	8	6.5	8.7		1.60E+11		1.15E-12		3.0E+09
Rockwell	Nary et al.	1995	2.00E+09	8	6.6	8.0	5.3	1.92E+11	3.62E+10	9.57E-13	0.6	3.0E+09
Lab d'Electr & de Phys A	DuCourant, et al.	1989	2.20E+09	5	4.5		1.05	4.89E+10	4.66E+10	3.76E-12		4.0E+08
Lab d'Electr & de Phys A	DuCourant, et al.	1986	3.00E+09	4			0.15					
HP & Rockwell	Poulton(HP),Wang(R).	1994	4.00E+09	6	5.2	5.6	5.7	1.48E+11	2.59E+10	1.24E-12		1.8E+09
Hewlett Packard	Schiller & Byrne	1991	4.00E+09	8	6.6		39	3.88E+11	9.96E+09	4.73E-13		
HRL Labs	Baringer, et al.	1996	8.00E+09	3	2.7	4.5	3.5	5.31E+10	1.52E+10	3.46E-12	0.6	1.2E+10

(c)

An equation for the quantization noise plus the contributions from all comparators due to the ambiguity probabilities is [7]

$$\langle v_{Q^+}^2 \rangle = \frac{Q^2}{12}\left(1 + P_i(2^N)\right)$$

where 2^N is the number of comparators in the ADC which holds for a flash converter with one overflow comparator (this is the fastest architecture). Substituting for P_i and defining the quantity $\Delta N = N - B_{\text{ambiguity}}$ gives

$$\langle v_{Q^+}^2 \rangle = \frac{Q^2}{12}\left(1 + \frac{2^{\Delta N}}{A_0}\, e^{-\pi f_T/5f_{\text{samp}}}\left(2^{2B_{\text{ambiguity}}}\right)\right).$$

The second term in the parentheses can be considered as an excess noise and can be equated with a fraction, α, of the quantization noise, i.e.,

$$\alpha = \frac{2^{\Delta N}}{A_0}\, e^{-\pi f_T/5f_{\text{samp}}}\left(2^{2B_{\text{ambiguity}}}\right).$$

Solving for $B_{\text{ambiguity}}$ yields the following:

$$B_{\text{ambiguity}} = \frac{\pi f_T}{10\,\ln 2 f_{\text{samp}}} + \frac{1}{2}\left(\log_2(\alpha A_0) - \Delta N\right).$$

If the following assumptions are made: 1) the additive term should be no more than .5 LSB, then $\alpha = .25$, 2) a value for $A_0 = 2.5$ [5], and 3) $\Delta N = 1.5$ [see Fig. 4(a)], then the final expression for $B_{\text{ambiguity}}$ is obtained

$$B_{\text{ambiguity}} = \frac{\pi f_T}{6.93 f_{\text{samp}}} - 1.1.$$

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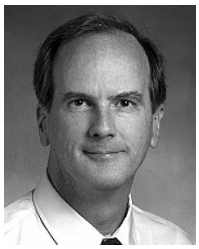

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