"The figures of merit (FoMs) encompassing power, effective resolution and speed rank the dynamic performance of the ADC core among the best in its class."

J. Bjørnsen:
Design of a High-speed, High-resolution ADC for Medical Ultrasound Applications - *Highlights and summary*

ENOB of state-of-the-art ADCs

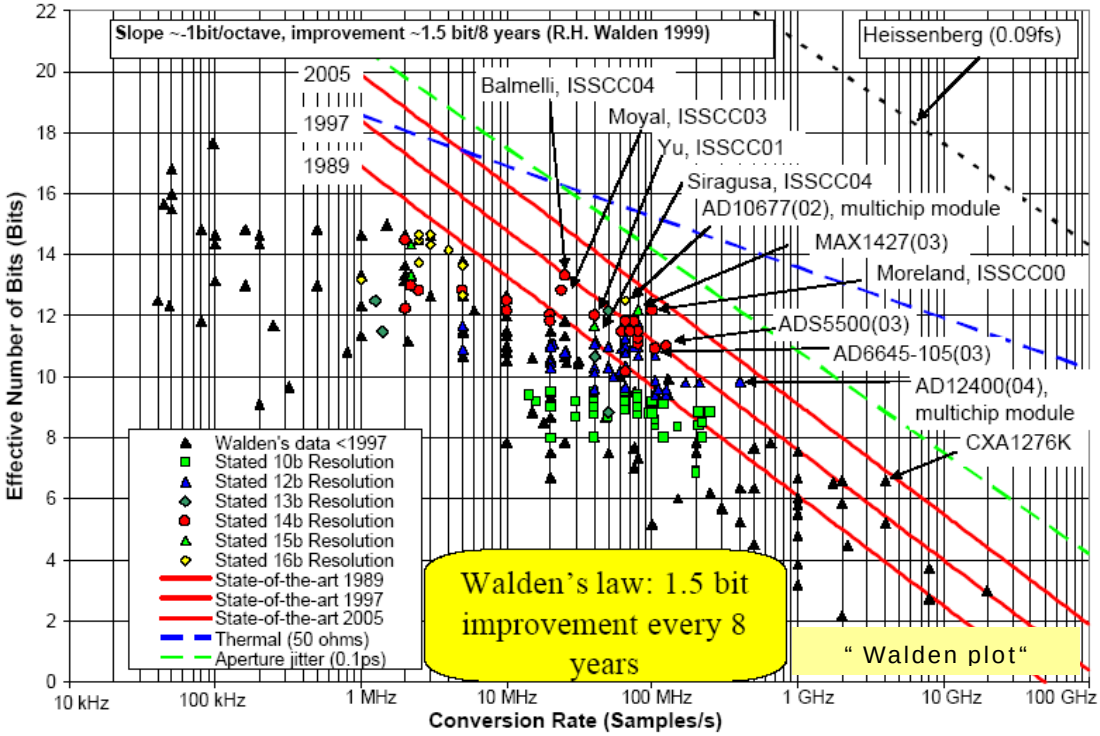
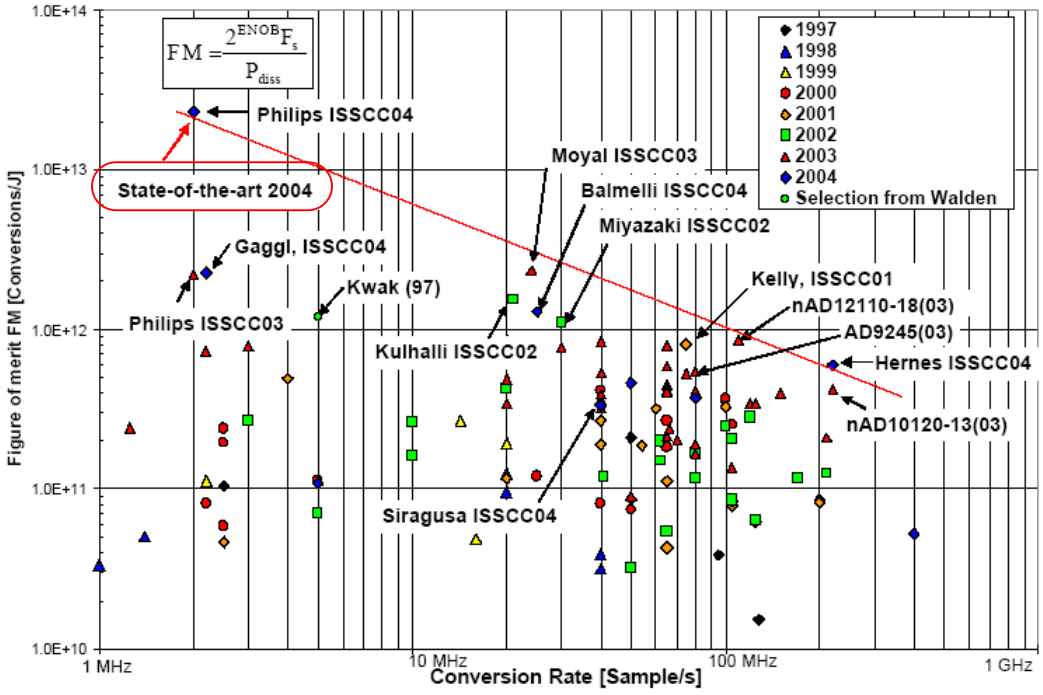


Figure of merit for state-of-the-art ADCs

FOM$_1$



High-Speed Analog-to-Digital Converter Survey

Kent H. Lundberg

1 Quantization Energy Figure of Merit

FOM

The analog program committee of the IEEE International Solid-State Circuits Conference suggested a figure of merit for A/D converters that takes into account power dissipation, resolution, and sampling rate [1]. It has units of energy, and represents the energy used per conversion step

$$E = \frac{P}{2^N F_S} \qquad \Rightarrow \; E_{\text{conv}}$$

where P is the power dissipation, N is the stated number of bits, and F_S is the sampling rate. This quantity is nearly the inverse of a similar figure of merit suggested earlier by Robert Walden [2, 3] that uses the *effective* number of bits (ENOB), B, instead of the stated number of bits

$$\text{FM} \; \Leftarrow \qquad F = \frac{2^B F_S}{P}$$

Walden's figure of merit F correctly includes the performance limitation of signal-to-noise-and-distortion ratio (SNDR), but still produces optimistic results for some A/D converters[1]. In most applications, A/D converters are expected to faithfully convert all input-signal frequencies below the Nyquist frequency (one half of the sampling rate F_S), but many A/D converters exhibit severe degradation of SNDR at frequencies well below the Nyquist frequency. For this reason, the literature has recently started using the effective resolution bandwidth (ERBW) instead of the sampling rate in the equation for the figure of merit [4, 5]. This figure of merit is known as the "quantization energy"

$$E_Q = \frac{P}{2^B (2F_{BW})}$$

where P is the power dissipation, B is the high-frequency ENOB (calculated from SNDR), and F_{BW} is either the effective resolution bandwidth or the Nyquist frequency, which ever is less.

...

[1] Hopeless pedants, like this author [6], also complain about its nonsensical units of "inverse joules."

[1] Frank Goodenough. Analog technology of all varieties dominate ISSCC. *Electronic Design*, 44(4):96–111, February 19, 1996.

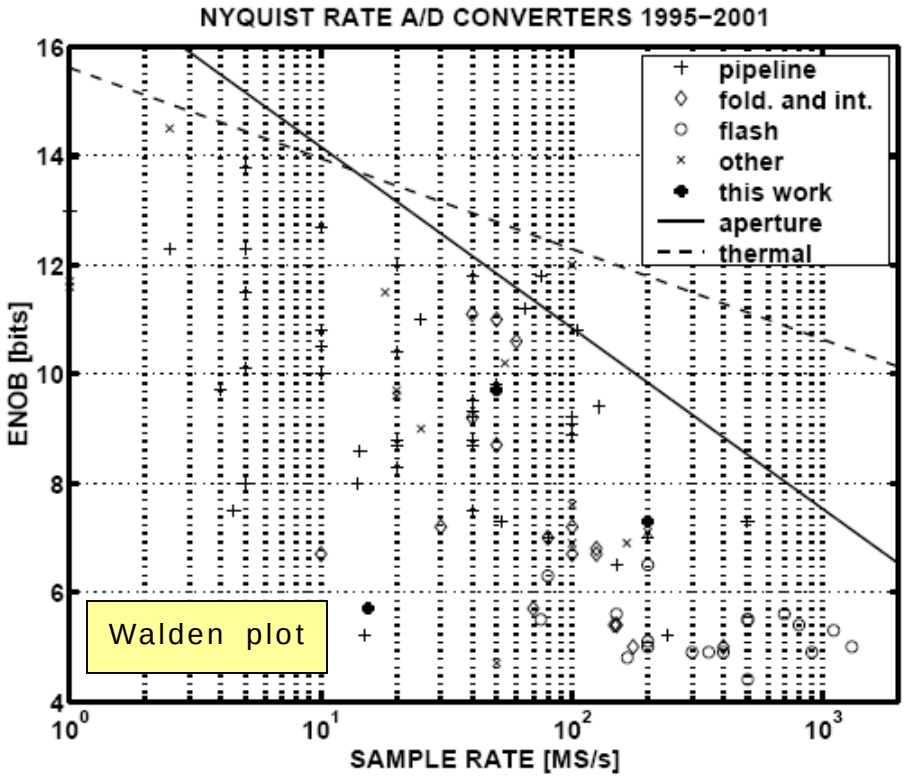
[2] Robert H. Walden. Analog-to-digital converter technology comparison. In *IEEE GaAs IC Symposium, Technical Digest*, pages 217–219, October 1994.

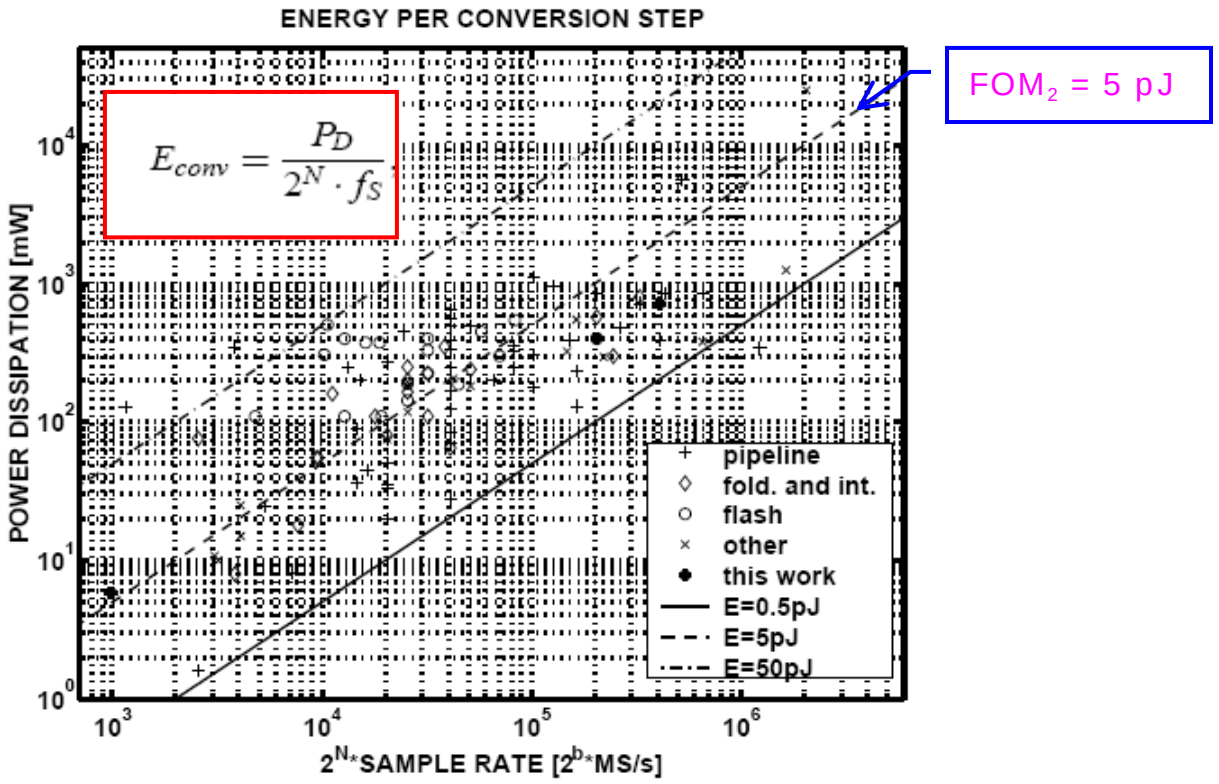
[3] Robert H. Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on Selected Areas in Communication*, 17(4):539–550, April 1999.

[4] Govert Geelen. A 6b 1.1GSample/s CMOS A/D converter. In *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pages 128–129, February 2001.

[5] Peter Scholtens and Maarten Vertregt. A 6b 1.6GSample/s flash ADC in 0.18μm CMOS using averaging termination. In *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pages 168–169, February 2002.

[6] Joshua W. Phinney. Student Evaluation for MIT Course 6.331: Advanced Circuit Techniques, May 2002. In his evaluation, Mr. Phinney wrote: "Recitation Instructor [Kent Lundberg] is hopelessly pedantic." This comment was taken as a compliment.

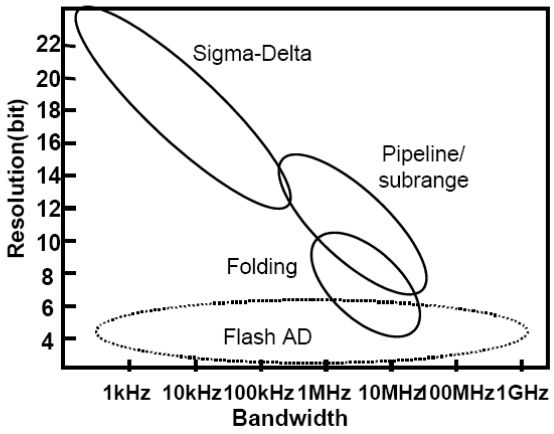

NYQUIST RATE A/D CONVERTERS 1995−2001
ENOB [bits]
SAMPLE RATE [MS/s]
pipeline
fold. and int.
flash
other
this work
aperture
thermal
Walden plot


ENERGY PER CONVERSION STEP
$E_{conv} = \frac{P_D}{2^N \cdot f_S}$
FOM$_2$ = 5 pJ
POWER DISSIPATION [mW]
2^N*SAMPLE RATE [2^b*MS/s]
pipeline
fold. and int.
flash
other
this work
E=0.5pJ
E=5pJ
E=50pJ

A. Baschirotto, et al. "A/D and D/A Converters"

A/D Converter: Speed vs. Resolution

A trade-off exists between Speed and Resolution

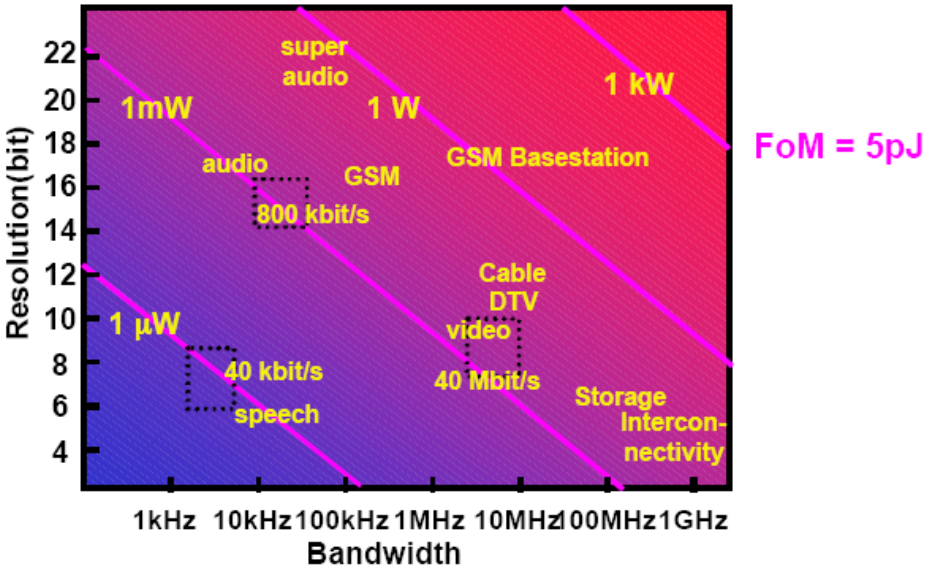


A/D Converter power

F.o.M. = energy needed per conversion [Joules]

$$F.o.M. = \frac{P}{2^n \cdot 2 \cdot BW}$$

- signal bandwidth (BW)
- effective number of bits (n)
- power dissipation (P)



FoM = 5pJ

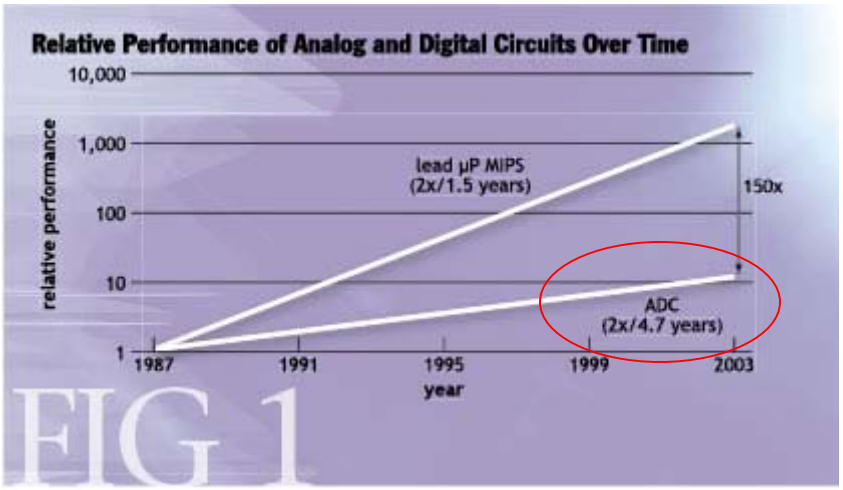
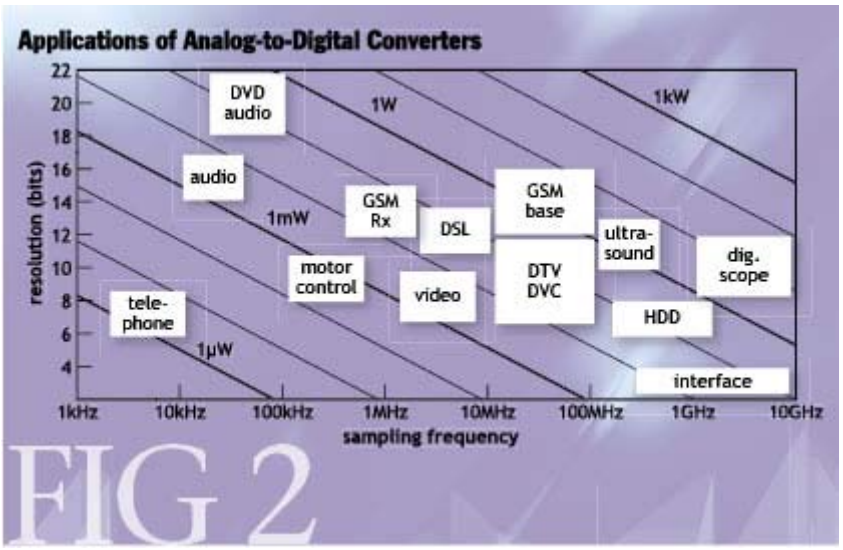
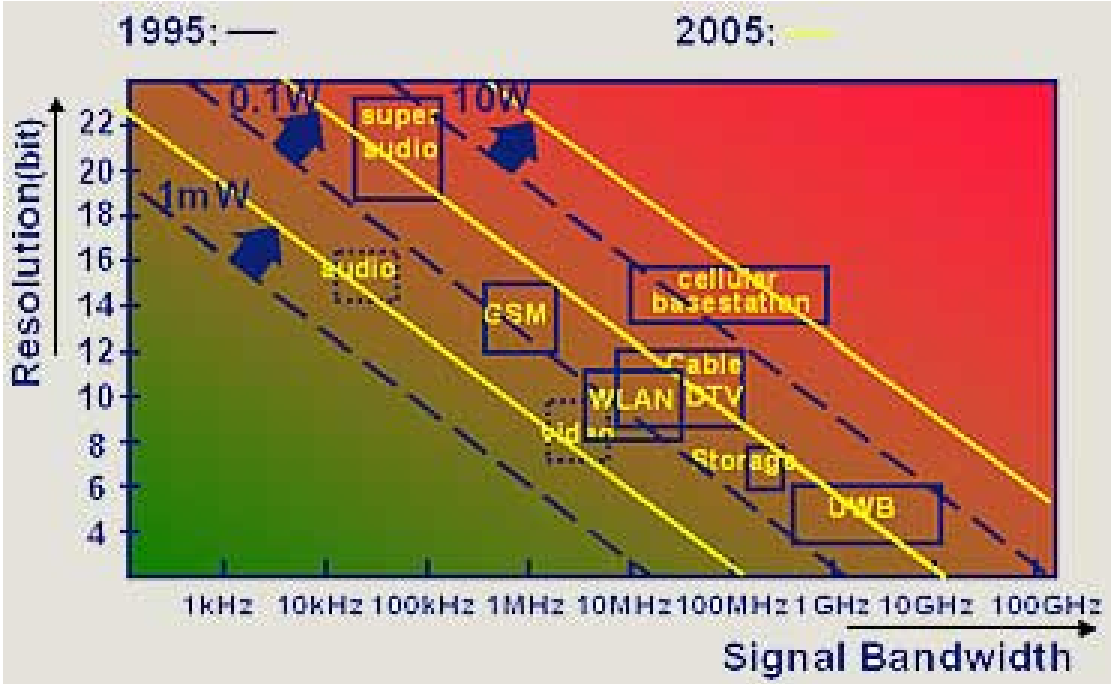


Figure 1 shows the relative performance of microprocessors and **analog-to-digital converters** over the last 15 years. While analog and digital system performance increases exponentially over time, microprocessor performance increased more than a thousandfold compared with **an increase of only 10 times for ADCs**. As the relative performance gap widens, applications such as digital audio, video, and RF (radio frequency) communication are increasingly *limited* not by the available digital processing power, but by their analog interfaces.



With the increasing trend toward battery-powered devices, **power** dissipation is an important consideration when choosing an ADC. In most portable applications the power budget for an ADC is limited to a fraction of a watt. As shown in **figure 2**, this dictates a very strict upper limit on performance that depends only weakly on technology. Power dissipation is a showstopper for an increasing number of otherwise attractive applications, such as so-called "software radios."

http://www.research.philips.com/technologies/ics/sigma-delta/T

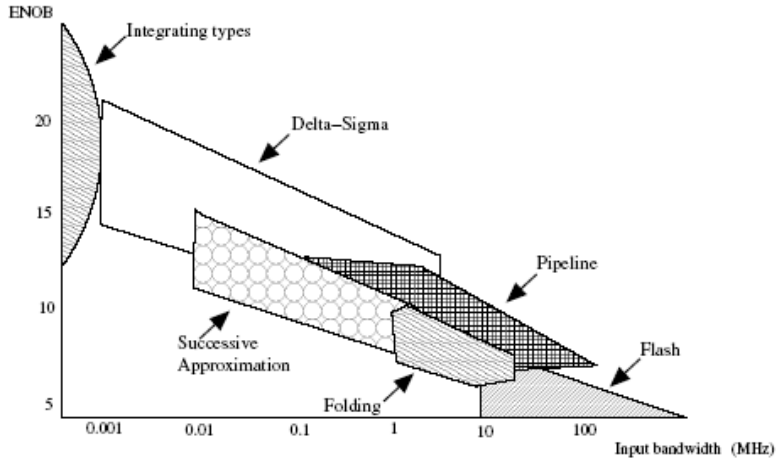


The basic principle of **sigma delta** converters involves the trade-off of amplitude resolution for sampling rate. In contrast to other converter technologies such as Nyquist and Flash converters, sigma delta converters sample signals many times *faster* that the Nyquist sampling frequency (i.e. twice the bandwidth of the input signal) but only with one bit of amplitude resolution. They offer high resolution achieved principally by their high-speed sampling combined with feedback, *noise shaping and digital filtering.*

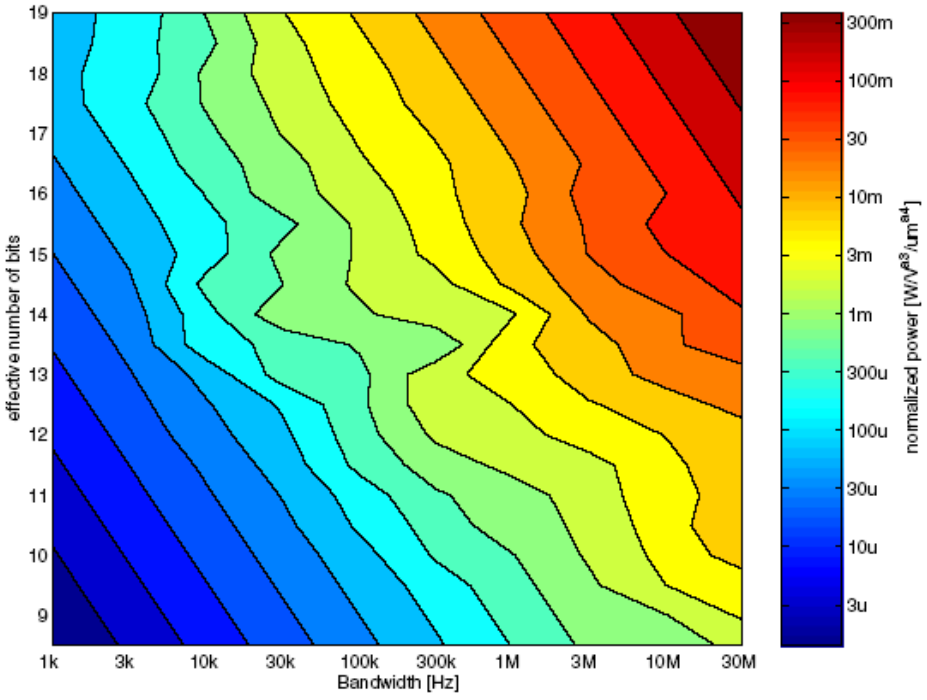
With the present state of the technology, Nyquist and Flash converters are more suitable for wideband applications than oversampled sigma delta converters. However, sigma delta converters do offer the distinct advantage of lower power consumption. This is an important criterion especially with the proliferation of **low-power** mobile communication systems in today's consumer electronics market, which means that the application areas for sigma delta converters will only grow.

Architectural Selection of A/D Converters

Martin Vogels Georges Gielen



Areas of application for different converter types.



Contour plot for the power of ΔΣ converters.

Analyzing sigma-delta ADCs in deep-submicron CMOS technologies

By Yann Le Guillou

$$FOM = \frac{Power}{2^{ENOB} \cdot 2 \cdot signalband} \qquad \text{Eq. 1}$$

where ENOB is the effective number of bits, calculated according to the peak signal-to-noise-and-distortion-ratio (SNDR):

$$ENOB = \frac{SNDR\big|_{dB} - 1{,}76}{6{,}02} \qquad \text{Eq. 2}$$

The FOM is expressed in picojoules per conversion (pJ/conv.)

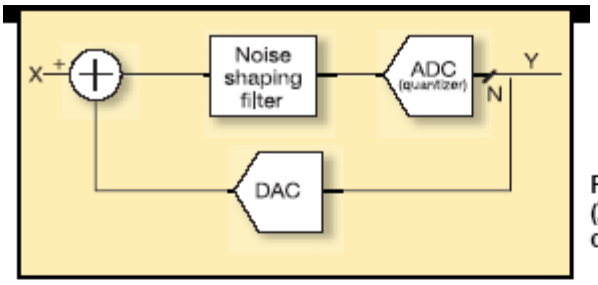


Figure 2. Sigma-delta (ΣΔ) ADC block diagram.

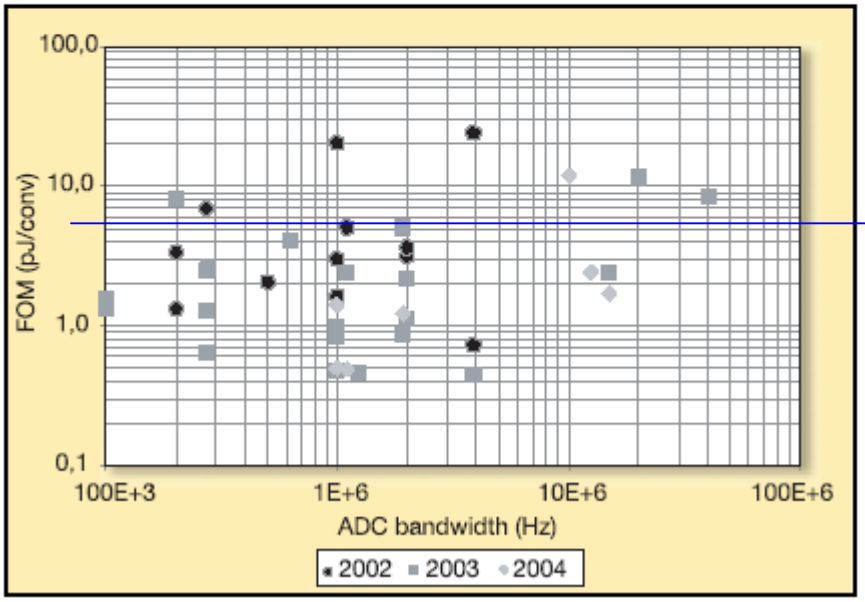


Figure 3. Surveying ΣΔ ADCs bandwidth limits.

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As a reference, Fig. 18 shows the comparison of this design (marked by a square) and the previously reported high-resolution ADCs (marked by diamonds) with a 12-b and higher resolution dated from 1988 to 2004. For SNR-limited designs, a more appropriate figure of merit (FOM) used in this comparison is defined as

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot f_s} \cdot V_{dd}. \tag{5}$$

This is in accordance with (1) that the conversion power is inversely proportional to the supply voltage, as manifested by the normalization to the supply voltage in (5). This 14-b pipeline ADC has achieved the lowest FOM in this category of Nyquist converters.

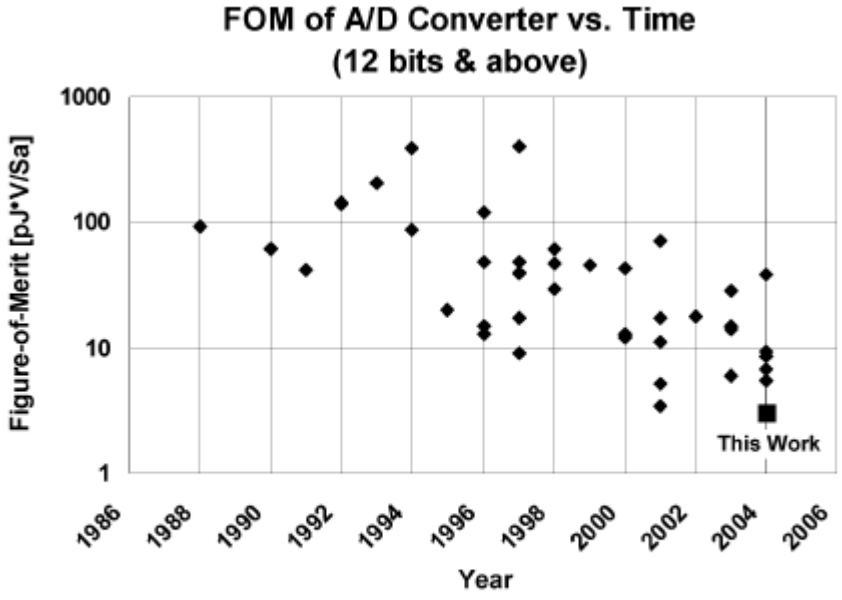

Fig. 18. Comparison of this prototype (square) and previously published ADCs (diamonds).

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IX. Resolution/Speed/Power Figure of Merit

As the previous sections clarified, for a given process technology the main tradeoff concerning this converter is resolution versus supply voltage, which in turn affects power consumption and speed. Theoretical analyses of the nonidealities in silicon technologies [19], [20], complemented by aperture jitter and thermal noise considerations in [21] finally lead to the definition of a figure of merit (FoM1) in [22] that rates the resolution via the ENOB and the effective conversion speed via the SINAD bandwidth taken at -3 dB (ERBW in the following). By definition, $f_S = 2 \cdot \mathrm{ERBW}$ sets the maximum sampling rate that prevents the ENOB degradation from exceeding 0.5 bits at Nyquist, and is normalized to the power P_{tot} dissipated by the ADC

$$\mathrm{FoM1} = \frac{P_{\mathrm{tot}}}{2^{\mathrm{ENOB}} \cdot (2\mathrm{ERBW})}. \tag{9}$$

More recently [23], normalization for the supply voltage was added to the definition found in [21] which adopts f_s instead of ERBW. Such figure (FoM2) weighs the sampling rate against supply, as is especially meaningful for CMOS cores

$$\mathrm{FoM2} = \frac{P_{\mathrm{tot}}}{2^{\mathrm{ENOB}} \cdot f_s} \cdot V_{\mathrm{DD}}. \tag{10}$$

The formulas provide unified metrics for comparison of ADCs built for different resolutions, conversion rates, and power constraints. Dimensionally, the FoMs are expressed as "energy per conversion," i.e., lower figures identify more efficient converters. Examples of FoM computation are reported in Table II for the ADCs referenced in Section I as compared to this core. Note how the ERBW of [3] has been assumed to be $f_S/2$, lacking more specific data.

Finally, Fig. 17 shows FoM1 and FoM2 as calculated on many other published and commercial Nyquist ADCs with at least 14 bits and $f_s > 20$ MS/s. When sorted against the stated resolution as done in the plot, the FoMs reveal the same trend of efficiency loss for less mature nodes already noticed in [21] (dashed lines), which the proposed converter indeed overturns. When the FoMs dependence on the ENOB is emphasized by representing ADCs with $\mathrm{ENOB} > 12.4$ with darker squares, it is apparent that the protoype 16-bit converter developed in this work ranks among the best very-high-resolution ADCs reported to date. In particular, once the FoM2 of ADCs operating at $f_s >= 65$ MS/s is considered, this core ranks best among any ADC with ENOB of 12.1 or higher.

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TABLE II
Examples of FoM Extraction and Comparison

ADC	Stated # of bits	f_s [MS/s]	ENOB @dc	ERBW [MHz]	Power [mW]	FoM1 [pJ/conv]	FoM2 [pJ·V/conv]
[2]	14	100	12.1	70	1250	2.0	14.2
[3]	16	20	12.6	10	750	6.0	30.2
This work (ext VREF)	**16**	**65**	**12.7**	**40**	**970**	**1.8**	**7.4**
This work (int VREF)	**16**	**65**	**12.6**	**50**	**1150**	**1.9**	**9.4**

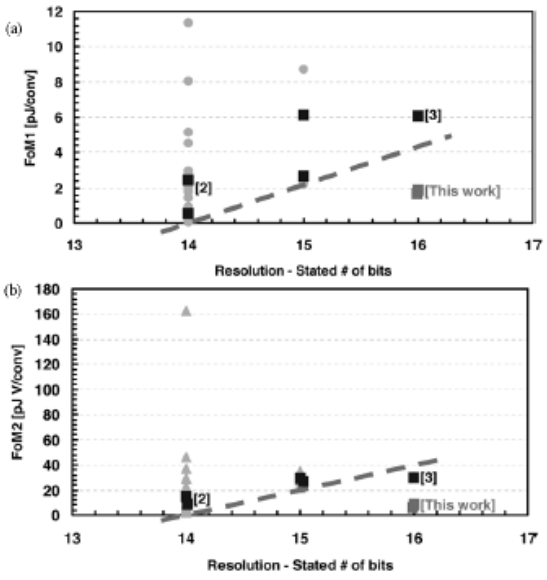


Fig. 17. (a) FoM1 and (b) FoM2 categorized versus the stated resolution. The dashed lines extrapolate the best-in-class FoM trend; the darker squares mark ADCs with $\mathrm{ENOB} > 12.4$. The 14-bit converter with $\mathrm{ENOB} = 12.6$ and FoM1 of 0.6 pJ/conv is a 25 MS/s part.

[2] C. Moreland, F. Murden, M. Elliott, J. Young, M. Hensley, and R. Stop, "A 14b 100 Msample/s subranging ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1791–1798, Dec. 2001.

[3] S. Hisano and S. E. Sapp, "A 16-bit, 20 MSPS CMOS pipeline ADC with direct INL detection algorithm," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2003, pp. 417–420.

[19] P. Kinget and M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1996, pp. 333–336.

[20] K. Uyttenhove and M. Steyaert, "Speed-power-accuracy trade-off in high-speed ADC's: What about nano-electronics?," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2001, pp. 341–344.

[21] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[22] G. J. G. M. Geelen, "A 6b 1.1 Gsample/s CMOS A/D converter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2001, pp. 128–129.

[23] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14b 12 MSps CMOS pipeline ADC with over 100 dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, Dec. 2004.

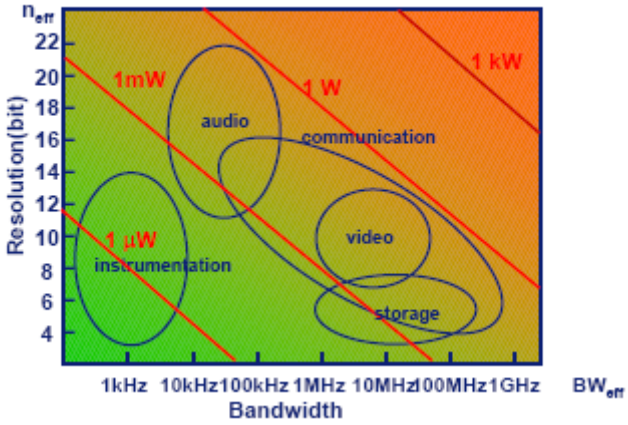
Figure of Merit (FoM) for AD

$$FoM = Power / (2^{n_{eff}} * 2\,BW_{eff})$$

energy/conversionstep [pJ]

- Combines effective performance and power
  - BW_{eff} & resolution: span several orders of magnitude
  - FoM spans 1 order of magnitude
  - State of the art is 0.5 to 5pJ
- Useful as benchmark & to estimate power in system design

Equal power lines for FoM = 1pJ



Example calculation of FoM

ANALOG DEVICES

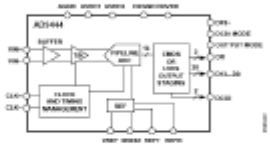
14-Bit 80 MSPS A/D Converter

AD9444

FEATURES

- 80 MSPS guaranteed sampling rate
- 100 dB two-tone SFDR with 69.3 MHz and 70.3 MHz
- 73.1 dB SNR with 70 MHz input
- 97 dBc SFDR with 70 MHz input
- Excellent linearity
  - DNL = ±0.4 LSB typical
  - INL = ±0.6 LSB typical
- 1.2 W power dissipation
- 3.3 V and 5 V supply operation
- 2.0 V p-p differential full-scale input

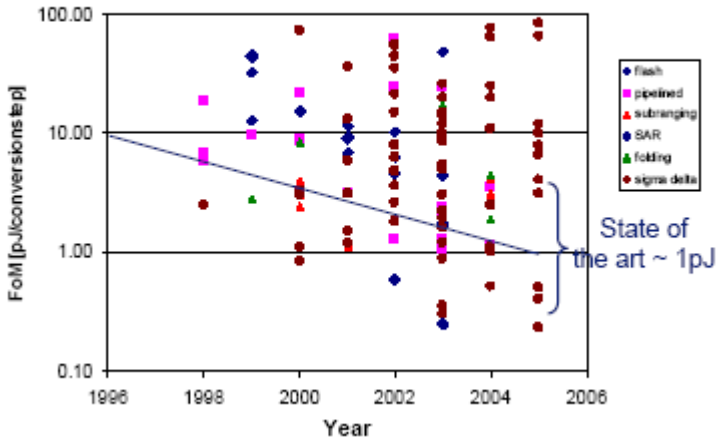
FUNCTIONAL BLOCK DIAGRAM



SIGNAL-TO-NOISE-AND DISTORTION (SINAD)					
f_{IN} = 10 MHz	25°C	IV	71.0	74.0	dB
	Full	IV	72.7		dB
f_{IN} = 35 MHz	25°C	I	72.4	73.7	dB
	Full	IV	72.1		dB
f_{IN} = 70 MHz	25°C	IV	72.1		dB
	Full	IV	72.0		dB
f_{IN} = 180 MHz	25°C	V		72.3	dB
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C	V		12.1	Bits
f_{IN} = 35 MHz	25°C	V		12.0	Bits
f_{IN} = 70 MHz	25°C	V		11.9	Bits
f_{IN} = 180 MHz	25°C	V		11.8	Bits

$$FoM = 1.2 / (2^{12.1} * 2\,40M) = 3.4pJ$$

FoM as function of time



http://public.itrs.net/Files/2001ITRS/SysDrivers.pdf

ANALOG-TO-DIGITAL CONVERTER (ADC)

Digital processing systems have interfaces to the analog world: audio and video interfaces, interfaces to magnetic and optical storage media, and interfaces to wired or wireless transmission media. The analog world meets digital processing at the analog-to-digital converter (ADC), where continuous-time and continuous-amplitude analog signals are converted to discrete-time (sampled) and discrete-amplitude (quantized). The ADC is therefore a useful vehicle for identifying advantages and limitations of future technologies with respect to system integration. It is also the most prominent and widely used mixed-signal circuit in today's integrated mixed-signal circuit design.

To yield insight into the potential of future technology nodes, the ADC FoM should combine dynamic range, sample rate f_{sample} and power consumption P. However, these nominal parameters do not give accurate insight into the effective performance of the converter; a better basis is the effective performance extracted from measured data. Dynamic range is extracted from low frequency signal-to-noise-and-distortion ($SINAD_0$) measurement minus quantization error (both values in dB). From $SINAD_0$ an "effective number of bits" can be derived as $ENOB_0 = (SINAD_0 - 1.76)/6.02$. Then, the sample rate may be replaced by twice the effective resolution bandwidth (2x$ERBW$) if it has a lower value, to establish a link with the Nyquist criterion:

$$FoM_{ADC} = \frac{\left(2^{ENOB_0}\right) \times \min(\{f_{sample}\}, \{2 \times ERBW\})}{P}$$

For ADCs, the relationship between FoM and technology parameters is strongly dependent on the particular converter architecture and circuits used.

The trend in recent years shows that the ADC FoM improves by approximately a factor of 2 every three years. Taking increasing design intelligence into account, these past improvements are in good agreement with improvements in analog device parameters. Current best-in-class is approximately 800G [conversion-step/Joule] for stand-alone CMOS/BiCMOS, and approximately 400G [conversion-step/Joule] for embedded CMOS. Expected future values for the ADC FoM are shown in Table 9. Major advances in design are needed to maintain performance increases for ADCs in the face of decreased voltage signal swings and supplies. In the long run, fundamental physical limitations (thermal noise) may block further improvement of the ADC FoM.

Table 9 Projected Mixed-signal Figures of Merit for Four Circuit Types

YEAR OF PRODUCTION	2001	2004	2007	2010	2013	2016
MPU ½ PITCH	130	90	65	65	45	22
F_oM_{LNA} [GHz]	10	15	25	30–40	40–50	50–70
F_oM_{VCO} [1/J] 10^{22}	5	6	7	8–9	10–11	12–14
F_oM_{PA} [W•GHz^2] 10^4	6	12	24	40–50	80–90	100–130
F_oM_{ADC} [1/J] 10^{12}	0.4	0.8	1-1.2	1.6–2.5	2.5–5	4–10

Estimation of technology sufficiency—Figure 9 shows ADC requirements for recent applications in terms of a power/performance relationship. Under conditions of constant performance (resolution × bandwidth), a constant power consumption is represented by a straight line with slope −1. Increasing performance, achievable with better technology or circuit design, is equivalent to a shift of the power consumption lines toward the upper right. The data show a very slowly moving technological "barrier-line" for ADCs for a given ADC sampling rate and power consumption of 1W (Figure 9). Most of today's ADC technologies (silicon, SiGe, and III-V compound semiconductor technologies and their hybrids) lie below the 1W barrier-line, and near-term solutions for moving the barrier-line more rapidly are unknown.

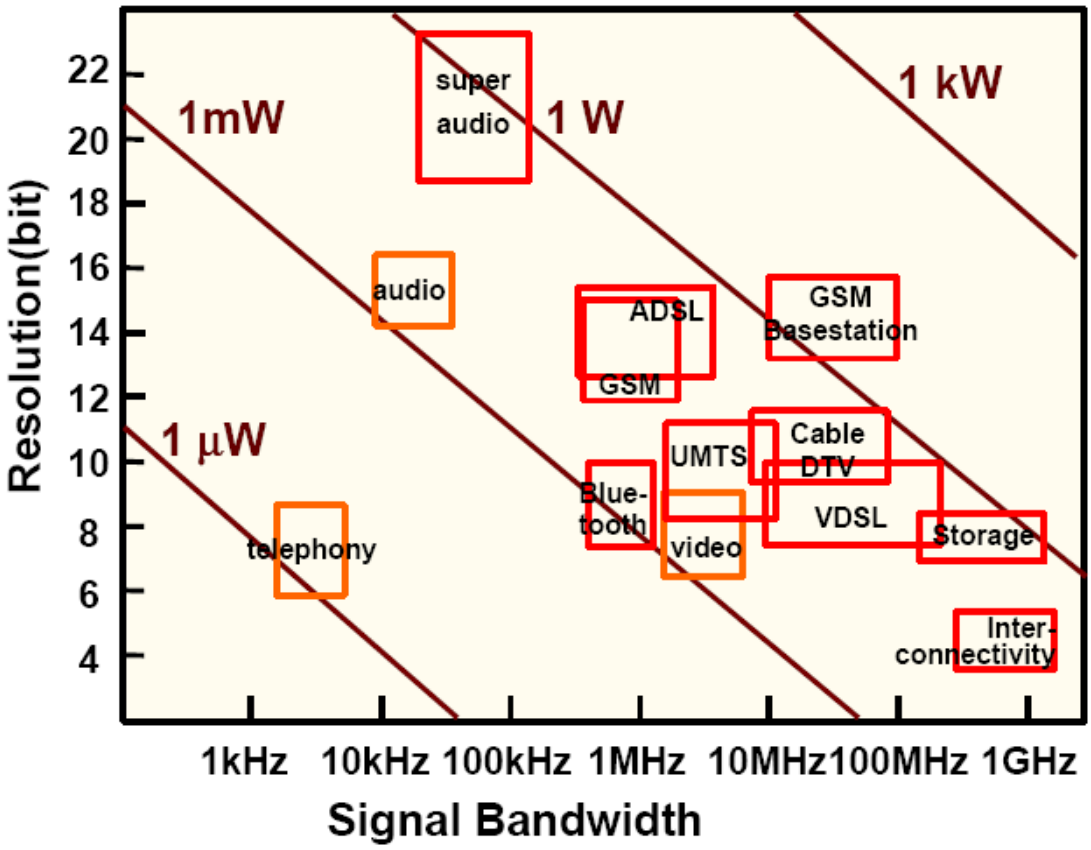
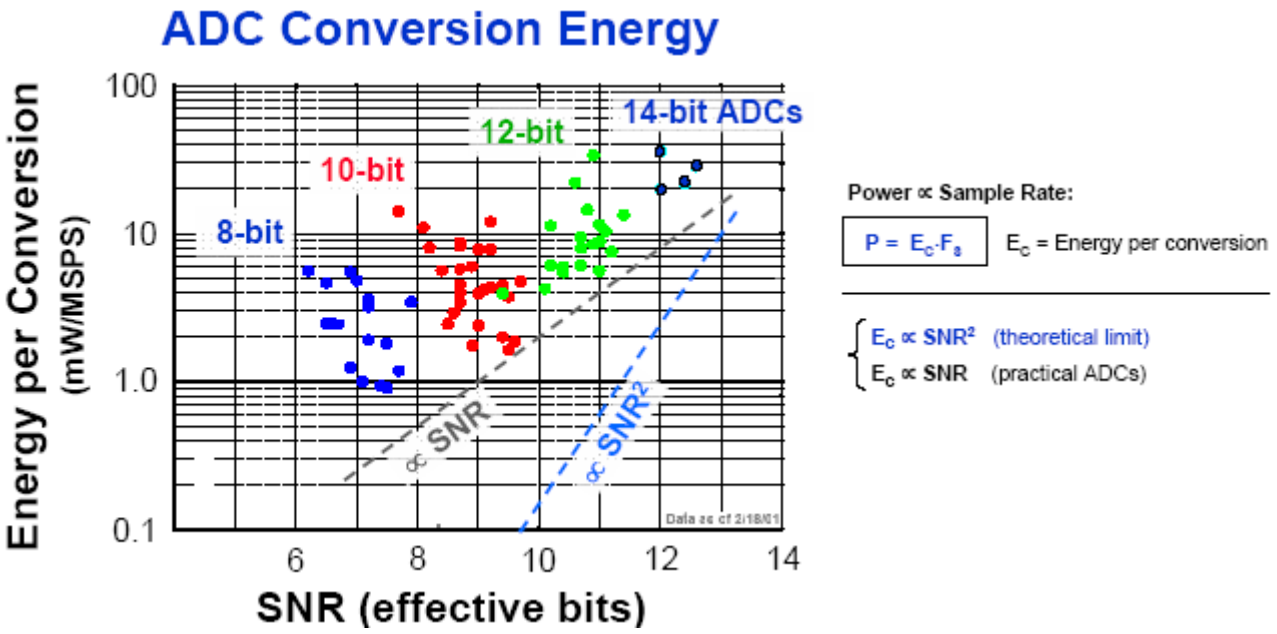
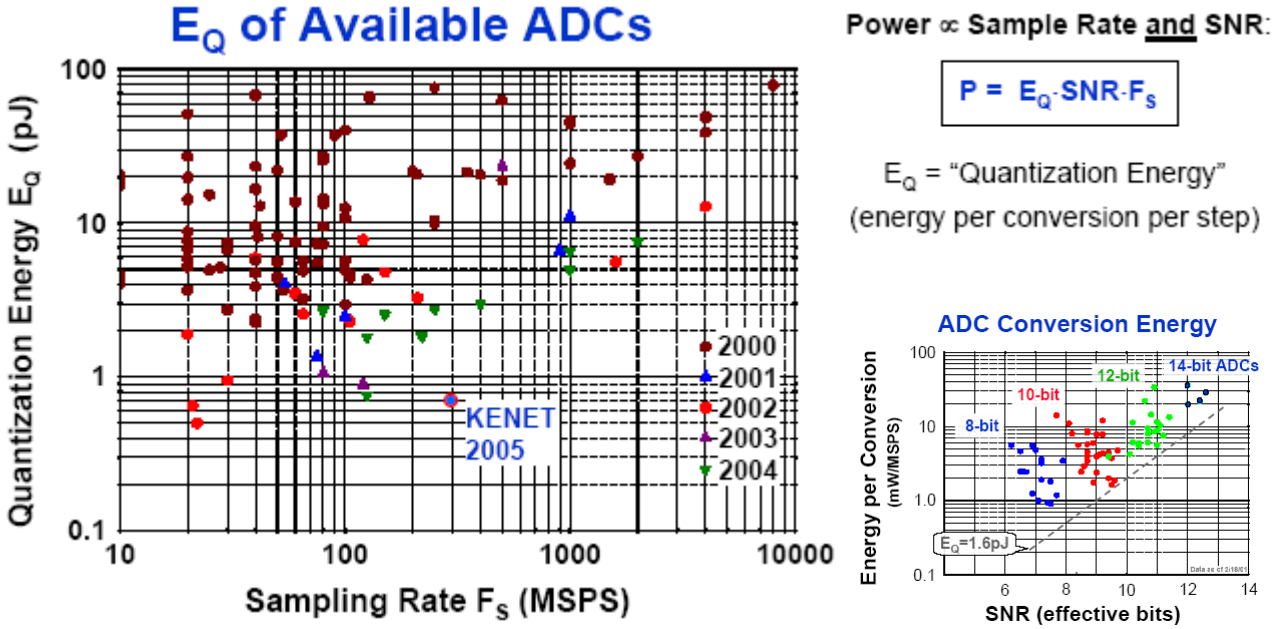


Figure 9 Recent ADC Performance Needs for Important Product Classes

While the rate of improvement in ADC performance has been adequate for handset applications, this is clearly not the case for applications such as digital linearization of GSM base-stations, and handheld/mobile high-data rate digital video applications. For example, a multi-carrier GSM base-station with a typical setup of 32 carriers requires over 80dB of dynamic range. Implementing digital linearization in such a base-station with a 25 MHz transmitter band requires ADCs that have sampling rates of 300 MHz and 14 bits of resolution. According to Table 9 and assuming progress at recent rates, it will be perhaps until after 2010 before ADCs with such performance are manufactured in volume. While system designers would like to have such ADCs now, silicon and SiGe technologies have the necessary bit resolution (large numbers of devices per unit area) but not the speed; on the other hand, III-V compound semiconductor technologies have the speed but not the bit resolution. This motivates consideration of solutions that potentially increase the rate of ADC improvement at reasonable costs – e.g., use of compound semiconductors for their speed (perhaps combinations of HBTs, HEMTs, and resonant tunneling diodes), and hybrids of both CMOS and compound semiconductor technologies. The challenge for compound semiconductors is to increase the number of devices per unit area and to be co-integrated with CMOS processing.

Attacking the Analog Scaling Problem with Novel Silicon Device Technology
(**Charge-Domain ADC,** FemtoCharge® CMOS technology)
Michael P. Anthony, **Kenet, Inc.**

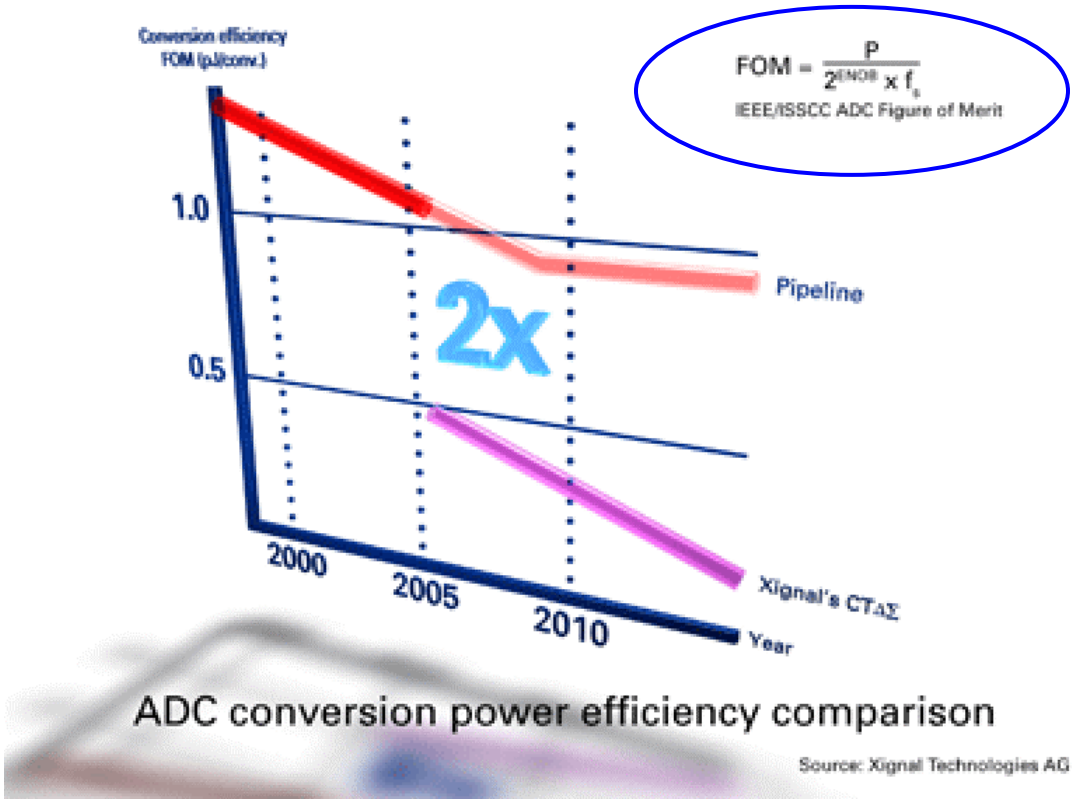




10bit @ 275Msps - performance equal to "the best traditional designs", but with *one-third* of the **core(!)** power and *one-half* of the **total(!!)** power

A/D converters break power barrier

By Bettyann Liotta, eeProductCenter
Nov 9 2005



The XT11 A/D converter family utilizes a fast, third-order continuous time delta-sigma modulator (CTDS), combined with an on-chip digital filter and tuneable loop filter.

Despite offering a **power figure of merit (FOM)** that is half that of current pipeline A/D converters, there is no trade-off in linearity or electrical performance. The XT11400 has a SNR of 76 dB and total harmonic distortion (THD) of -82 dB. The XT11200 turns in an SNR of 71 dB and THD of -78 dB.

The 12-bit (XT11200) and 14-bit (XT11400) devices consume only 70 mW — while operating at 20 to 40 Msamples/second.

Converter Topology	Resolution	Sample rate	Typical FOM
1. Flash	Typically up to 8-bits	Multi-GHz	VP1058 – Zarlink, 8b, 25 MSPS ADC Status: Obsolete (included for comparison only) FOM = 259 pJ/conv
2. Folding/Interpolating	6 to 10-bits	Up to 1 GHz	ADC081000 – National Semiconductor, 8b, 1000 MSPS Status: Production, FOM = 13.1 pJ/conv
3. Pipeline	10 to 16-bits	5 to 150 MHz	ADS5421 – TI, 14b, 40 MSPS Status: Production, FOM = 5.5 pJ/conv AD9244-40 – Analog Devices, 14b, 40 MSPS Status: Production, FOM = 2.78 pJ/conv MAX1260 – Maxim, 12b, 40 MSPS Status: Production, FOM = 2.54 pJ/conv LT2247 – LTC, 14b, 40 MSPS Status: Production, FOM = 1.05 pJ/conv
4. Conventional $\Delta\sum$ (discrete time)	>16-bits	200kHz to 1MHz	ADS1605 – Texas Instruments, 16b, 5 MSPS ADC Status: Production, FOM = 10.7 pJ/conv
5. Advanced CT $\Delta\sum$	10 to 16-bits	1 to 100 MHz	XT11 development – Xignal Technologies, 14b, 40 MSPS Status: In development, FOM = 0.4 pJ/conv with PLL & CLK,

An ADC Figure of Merit (FOM)

The analog program committee of the IEEE International Solid-State Circuits Conference suggested an objective figure of merit (FOM) for ADC comparisons that takes into account power consumption, effective resolution and sampling rate. With units of energy it represents the energy used per conversion, and is calculated as follows:

$$FOM = \frac{P}{(2^{ENOB} \times f_s)}$$

P is the power dissipation in Watts, ENOB is the effective number of bits at a sample rate f_s in Hertz. FOM yields a result in Joules/conversion.

Rarely found in manufacturer's data, the FOM has merit in comparing the performance of a particular ADC product or specific architecture. Its value lies in identifying best energy efficiency compared to raw dynamic performance of the converter. In using the ENOB specification it quantifies all noise and distortion sources introduced by the converter.

Design Considerations for Continuous-Time Bandpass ADCs

Richard Schreier
Oct 24 2005

ANALOG DEVICES

Outline

1 An ADC Figure-of-Merit

~~2 Overview of Bandpass ADCs~~

~~3 A High-Q Active-RC Resonator~~

~~4 IDAC Design Considerations~~

Thermal noise
Switching dynamics

An ADC Figure-of-Merit?

- Is an ADC which has SNR = 100 dB over BW = 1 MHz fundamentally better or worse than an ADC which has SNR = 90 dB over the same bandwidth, if ADC1 consumes 1 W while ADC2 consumes 100 mW?

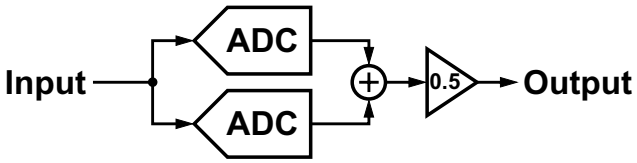
An ADC Figure-of-Merit?

- More generlally, what is the fundamental trade-off between

Bandwidth (BW),
Dynamic Range (DR)
and
Power consumption (P)
?

DR-P Trade-Off: Part 1

- To increase DR at the expense of P, parallel two ADCs and average:



- Averaging reduces noise by a factor of $\sqrt{2}$: DR += 3 dB
  Assuming the ADCs' noises are uncorrelated
- But uses twice the power: P += 3 dB

DR-P Trade-Off: Part 2

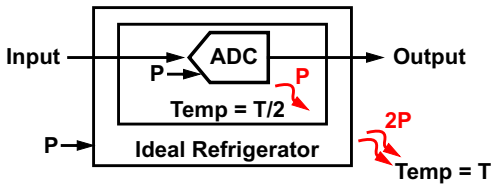
- To reduce P at the expense of DR, "cut the ADC in half"
  May not be practical if the ADC is already small, but if it can be done,
  P –= 3 dB & DR –= 3 dB
- ∴ For an ADC of some BW,
  x dB in DR costs *x* dB in P,
  or
  DR (in dB) – $10\log_{10}(P)$ = const

Q: Is This Trade-Off Optimal?

- **A: Yes, because it is bi-directional**
  The fact that you can (in principle) go both ways for any ADC means that no other trade-off can exist for ADCs that are optimal.
- **Consider a (supposedly) optimal ADC that can get more than 3 dB increase in DR for a doubling of P**
  Double P, then cut that ADC in half.
  The resulting ADC has the same P as the original, but more DR.

DR-P Trade-Off: Part 1b

- **Can increase DR by 3 dB by reducing T by a factor of 2:**



- **But this also costs twice the power**

What About BW?

- **Reducing BW by a factor of 2 increases DR by 3 dB but leaves P alone**
  Assuming the noise is white (distortion is not dominant) and that digital filtering takes no power.
- **Time-interleaving two ADCs doubles BW and doubles P, but leaves DR unchanged**
  I/Q processing does the same.
  Assumes that interleaving is perfect (can be calibrated).

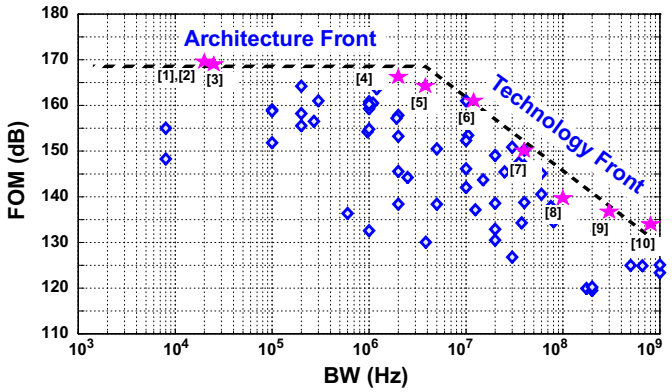
Resulting FOM

- **Use a dB scale:**

$$FOM = (DR)_{dB} + 10\log\frac{(BW)}{P}$$

- **For a given FOM, factors of 2 in BW or P are equivalent to a 3-dB change in DR**
- **Should really include T, but since T is usually 300K, omit it**
  Steyaert et al. like $FOM = \frac{4kT \times DR \times 2BW}{P}$

State-of-the-Art FOM



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