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ADC Standard Harmonization: Comparison of Test Methods

E. Balestrieri, P.Daponte, IEEE SENIOR MEMBER, S. Rapuano, IEEE MEMBER

Dept. of Engineering, University of Sannio, Corso Garibaldi 107, 82100, Benevento, Italy
Ph.: +39 0824305817; Fax: +39 0824305840
E-mail: {balestrieri, daponte, rapuano}@unisannio.it
http://lesim1.ing.unisannio.it

Abstract *– The paper describes an experimental investigation for the harmonization of the measures of the ADC dynamic performance in the frequency domain, according to the Standards in the field. The comparison results, involving Spurious Free Dynamic Range (SFDR), Total Harmonic Distortion (THD), SIgnal to Noise And Distortion ratio (SINAD), Signal to Noise Ratio (SNR) and Effective Number Of Bits (ENOB), show a good degree of similitude among the results provided using procedures and formulas from different standards of IEEE and IEC.*

Keywords *– ADC, Harmonization, DYNAD, IEEE, IEC, SFDR, THD, ENOB, SINAD, SNR.*

I. INTRODUCTION

Analog to Digital Converters (ADCs) translate analog quantities, which are characteristic of most phenomena in the "real world", to digital quantities, used in information processing, computing, data transmission and control systems [1]. In the years the considerable increase in the number and variety of ADCs produced and sold all over the world, has led to the need for common terms, definitions, and test methods internationally accepted. Although some ADC standards have been released, a unified approach is still missing because of the different adopted terms, acronyms, definitions and test methods. Standard harmonization is essential to provide manufacturing economies and to eliminate duplication of conformity assessment testing.

Aware of this, IEEE Technical Committees are currently working to harmonize IEEE Standards with those of IEC [2]. The intent is to write new IEEE Standards as truly international standards which could be accepted with little or no change by IEC [2]. Harmonizing existing standards requires: (i) comparing scopes, terminology, test procedures, requirements, measurement units, (ii) identifying differences, (iii) harmonizing wherever agreement can be reached, and (iv) clearly identifying the remaining areas of disagreement that need to be resolved [2].

In the last years the authors have been carried out a research work devoted to propose the harmonization of IEEE Standards in the ADC and Digital to Analog Converter (DAC) field with other international standards. An analytical comparison of ADC dynamic parameters reported in the most diffused standards that can be used internationally to put in evidence similarities and ambiguities in definitions and descriptions has already been described in [3]. This paper reports the results of a new phase of research. The test results obtained according to different standards on ADCs have been compared. In particular, a quantitative analysis of the ADC parameters in the frequency domain measured through the methods reported in IEC Std. 60748-4-3 [4], IEEE Std. 1241 [5], IEEE Std. Draft 1057 [6] and DYNAD [7] has been carried out. In this way, it is possible to deal with the above suggested steps by (i) comparing the test procedure, (ii) identifying differences among the test procedures and among the obtained results, (iii) understanding where an agreement can be reached, and (iv) identifying the disagreements to overcome.

A comprehensive analysis and comparison of the results obtained on different real ADCs by the implementation of the considered standard test methods on the same test bench has been carried out. In particular, the paper presents the first results of an experimental comparison involving the most widely used ADC dynamic parameters, the frequency domain ones: Spurious Free Dynamic Range (SFDR), Total Harmonic Distortion (THD), SIgnal to Noise And Distortion ratio (SINAD), Signal to Noise Ratio (SNR) and Effective Number Of Bits (ENOB).

II. ADC STANDARDS

The released standards on ADCs internationally available are: (i) IEEE Std.1241 [5], including terminology and test methods for static and dynamic performance assessment, (ii) IEEE Std.1057 [8], including the same issues focused on digitizing waveform recorders, (iii) IEC Std. 60748-4 [9] including only terminology and static test methods, (iv) IEC Std. 60748-4-3 [4], concerning dynamic performances, and (v) IEC Std. 62008 [10] dealing with performance characteristics and calibration methods for data acquisition systems.

In particular, the IEC international standard [4] introduces a set of dynamic methods, which are now coming into use in industry and which rely mostly on measurements made in the frequency domain using sinusoidal input signals. It also includes a further dynamic method that uses a wide-band input signal.

The IEEE Std.1241 identifies ADC error sources and provides test methods to perform the required error measurements. The information in the standard is useful both to manufacturers and to users of ADCs providing a basis for evaluating and comparing existing devices, as well as a template for writing specifications for ordering new ones [5].

The IEC Std. 62008 covers: (i) the minimum specifications that the DAQ device manufacturer must provide to describe

the performance of the Analogue-to-Digital Module (ADM) of the DAQ device; (ii) standard test strategies to verify the minimum set of specifications; (iii) the minimum calibration information required by the ADM that is stored on the DAQ device; and (iv) the minimum calibration software requirements for external and self-calibration of the ADM of the DAQ device.

The IEEE Std.1057 deals with waveform recorders (and digital oscilloscopes) which have digital outputs. Therefore, much of Std.1057 is appropriate for specifying and testing an ADC, too. The IEEE TC-10 has recently completed the revision of this standard [6], that is currently in the balloting stage. Some parameters missing in the previous versions of the standard, have been added and more detailed test procedures have been included both in the case of coherent and non-coherent sampling.

An important effort to contribute to the improvement of the European standards concerning dynamic ADC testing has been done by the research project 'Methods and draft standards for the DYNamic characterization and testing of Analog to Digital converters', (DYNAD) [7] supported by the European Commission programme on "Standards, Measurements and Testing". Purpose of the DYNAD project has been not only the evaluation and redefinition of some classical ADC test methods, but also the development of new ones. In particular, the final document addresses a number of open questions concerning the implementation of the "classical" dynamic test methods based on the application of a sinusoidal stimulus to the ADC under test, and provides a draft standard of test methods for the ADC dynamic characterisation using sinusoidal stimuli [7].

Both the IEEE Std.1241 and DYNAD have been proposed to support, to integrate and to complement the IEC Std. 60748-4 for the part concerning ADC dynamic testing before the new IEC Std. 60748-4-3 was published.

In this paper the methods provided to measure ADC frequency domain parameters reported in IEC Std. 60748-4-3, IEEE Std. 1241, IEEE Std. Draft 1057 and DYNAD have been compared, with the aim of determining their degree of harmonization from the application point of view. IEC Std. 62008 has not been considered since it addresses the IEC Std. 60748-4-3 for the ADC dynamic parameters measurement.

The obtained results can be also useful to give contributes and discussion topics during the revision of the IEEE Std. 1241 and its harmonization with the IEC standard.

III. COMPARISON OF STANDARD TEST PROCEDURES

The tests included in IEEE Std.1241, IEEE Std. Draft 1057, DYNAD and IEC Std.60748-4-3 for measuring SFDR, THD, SINAD, SNR and ENOB have been compared in terms of completeness and effectiveness through a comprehensive analysis of the differences in the obtained test results. In order to achieve such result the test setups and procedures have been compared first. Then, the procedures have been applied to a set of actual ADCs.

A. Comparison of test setups

All the considered standards to measure the quoted above ADC dynamic parameters use sinewaves as input signals. The advantage of sinewave as stimulus signal is that it is relatively easy to evaluate its spectral purity, for instance using a spectrum analyzer. It is also easy to improve its purity by suitable filtering [6].

IEEE Std. Draft 1057 does not report a scheme describing the sinewave test setup.

In the IEEE Std.1241 test setup (Fig.1) a sine wave generator provides the test signal while a clock generator provides the clock (or conversion) signal. If frequency synthesizers are used to generate the test and clock signals, the synthesizers can often be phase-locked to maintain precise phase relationships between the signal and the sampling clock. Both the clock and the test signals must be suitable for the test being performed. Filters may be required in either the clock or signal paths to reduce noise or harmonic distortion. Also, low-pass or band-pass filters may be required in the signal path to reduce noise or eliminate other undesirable signals. The type of circuitry used to capture the digital data samples produced by the ADC is mainly determined by the data rate. Therefore, the sinewave test setup reported in the IEEE standard includes as optional a buffer memory, latches and demultiplexers. In fact, while slower ADCs may be interfaced directly to the computer faster ADCs often require a buffer memory to acquire data at the ADC sample rate and then download stored samples to the computer at a slower rate.

While in the IEEE Standard filters between the source and the ADC are considered optional, DYNAD setup (Fig.2) in any case requires the bandpass filters, as the spectral purity of the generator alone can be frequently not adequate to the purpose of testing. Moreover, DYNAD suggests that could be necessary to use level adapters, unbalanced to balanced converters, or some other signal-conditioning device. When they are used, it is preferable to place any signal conditioning device before the filters so that any added distortion and noise can be minimized. Another difference can be found in the

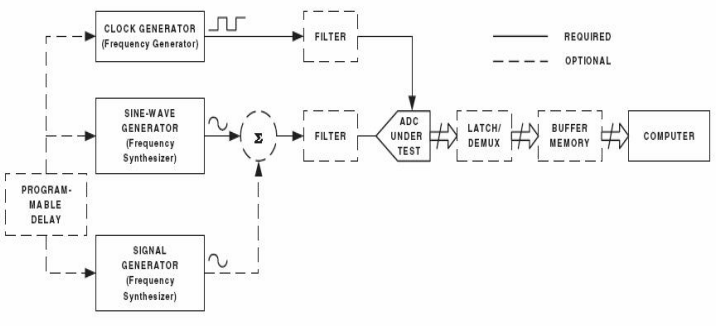

Fig.1. IEEE Std. 1241 sinewave test setup.

logic analyzer required to capture data produced by the ADC considered in the DYNAD setup.

In order to obtain a better electromagnetic environment, DYNAD suggests to use a sinewave generator to deliver the sampling clock signal. Sharp edges, in fact, can become a problem at high frequencies because of impedance mismatch, propagation delay and Voltage Standing Wave Ratio (VSWR) at higher harmonics. If a sinusoidal signal is used for clocking, the high frequency harmonic contents related to the presence of a digital clock signal are confined to a small portion of the test board, between the comparator/clock driver and the ADC under test. An external frequency divider may be inserted in the clock chain, with the aim of achieving more closely the desired frequency ratio and/or reducing the phase noise of the sampling signal. However, any additional integrated circuit provides additional jitter, so that the phase noise may even be worst with the divider than without, especially if it is not followed by a filter.

In order to specify the general requirements for measuring the characteristics of an ADC under dynamic conditions IEC Std. 60748-4-3 presents the test setup shown in Fig.3, that considers the cases of sinewave, step and linear ramp as input. This scheme is quite similar to that proposed by IEEE Std. 1241. As for the previous test setups in case of sinewave input the input voltage generator shall provide an accurate sinusoidal waveform with adjustable and stable amplitude and frequency [4]. Any impurity in the signal waveform and instability in its frequency should be low enough not to affect the measurement accuracy. Similarly, any instability in the frequency (jitter) of the clock signal should be equally low. Ideally, the input signal and the clock signal should be synchronized from a common source [4]. The IEC standard gives also recommendations about the adjustment range of the input voltage that should be such that, at its maximum excursion, the most positive and most negative peaks exceed the working range of the ADC, but do not exceed its limiting input voltages. When testing adjustable converters it is recommended to include equipment for the adjustment of offset and gain points, too [4].

B. Standard test methods

An experimental analysis about the choice of the test signal, the clock frequencies and the record size, on the accuracy of the input frequency, as well as the number of sample records used to calculate the average spectrum have been first carried out. After that SFDR, THD, SINAD, SNR and ENOB have been measured according to test methods reported in IEEE Std. 1241, IEEE Std. Draft 1057, DYNAD and IEC Std. 60748-4-3 and summarized in Tab.1.

Tab.1. IEEE Std. 1241, draft Std. 1057, DYNAD and IEC Std. 60748-4-3 test methods.

PARAM.	IEEE Std. 1241	IEEE Std. Draft 1057	DYNAD	IEC Std. 60748-4-3
SFDR	Section 4.4.5	Section 8.7	Section 6.7	Section 5.1.4
THD	Section 4.4.5	Section 7.7	Section 6.6	Section 5.1.4
SNR	Section 4.5.1	Section 8.2	Section 6.5	Section 5.1.3
SINAD	Section 4.5.1	Section 8.1	Section 6.3	Section 5.1.3
ENOB	Section 4.5.2	Section 8.4	Section 6.4	Section 5.1.3

IV. TEST SETUP AND TEST STRATEGY

Comparing the experimental results obtained by using IEEE Std. 1241, IEEE Std. Draft 1057, DYNAD and IEC Std. 60748-4-3 test methods to calculate the ADC parameters in the frequency domain, requires their implementation on the same test setup and the same Device Under Test (DUT).

Initially, some actual ADCs have been chosen including single devices to be connected to the control PC by means of a logic state analyzer and devices mounted on evaluation boards with on-board interfaces to PC. ADCs with different architecture and sampling frequency currently available in the market have been selected. The selection criteria are the following:

1) The DUT variety is more important than their number, therefore, at least one ADC should be chosen from each of the three most known manufacturers.
2) The DUT resolution should be low or middle, removing the problems due to the high spectral purity required to the signal generators at resolutions higher than 10-12 bits. The test bench and the specific set-up operations should be as similar as possible. Otherwise, no general observation can be done about the figures of merit.
3) The maximum sampling frequencies should be chosen as much different as possible including ADCs with low and high sampling frequencies.

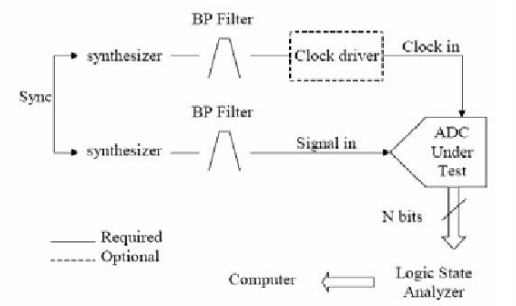

Fig.2. DYNAD sinewave test setup.

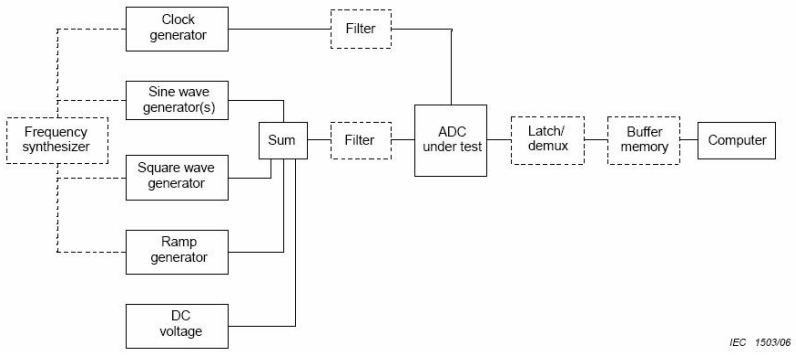

Fig.3. IEC Std. 60748-4-3 test setup.

In particular, the DUTs chosen for the first test round are 3 8-bit ADCs:

- TLC548, successive-approximation ADC produced by Texas Instruments, with a maximum sampling rate of 45.5 kSa/s [11], quoted in the following as ADC1;
- MAX 1198, pipelined ADC produced by Maxim with a maximum sampling rate of 100 MSa/s [12], quoted in the following as ADC2;
- AD9481, pipelined ADC produced by Analog Devices with a maximum sampling rate of 250 MSa/s [13], quoted in the following as ADC3.

The ADC1 has been embedded in a self-made breadboard, the ADC2 and ADC3 have been bought embedded in evaluation boards provided by their manufacturers.

Then, according to the test methods recalled in the previous section, the test frequencies and the record lengths have been chosen for each DUT.

Due to the different architecture of the DUTs, the record length was chosen equal to 2048 samples for ADC1 and 8192 samples for ADC2 and ADC3.

The input signal and the clock frequencies have been chosen as low as possible in order to consider negligible electromagnetic disturbances and phase noise coming from the test setup and environment. This meant to fix the test sampling rates near the maximum for the ADC1 and about 10% or 15% of the maximum for the ADC2 and ADC3. This condition is not a limit to the validity of the achievable results as the target is not to assess the DUT performances but to observe the differences among the figures of merit provided by the different standards in a given test scenario. In all cases, the tests have been carried out adopting coherent sampling.

Successively, several measurement instruments have been chosen to reproduce the actual test benches: the arbitrary waveform generators Tektronix AWG420, Agilent 33220A and Agilent 33250A, the Fluke 5500A calibrator, the Tektronix TDS 5104 digital phosphor oscilloscope (DPO).

The Tektronix AWG420 has been used as trigger source, the Agilent 33250A has been used as clock source, the Agilent 33220A and Fluke 5500A have been used as signal generators, the Tektronix TDS 5104 has been used as signal monitor and to acquire the samples from the serial output interface of ADC1.

In order to verify the correct sources for the DUTs, all the generators have been tested for their spectral purity at the chosen test frequencies by using the Agilent E4404B spectrum analyzer before starting the tests.

The logic state analyzer Tektronix TLA5200 has been used between the ADC2 and the computer to acquire the samples.

The Agilent 53132A frequency counter has been used to verify the generated clock and signal frequencies, to generate a high stability 10 MHz clock, to synchronize the signal generators and the acquisition clock to the same timebase.

Finally, the tests have been carried out following the standard clauses reported in Table 1.

Even if the test bench is the same, the instruments have been connected in different ways according to the different output interfaces of the DUTs.

Figure 4 describes the part of the test setup used for ADC1. In particular, the setup includes the Fluke 5500A Calibrator to generate the input signal, the Tektronix AWG420 to generate the Chip Select (CS) signal and an external trigger to the Agilent 33250A Arbitrary Waveform Generator. This last generates the I/O clock signal to the ADC.

The Tektronix TDS 5104 DPO has been used to provide the ADC serial output waveforms from the analog input signals according to the TLC548 principle of operation. The instruments have been connected to the PC by means of a GPIB.

The setup used for ADC2 includes the Agilent 33220A AWG to generate the input signal, the Agilent 53132A counter to generate the clock signal to the evaluation board, and to synchronize the signal generation with the sampling. The parallel outputs of the evaluation board are acquired and sent to the PC by means of the Tektronix TLA 5200 logic state analyzer.

The test setup for ADC3 is almost the same as for ADC2 with the following relevant differences: (i) the clock to the evaluation board is provided from the Agilent 33250A, and (ii) the ADC samples are sent to the PC by means of a USB interface.

In all the cases the acquired sample records have been processed, according to the clauses in Table 1, by means of Matlab functions implementing the formulas reported in the previous theoretical comparison [3].

V. PRELIMINARY EXPERIMENTAL RESULTS

According to the previous section, the test on ADC1 has been carried out adopting coherent sampling and acquiring records of 2048 samples, considering a sampling frequency of 43.48 kSa/s. Eight sine waves of different frequency and peak to peak amplitude equal to the device full scale (FS) have been provided as input to the ADCs to cover the first Nyquist band. Eight records have been considered to compute the averaged spectrum as reported in the standards.

The ADC serial output waveforms have been acquired by means of the DPO in a single acquisition of 10ms, corresponding to 2048 consecutive samples, and then

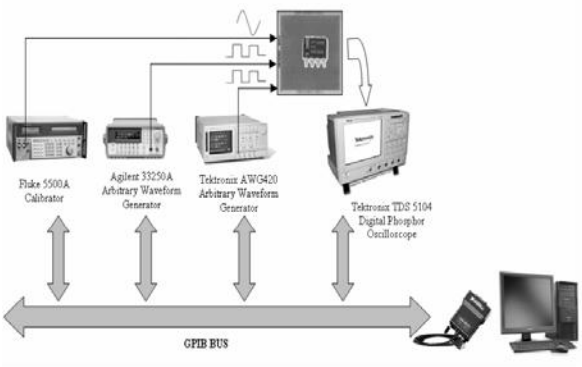

Fig.4. Test setup for the experimental comparison on TLC548.

decoded in the PC by using Matlab. In order to synchronize the acquisition, the timing signals for the ADC (CS and I/O clock) have been routed to separate DPO channels too.

SFDR and THD results for ADC1 obtained from IEC Std. 60748-4-3, IEEE Std.1241, IEEE Std. Draft 1057 and DYNAD are shown in Fig.5. As previously observed in [3], the SFDR formulas proposed by all the standards are almost harmonized with the exception of the different notation. This is clearly visible from the SFDR experimental results obtained from the performed tests (Fig.5a).

The experimental THD results obtained are shown in Fig.5b. As it can be seen, the DYNAD results can be hardly distinguished from the standard results.

The tests on ADC2 and ADC3 were carried out by acquiring records of 8192 samples in coherent sampling conditions, driving the DUT inputs with sine waves at FS peak to peak amplitude. In both cases 15 sine waves of different frequency and peak to peak amplitude equal to the device FS have been provided as input to the ADCs to cover the first Nyquist band. Ten records have been considered to compute the averaged spectrum as reported in the standards.

The tests on ADC2 have been carried out using as sampling clock the 10MHz reference frequency generated from the 53132A high stability timebase.

The tests on ADC3 have been carried out as on ADC2 for the 10 MHz frequency. Moreover, additional tests have been carried out at 20, 30 and 40 MSa/s using the Agilent 33250A as clock source.

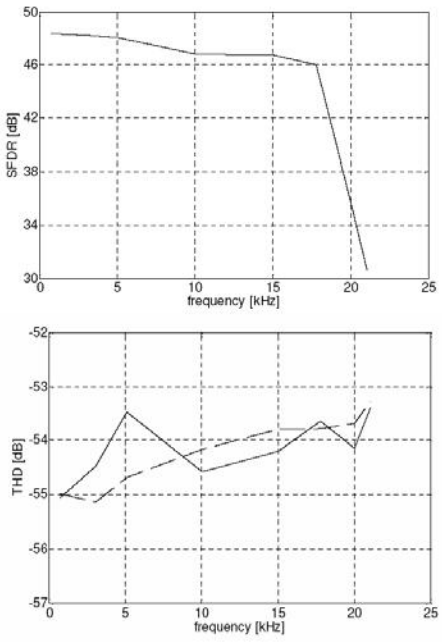

Fig.5.a) SFDR results for TLC548. The obtained SFDR values are equal each other, giving the same line in the plot. b) THD experimental results obtained by using the DYNAD formula (solid line) and the IEC 60748-4-3, IEEE Std. Draft 1057 and IEEE Std. 1241 ones (dashed line).

The results at 10 MSa/s concerning all the figures of merit considered in this paper for both the DUTs are shown in Fig.6.

Also in this last case, it seems clear that although the IEC and IEEE standards formulas are apparently different in notation they are substantially the same by looking at the results. The only relevant difference, highlighted from the experimental results, seems due to the choice made by IEC Std.60748-4-3, IEEE Std. Draft 1057 and IEEE Std.1241 of considering the averaged spectrum unlike DYNAD, that takes into account the averaged spectrum only in the case of SFDR computation.

VI. CONCLUSIONS

In the paper experimental results about the most widely used ADC dynamic parameters, including Spurious Free Dynamic Range, Total Harmonic Distortion, SIgnal to Noise And Distortion ratio, Signal to Noise Ratio and Effective Number Of Bits, have been measured on actual ADCs according to the test methods provided in IEEE Std.1241, IEEE Std. Draft 1057, DYNAD and IEC Std.60748-4-3. The test setups resulting by an experimental investigation on the test signals spectral purity required by the DUTs have comprised both high-value and cheaper instrumentation. The quoted above standards have been analyzed and compared through the obtained experimental results showing a good degree of harmonization.

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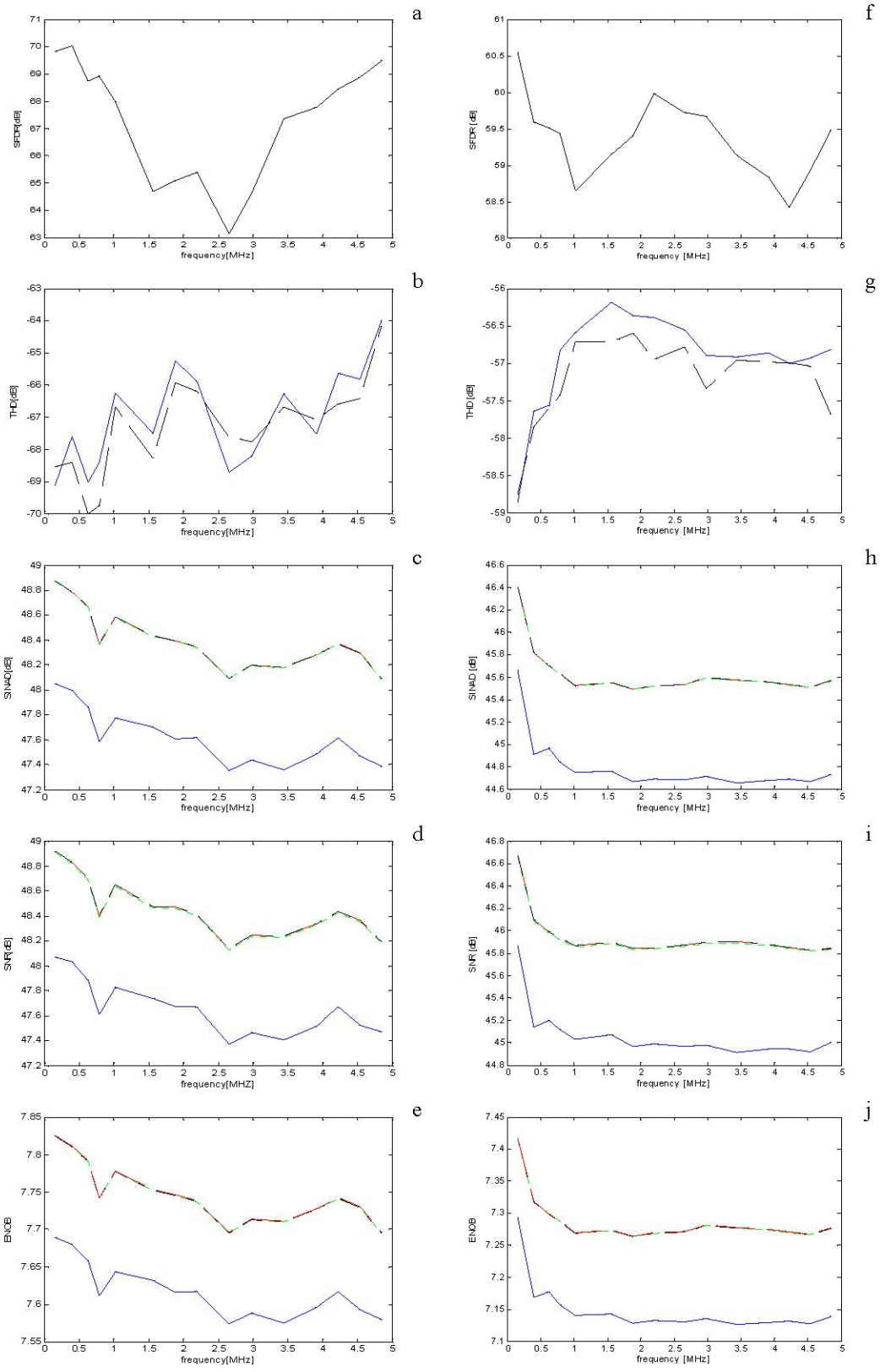

Fig. 6. Test results for ADC2 at 10 MSa/s: a) SFDR, b) THD, c) SINAD, d) SNR, e) ENOB. Test results for ADC3 at 10 MSa/s: f) SFDR, g) THD, h) SINAD, i) SNR, j) ENOB. In all the graphs the blue line represents the results obtained using DYNAD formulas.