D. Maximum CMRR

The amplifier's CMRR is maximized by equating the right side of (18) to zero. Therefore, let

$$\mathrm{CMRR}_2 = -\frac{\mathrm{CMRR}_1'}{\mathrm{CMRR}_1}. \tag{19}$$

For the 3-op-amp *instrumentation amplifier*, $\mathrm{CMRR}_1 = A_{\mathrm{d}1}$ and

$$\mathrm{CMRR}_2 = -\frac{A_{\mathrm{d}1}}{\Delta A_{\mathrm{cm}1}}\,\frac{1}{A_{\mathrm{d}1}} = -\frac{1}{\Delta A_{\mathrm{cm}1}}. \tag{20}$$

For an ideal amplifier where $\Delta A_{\mathrm{cm}1} = 0$, CMRR_2 is infinite and the second stage is tweaked for maximum CMR. Since there is always a small but finite imbalance in the common-mode gains of the first stage, however, the conclusion from the analysis is that the second stage should be adjusted not in isolation but coupled to the first stage with a common-mode voltage applied to the input of the first stage; a standard procedure.

III. Experimental Results

Using an LM747CN strapped with balanced resistors ($r = 1$) and a differential gain of 500, the measured common-mode gain is 7.00×10^{-3} V/V at low frequencies (10 Hz). $R_1 = R_3 = 1.0018$ kΩ and $R_2 = R_4 = 500.5$ kΩ. The common-mode rejection ratio for the device is, therefore, $\mathrm{CMRR}_{\mathrm{d}} = 500/7.00 \times 10^{-3} = 71\,430$, and $CMR_{\mathrm{d}} = 97.07$ dB, which agrees with the published data.

Tweaking the circuit for minimum common-mode gain by adjusting resistor R_4 to unbalance the resistive network, the common-mode gain decreases to 8.75×10^{-4} at $R_4 = 497.3$ kΩ. The CMRR increases to 5.714×10^5, or a CMR of 115.1 dB, an improvement of 18.0 dB over the device's common-mode rejection.

The measured R_4 is equal to the expected theoretical value. For maximum CMRR, the resistance ratio is, from (11), $r = 1/(1 + 500.6/71\,430) = 0.993$, and $R_4 = rR_3(R_2/R_1) = 0.993(500.5) = 497$ kΩ.

IV. Conclusions

The study shows that, by redefining the common-mode rejection ratio to include the phase angle, the theoretically derived CMRR is consistent with practice and simulation; that an amplifier's CMR may exceed the CMR of the device(s) or the external components. The improved CMR is achieved by the unbalancing of the components external to the device.

References

[1] P. H. Garrett. *Analog I/O Design Acquisition: Conversion: Recovery*. Reston, VA: Reston, 1981, ch. 3, pp. 54–57.

[2] R. Pallas-Areny and J. G. Webster, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 669–681, Aug 1991.

Correction to "Comments on 'The Modulo Time Plot: A Useful Data Acquisition Diagnostic Tool'"

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Manuscript received July 16, 1996.

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Publisher Item Identifier S 0018-9456(97)03613-9.

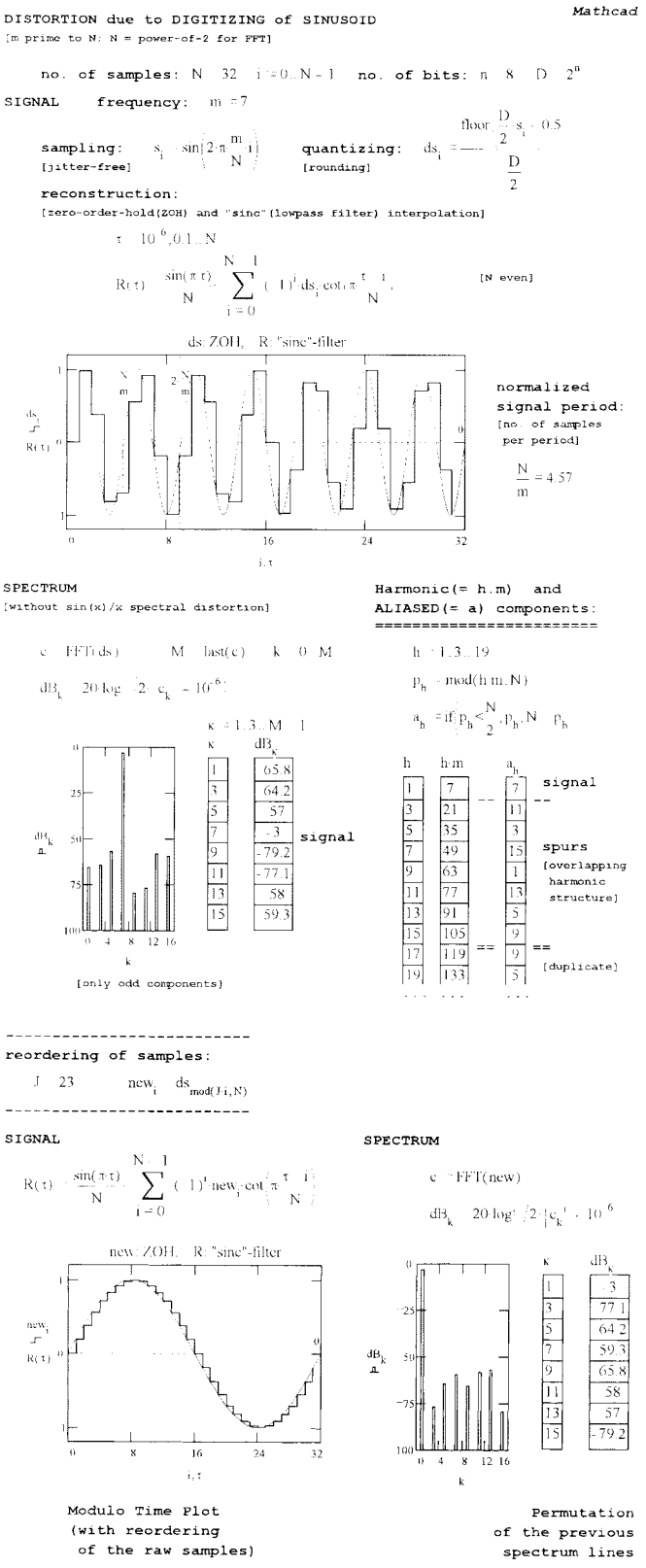

Fig. 1 *Mathcad* simulation: spurious components due to quantization.

In the above paper[1], an error occurred in Fig. 1. An important part of the figure (the reordering of raw samples) was omitted. Shown here is the correct figure in its entirety.

[1] Z. Papay, *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 959, Dec. 1996.